

Advanced HD AVC processor with integrated low power standby controller

Data brief

Features

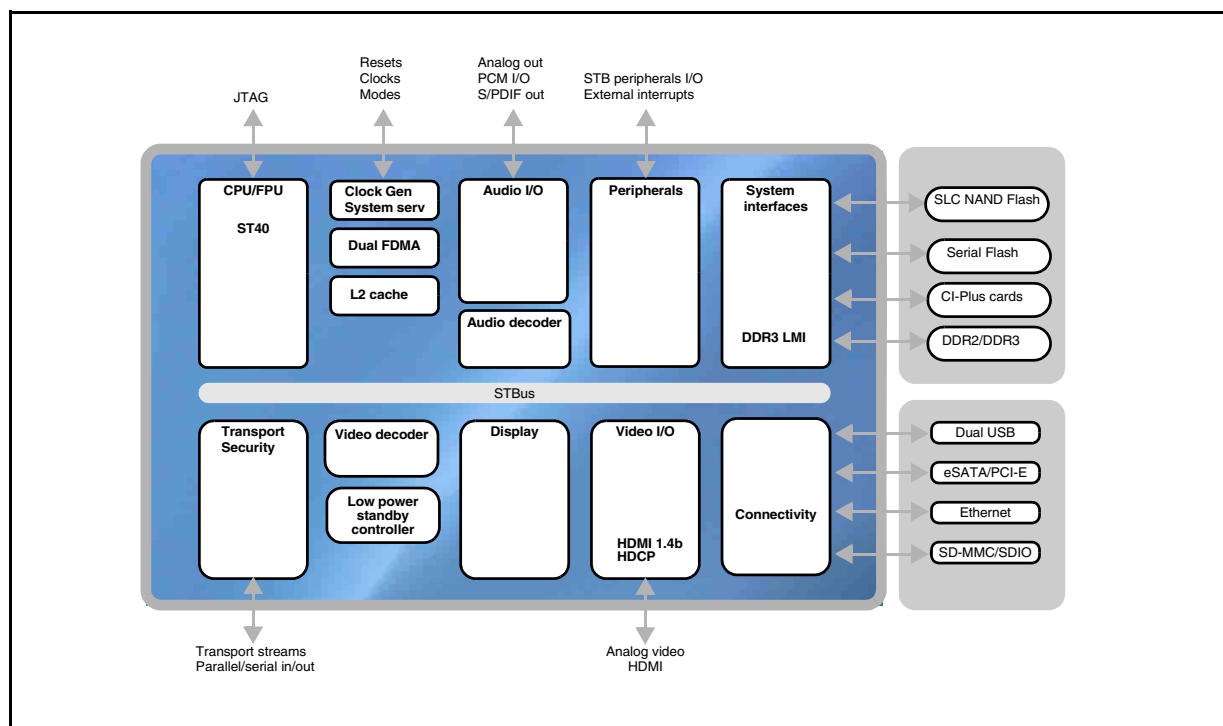
- ST40 applications CPU with 256 KB L2 cache
- 16-bit LMI supporting DDR2/DDR3
- Decoding of H264, MPEG2, VC-1 and AVS HD video streams
- 3DTV decoding and display compatible with HDMI 1.4b
- Extensive connectivity (2 × USB 2.0 ports; Ethernet MII/RMII/TMII port; SD/MMC card port; eSATA port; PCIe)
- Secure booting from SLC NAND Flash or Serial NOR Flash; eMMC booting option
- Low-power process and architecture
- Integrated low power standby controller
- High-quality video resizing and de-interlacing
- Integrated Ethernet PHY

- Targets two layer PCBs for cost-effective zapper STB applications
- 23 mm x 23 mm PBGA package

Description

The STiH205 uses the latest process technology to provide a cost-effective, feature rich, highly integrated SoC for set-top boxes (STBs). It is targeted at the advanced decoding STB market across all networks (cable/satellite/DTT/x-DSL/IP) worldwide and is suitable for operator markets (with advanced security) and retail markets.

The STiH205 provides a solution for operators and manufacturers to specify a range of cost-effective, high performance zapper STBs, interactive STBs, IP clients, and DVR STBs with content delivery possible using broadcast or broadband networks, or both (Hybrid STBs).



1 Introduction

The STiH205 offers current users of ST's growing family of advanced decoding ICs enhancements in performance and features, enabling operators to offer consumers new multimedia-rich services and viewing experiences, including new 3DTV features. Faster DDR3 memory is also supported, and the applications CPU benefits from an L2 cache. The STiH205 keeps pace with the latest advanced security requirements of the main CA vendors, and an integrated standby controller enables the STiH205 to target stringent low power regulations.

Features

ST40 applications CPU, with 32 KI and 32 KD L1 caches and 256 Kbyte L2 cache.

Integrated low power standby controller within its own power island.

Latest generation of ST's Delta video decoder, coupled with a High Quality Video Display Pipeline (HQVDP).

Dual USB 2.0 hosts, eSATA, Ethernet MAC with MII/RMII/TMII interfaces, PCI-e, SD-MMC/SDIO interface.

NOCS3.0, NSK2.0 and DVB-CSA3 ready.

23 mm x 23 mm package, smaller than other STiH205/STiH207 family variants.

Benefits

High performance processing for applications and middleware.

Secure hibernation to, and fast resume from, very low power passive standby mode, targeting STB standby power < 0.5 W.

Decoding of advanced high-definition standards (MPEG2, H264, VC-1, AVS) plus the performance and flexibility for web-based content decoding such as Flash[®], DivX[™], MJPEG and Real[®], without impacting applications CPU performance.

Extensive high-speed connectivity for the widest range of STB peripherals, such as Flash drives, external HDDs, Ethernet, home network controllers (such as MoCA[®], Wi-Fi), DOCSIS[®] modem and memory cards.

Fully compliant with the latest advanced security requirements of CA vendors.

Ideal for space constrained form factors such as dongles and plug based STBs and media players.

2 Revision history

Table 1. Document revision history

Date	Revision	Changes
22-Jul-2011	1	Initial release.
09-Feb-2012	2	<ul style="list-style-type: none">– Replaced decoder by processor in the title.– Updated the cover page diagram.
30-Aug-2012	3	<ul style="list-style-type: none">– Updated the second last point of <i>Features on page 2</i>.– Added last row in Features and benefits table.– Replaced HDMI 1.4a by HDMI 1.4b in the <i>Features on page 1</i>.– Added a feature related to package in the <i>Features on page 1</i>.

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