



AK4425A

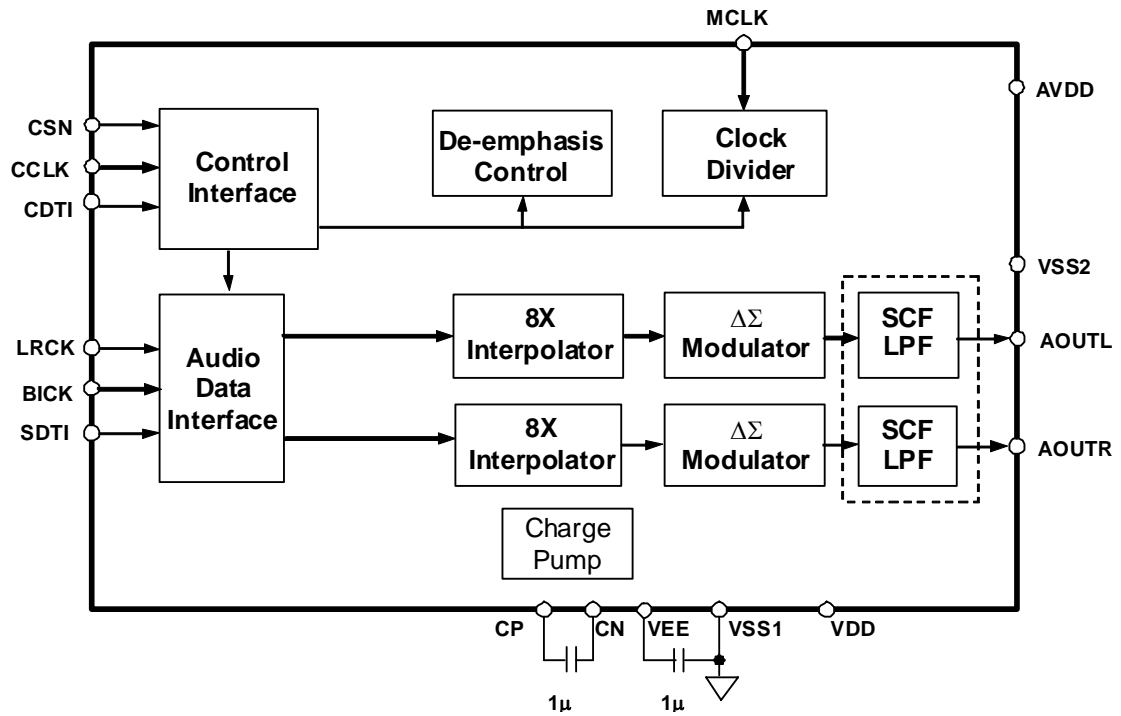
192kHz 24-Bit Stereo $\Delta\Sigma$ DAC with 2Vrms Output

GENERAL DESCRIPTION

The AK4425A is a 5V 24-bit stereo DAC with an integrated 2Vrms output buffer. A charge pump in the buffer develops an internal negative power supply rail that enables a ground-referenced 2Vrms output. Using AKM's multi bit modulator architecture, the AK4425A delivers a wide dynamic range while preserving linearity for improved THD+N performance. The AK4425A integrates a combination of switched-capacitor and continuous-time filters, increasing performance for systems with excessive clock jitter. The 24-bit word length and 192kHz sampling rate make this part ideal for a wide range of consumer audio applications, such as DVD, AV receiver system and set-top boxes. The AK4425A is offered in a space saving 16pin TSSOP package.

FEATURES

- Sampling Rate Ranging from 8kHz to 192kHz
- 128 times Oversampling (Normal Speed Mode)
- 64 times Oversampling (Double Speed Mode)
- 32 times Oversampling (Quad Speed Mode)
- 24-Bit 8 times FIR Digital Filter
- Switched-Capacitor Filter with High Tolerance to Clock Jitter
- Single Ended 2Vrms Output Buffer
- Digital De-emphasis Filter: 32kHz, 44.1kHz or 48kHz
- Soft mute
- Digital Attenuator (Linear 256 Step)
- Control I/F: 3-wire
- Audio I/F format: 24Bit MSB justified, 24/20/16 LSB justified or I²S compatible
- Master clock: 256fs, 384fs, 512fs, 768fs or 1152fs (Normal Speed Mode)
128fs, 192fs, 256fs or 384fs (Double Speed Mode)
128fs, 192fs (Quad Speed Mode)
- THD+N: -91dB
- Dynamic Range: 106dB
- Automatic Power-on Reset Circuit
- Power supply: +4.5 ~ +5.5V
- Ta = -20 to 85°C
- Small Package: 16pin TSSOP (6.4mm x 5.0mm)



Block Diagram

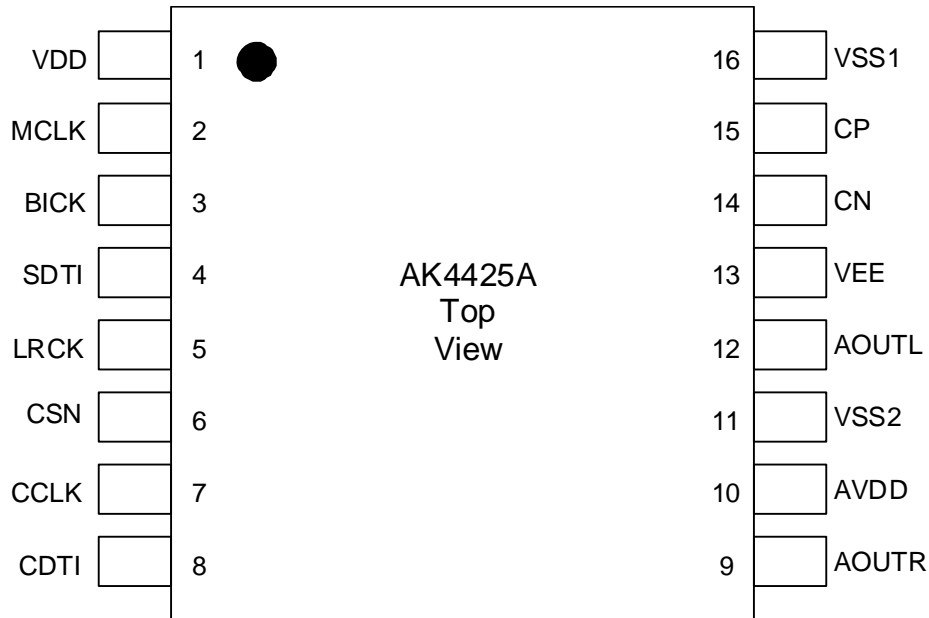
■ Ordering Guide

AK4425AET
AKD4425A

-20 ~ +85°C

16pin TSSOP (0.65mm pitch)
Evaluation Board for AK4425A

■ Pin Layout



■ Compatibility with the AK4426

Functions	AK4426	AK4425A
Power Supply	+4.5 ~ +5.5V	←
DC Offset	± 8mV	± 5mV
THD+N	-91dB	←
DR	106dB	←
DEM	X	←
SMUTE	X	←
Digital ATT	X	←
I/F Format	24-bit MSB/ I ² S/ 24,20,16bitLSB	←
Control I/F	I ² C	←
Operating Temperature	ET: -20 ~ +85°C VT: -40 ~ +85°C	←

-: Not available

X: Available

PIN/FUNCTION

No.	Pin Name	I/O	Function
1	VDD	-	Digital Circuit and Charge Pump Circuit Power Supply Pin: 4.5V~5.5V
2	MCLK	I	Master Clock Input Pin An external TTL clock must be input on this pin.
3	BICK	I	Audio Serial Data Clock Pin
4	SDTI	I	Audio Serial Data Input Pin
5	LRCK	I	L/R Clock Pin
6	CSN	I	Chip Select Pin
7	CCLK	I	Control Clock input Pin
8	CDTI	I	Control Data Input Pin
9	AOUTR	O	Rch Analog Output Pin When power down, outputs VSS(0V, typ).
10	AVDD	-	Analog Block Power Supply Pin: 4.5V~5.5V
11	VSS2	-	Ground Pin2
12	AOUTL	O	Lch Analog Output Pin When power down, outputs VSS(0V, typ).
13	VEE	O	Negative Voltage Output Pin Connect to VSS1 with a 1.0 μ F capacitor which is low ESR (Equivalent Series Resistance) over all temperature range. When this capacitor has the polarity, the positive polarity pin must be connected to the VSS1 pin. Non polarity capacitors can also be used.
14	CN	I	Negative Charge Pump Capacitor Terminal Pin Connect to CP with a 1.0 μ F capacitor which is low ESR (Equivalent Series Resistance) over all temperature range. When this capacitor has the polarity, the positive polarity pin must be connected to the CP pin. Non polarity capacitors can also be used.
15	CP	I	Positive Charge Pump Capacitor Terminal Pin Connect to CN with a 1.0 μ F capacitor which is low ESR (Equivalent Series Resistance) over all temperature range. When this capacitor has the polarity, the positive polarity pin must be connected to the CP pin. Non polarity capacitors can also be used.
16	VSS1	-	Ground Pin1

Note: All input pins except for the CN pin should not be left floating.

ABSOLUTE MAXIMUM RATINGS

(VSS1=VSS2=0V; [Note 1](#))

Parameter	Symbol	min	max	Units
Power Supply	VDD	-0.3	+6.0	V
	CVDD	-0.3	+6.0	V
Input Current (any pins except for supplies)	IIN	-	±10	mA
Input Voltage	VIND	-0.3	VDD+0.3	V
Ambient Operating Temperature	Ta	-20	85	°C
Storage Temperature	Tstg	-65	150	°C

Note 1. All voltages with respect to ground.

Note 2. VSS1, VSS2 connect to the same analog ground.

WARNING: Operation at or beyond these limits may result in permanent damage to the device.

Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS

(VSS1=VSS2=0V; [Note 1](#))

Parameter	Symbol	min	typ	max	Units
Power Supply	VDD	+4.5	+5.0	+5.5	V
	AVDD		VDD		

Note 3. AVDD should be equal to VDD

*AKM assumes no responsibility for the usage beyond the conditions in this datasheet.

ANALOG CHARACTERISTICS

(Ta = 25°C; VDD=AVDD = +5.0V; fs = 44.1 kHz; BICK = 64fs; Signal Frequency = 1 kHz;
24bit Input Data; Measurement frequency = 20Hz ~ 20kHz; Ri ≥5kΩ)

Parameter	min	typ	max	Units	
Resolution			24	Bits	
Dynamic Characteristics (Note 4)					
THD+N	fs=44.1kHz, BW=20kHz		-91	-84	dB
	fs=96kHz, BW=40kHz		-91	-	dB
	fs=192kHz, BW=40kHz		-91	-	dB
Dynamic Range (-60dBFS with A-weighted. (Note 5))	100	106		dB	
S/N (A-weighted. (Note 6))	100	106		dB	
Interchannel Isolation (1kHz)	90	100		dB	
Interchannel Gain Mismatch		0	0.5	dB	
DC Accuracy					
DC Offset (at output pin)	-5	0	+5	mV	
Gain Drift		100	-	ppm/°C	
Output Voltage (Note 7)	2.05	2.2	2.35	Vrms	
Load Capacitance (Note 8)			25	pF	
Load Resistance	5			kΩ	
Power Supplies					
Power Supply Current: (Note 9)					
Normal Operation (fs≤96kHz)		24	36	mA	
Normal Operation (fs=192kHz)		27	40	mA	
Power-Down Mode (Note 10)		10	100	μA	

Note 4. Measured by Audio Precision (System Two). Refer to the evaluation board manual.

Note 5. 98dB for 16bit input data

Note 6. S/N does not depend on input data size.

Note 7. Full-scale voltage (0dB). Output voltage is proportional to the voltage of VDD,

$$AOUT (typ.@0dB) = 2.2V_{rms} \times VDD/5.$$

Note 8. In case of driving capacitive load, inset a resistor between the output pin and the capacitive load.

Note 9. The current into VDD and AVDD.

Note 10. All digital inputs including clock pins (MCLK, BICK and LRCK) are fixed to VSS1(VSS2) or VDD(AVDD).

SHARP ROLL-OFF FILTER CHARACTERISTICS
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(Ta = 25°C; VDD=AVDD = +4.5 ~ +5.5V; fs = 44.1 kHz; DEM = OFF; SLOW = "0")

Parameter	Symbol	min	typ	max	Units	
Digital filter						
Passband	±0.05dB (Note 11) -6.0dB	PB	0	20.0	kHz	
			-	-	kHz	
Stopband (Note 11)		SB	24.1		kHz	
Passband Ripple		PR		± 0.02	dB	
Stopband Attenuation		SA	54		dB	
Group Delay (Note 12)		GD	-	19.3	1/fs	
Digital Filter + LPF						
Frequency Response	20.0kHz	fs=44.1kHz	FR	-	± 0.05	dB
	40.0kHz	fs=96kHz	FR	-	± 0.05	dB
	80.0kHz	fs=192kHz	FR	-	± 0.05	dB

Note 11. The passband and stopband frequencies scale with fs(system sampling rate).

For example, PB=0.4535×fs (@±0.05dB), SB=0.546×fs.

Note 12. Calculated delay time caused by digital filter. This time is measured from setting the 16/24bit data of both channels to input register to the output of the analog signal.

SLOW ROLL-OFF FILTER CHARACTERISTICS

(Ta = 25°C; VDD=AVDD = +4.5 ~ +5.5V; fs = 44.1kHz; DEM = OFF; SLOW = "1")

Parameter	Symbol	min	typ	max	Units	
Digital Filter						
Passband	±0.04dB (Note 13) -3.0dB	PB	0	8.1	kHz	
			-	-	kHz	
Stopband (Note 13)		SB	39.2		kHz	
Passband Ripple		PR		± 0.005	dB	
Stopband Attenuation		SA	72		dB	
Group Delay (Note 12)		GD	-	19.3	1/fs	
Digital Filter + LPF						
Frequency Response	20.0kHz	fs=44.kHz	FR	-	+0/-5	dB
	40.0kHz	fs=96kHz	FR	-	+0/-4	dB
	80.0kHz	fs=192kHz	FR	-	+0/-5	dB

Note 13. The passband and stopband frequencies scale with fs(system sampling rate).

For example, PB=0.185×fs (@±0.04dB), SB=0.888×fs.

DC CHARACTERISTICS

(Ta = 25°C; VDD=AVDD = +4.5 ~ +5.5V)

Parameter	Symbol	min	typ	max	Units
High-Level Input Voltage	VIH	2.2	-	-	V
Low-Level Input Voltage	VIL	-	-	0.8	V
Input Leakage Current	Iin	-	-	± 10	μA

SWITCHING CHARACTERISTICS

(Ta = 25°C; VDD=AVDD = +4.5 ~ +5.5V)

Parameter	Symbol	min	Typ	max	Units
Master Clock Frequency	fCLK	2.048	11.2896	36.864	MHz
Duty Cycle	dCLK	30		70	%
LRCK Frequency					
Normal Speed Mode	fsn	8		48	kHz
Double Speed Mode	fsd	32		96	kHz
Quad Speed Mode	fsq	120		192	kHz
Duty Cycle	Duty	45		55	%
Audio Interface Timing					
BICK Period					
Normal Speed Mode	tBCK	1/128fsn			ns
Double Speed Mode	tBCK	1/64fsd			ns
Quad Speed Mode	tBCK	1/64fsq			ns
BICK Pulse Width Low	tBCKL	30			ns
Pulse Width High	tBCKH	30			ns
BICK “↑” to LRCK Edge (Note 14)	tBLR	20			ns
LRCK Edge to BICK “↑” (Note 14)	tLRB	20			ns
SDTI Hold Time	tSDH	20			ns
SDTI Setup Time	tSDS	20			ns
Control Interface Timing					
CCLK Period	tCCK	200			ns
CCLK Pulse Width Low	tCCKL	80			ns
Pulse Width High	tCCKH	80			ns
CDTI Setup Time	tCDS	40			ns
CDTI Hold Time	tCDH	40			ns
CSN High Time	tCSW	150			ns
CSN “↓” to CCLK “↑”	tCSS	50			ns
CCLK “↑” to CSN “↑”	tCSH	50			ns

Note 14. BICK rising edge must not occur at the same time as LRCK edge.

■ Timing Diagram

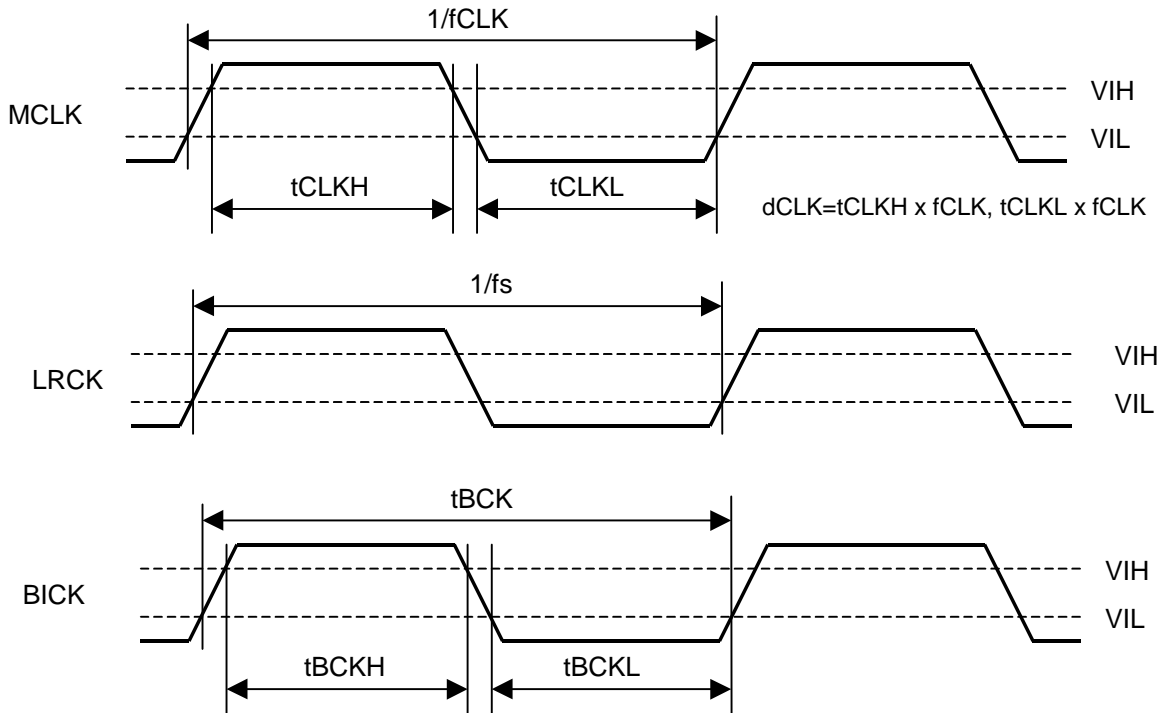


Figure 1. Clock Timing

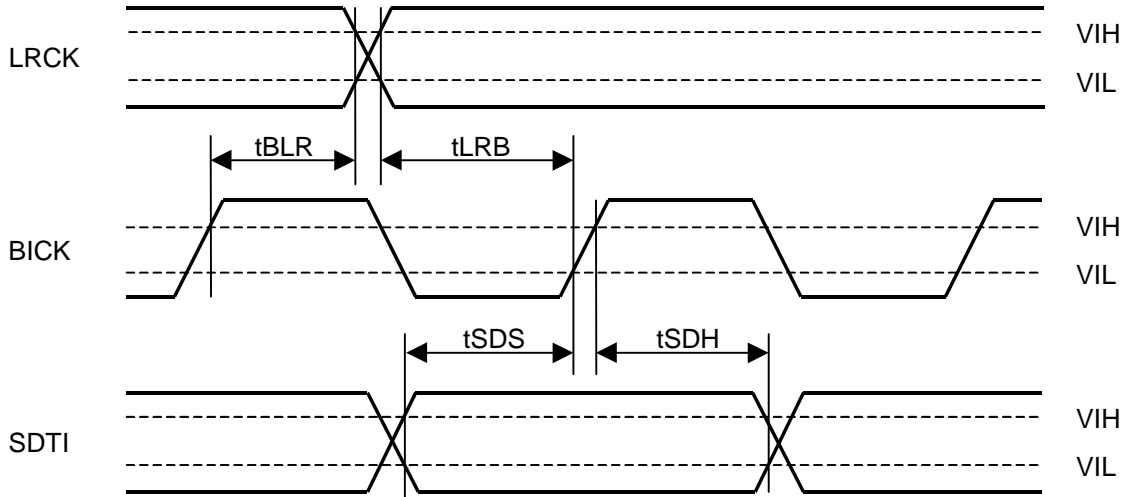


Figure 2. Serial Interface Timing

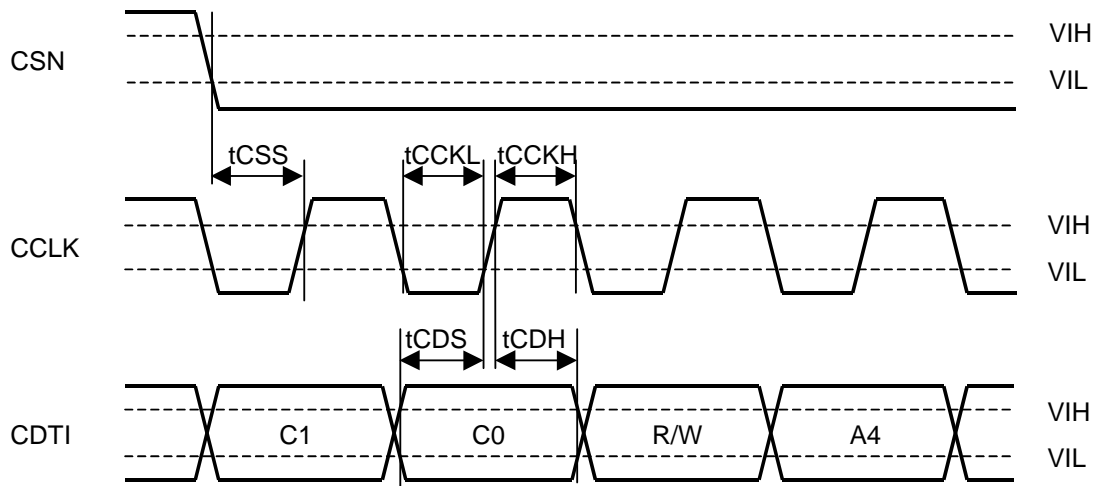


Figure 3. WRITE Command Input Timing

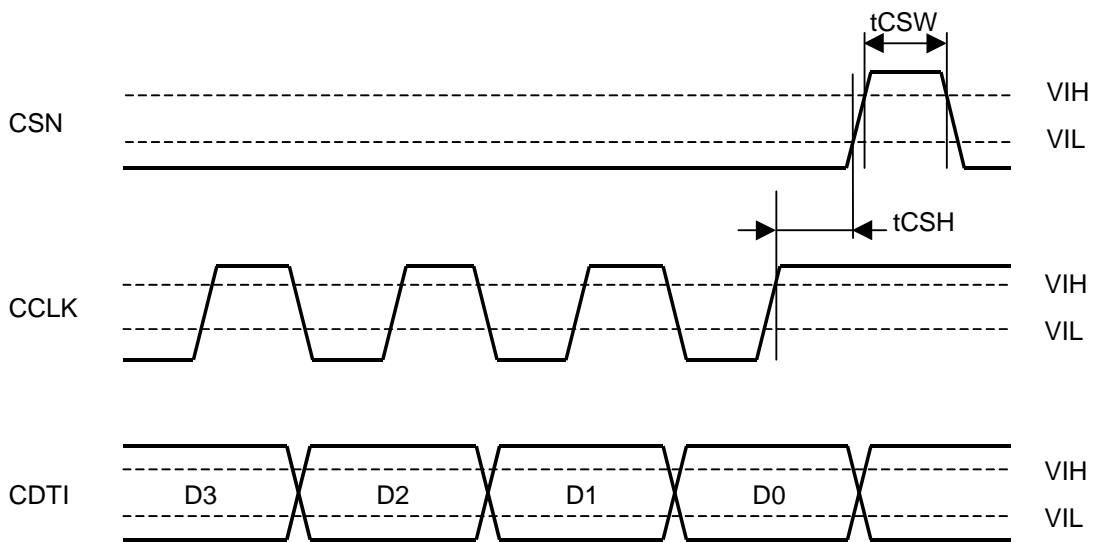


Figure 4. WRITE Data Input Timing

OPERATION OVERVIEW

■ System Clock

The external clocks required to operate the AK4425A are MCLK, LRCK and BICK. The master clock (MCLK) should be synchronized with LRCK but the phase is not critical. The MCLK is used to operate the digital interpolation filter and the delta-sigma modulator. The MCLK is used to operate the digital interpolation filter and the delta-sigma modulator. There are two methods to set MCLK frequency. In Manual Setting Mode (ACKS = "0": Register 00H), the sampling speed is set by DFS0/1 (Table 1). The frequency of MCLK at each sampling speed is set automatically. (Table 2) When the power applied, the AK4425A is in Auto Setting Mode. In Auto Setting Mode (ACKS = "1": Default), as MCLK frequency is detected automatically (Table 3), and the internal master clock becomes the appropriate frequency (Table 4), it is not necessary to set DFS0/1.

The AK4425A is automatically placed in power saving mode when MCLK, LRCK and BICK stop during normal operation mode, and the analog output is forced to 0V(typ). When MCLK, LRCK and BICK are input again, the AK4425A is powered up. After power-up, the AK4425A is in the power-down mode until MCLK, LRCK and BICK are input.

DFS1	DFS0	Sampling Rate (fs)	
0	0	Normal Speed Mode	8kHz~48kHz
0	1	Double Speed Mode	60kHz~96kHz
1	0	Quad Speed Mode	120kHz~192kHz

(default)

Table 1. Sampling Speed (Manual Setting Mode)

DFS1	DFS0	Sampling Speed	LRCK (kHz)	MCLK (MHz)						BICK (MHz)	
				fs	128fs	192fs	256fs	384fs	512fs		768fs
0	0	Normal	32.0	-	-	8.1920	12.2880	16.3840	24.5760	36.8640	2.0480
0	0		44.1	-	-	11.2896	16.9344	22.5792	33.8688	-	2.8224
0	0		48.0	-	-	12.2880	18.4320	24.5760	36.8640	-	3.0720
0	1	Double	88.2	11.2896	16.9344	22.5792	33.8688	-	-	-	5.6448
0	1		96.0	12.2880	18.4320	24.5760	36.8640	-	-	-	6.1440
1	0	Quad	176.4	22.5792	33.8688	-	-	-	-	-	11.2896
1	0		192.0	24.5760	36.8640	-	-	-	-	-	12.2880

Table 2. System Clock Example

MCLK		Sampling Speed
1152fs		Normal (fs=32kHz only)
512fs	768fs	Normal
256fs	384fs	Double
128fs	192fs	Quad

Table 3. Sampling Speed(Auto Setting Mode: Default)

LRCK fs	MCLK (MHz)							Sampling Speed
	128fs	192fs	256fs	384fs	512fs	768fs	1152fs	
32.0kHz	-	-	-	-	16.3840	24.5760	36.8640	Normal
44.1kHz	-	-	-	-	22.5792	33.8688	-	
48.0kHz	-	-	-	-	24.5760	36.8640	-	
32.0kHz			8.192	12.288				Double
44.1kHz			11.2896	16.9344				
48.0kHz			12.288	18.432				
88.2kHz	-	-	22.5792	33.8688	-	-	-	
96.0kHz	-	-	24.5760	36.8640	-	-	-	Quad
176.4kHz	22.5792	33.8688	-	-	-	-	-	
192.0kHz	24.5760	36.8640	-	-	-	-	-	

Table 4. System Clock Example (Auto Setting Mode)

When MCLK= 256fs/384fs, the AK4425A supports sampling rate of 32kHz~96kHz in auto setting mode (Table 4). But, when the sampling rate is 32kHz~48kHz, DR and S/N will degrade by approximately 3dB as compared to when MCLK= 512fs/768fs.

MCLK	DR,S/N
256fs/384fs	103dB
512fs/768fs	106dB

Table 5. Relationship between MCLK frequency and DR, S/N (fs= 44.1kHz) (Auto Setting Mode)

■ Audio Serial Interface Format

The audio data is shifted in via the SDTI pin using the BICK and LRCK inputs. The DIF2-0 bit can select within five serial data modes as shown in Table 6. In all modes the serial data is MSB-first, two's complement format and it is latched on the rising edge of BICK. Mode 2 can be used for 16/20 MSB justified formats by zeroing the unused LSBs.

Mode	DIF2	DIF1	DIF0	SDTI Format	BICK	Figure
0	0	0	0	16bit LSB Justified	≥32fs	Figure 5
1	0	0	1	20bit LSB Justified	≥40fs	Figure 6
2	0	1	0	24bit MSB Justified	≥48fs	Figure 7
3	0	1	1	24bit I ² S Compatible	≥48fs	Figure 8
4	1	0	0	24bit LSB Justified	≥48fs	Figure 6

(default)

Table 6. Audio Data Format in Serial control mode

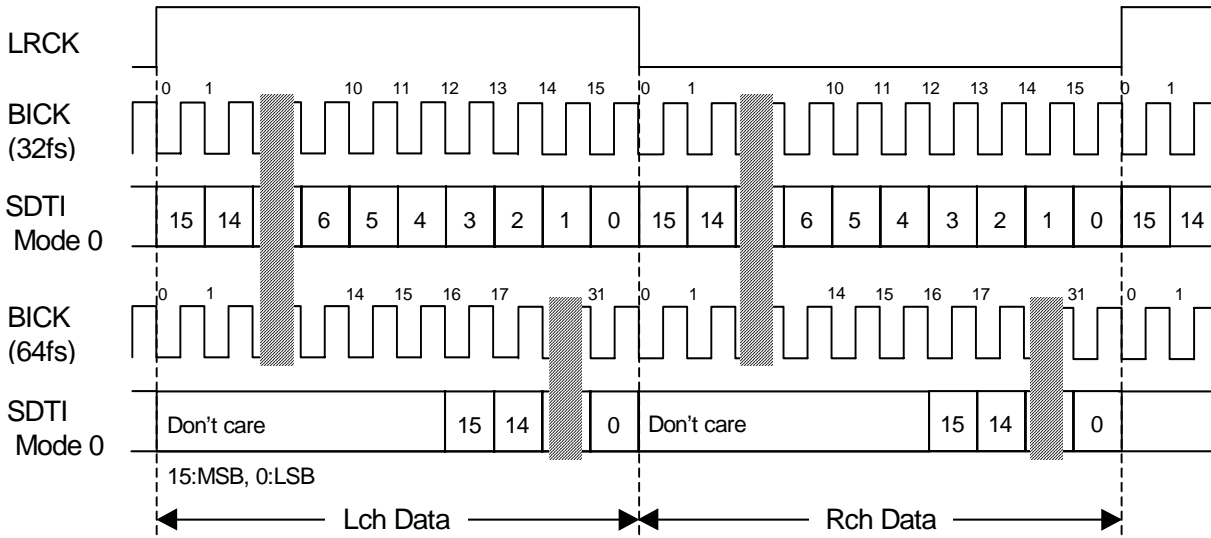


Figure 5. Mode 0 Timing

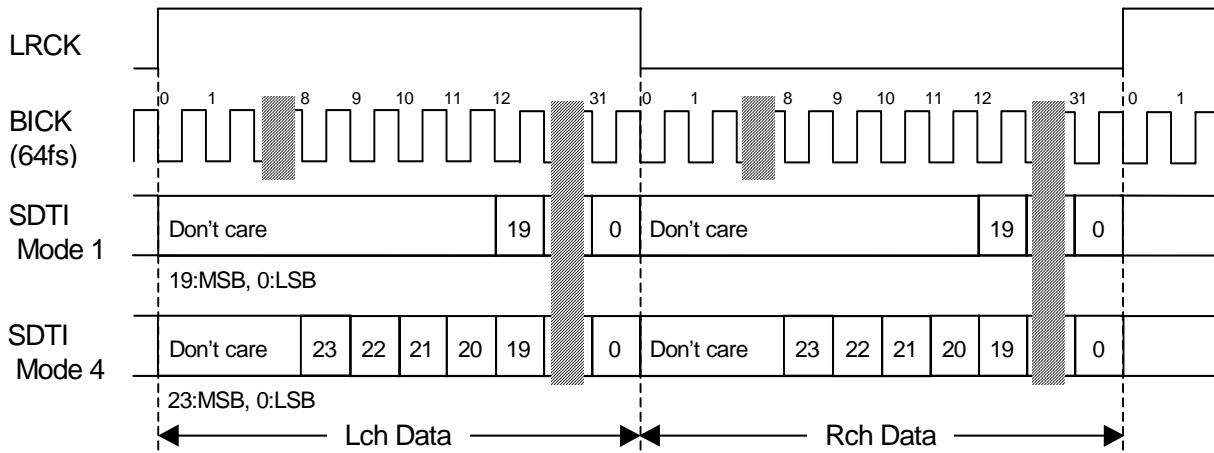


Figure 6. Mode 1/4 Timing

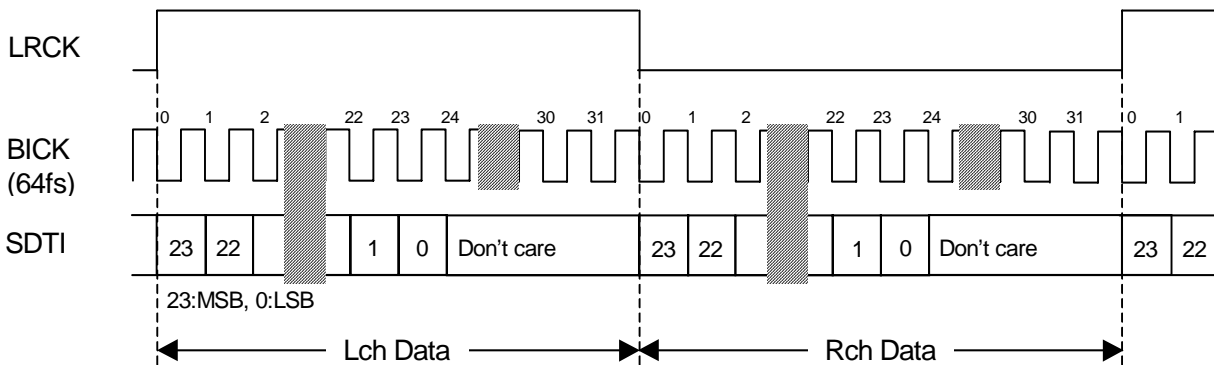


Figure 7. Mode 2 Timing

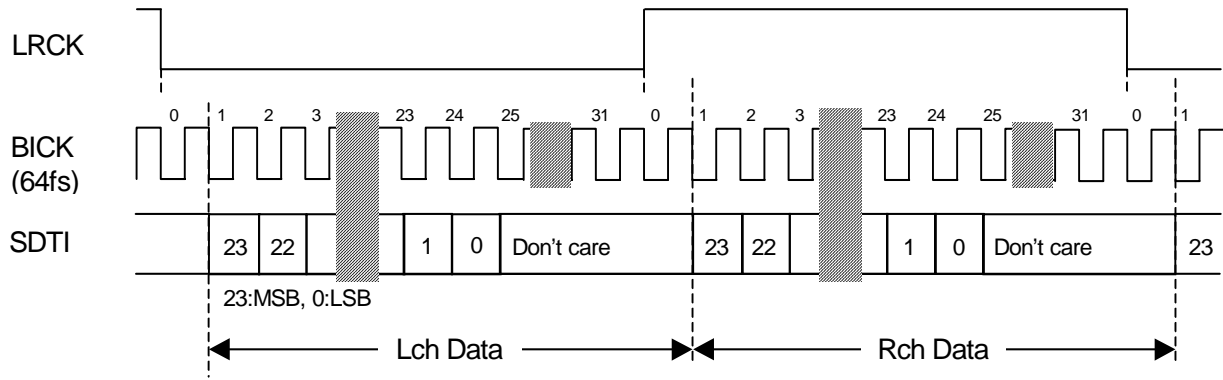


Figure 8. Mode 3 Timing

■ De-emphasis Filter

A digital de-emphasis filter is available for 32, 44.1 or 48kHz sampling rates ($t_c = 50/15\mu s$) and it is enabled or disabled by DEM0 and DEM1. In case of double speed and quad speed mode, the digital de-emphasis filter is always OFF.

DEM1	DEM0	Mode
0	0	44.1kHz
0	1	OFF
1	0	48kHz
1	1	32kHz

Table 7. De-emphasis Filter Control (Normal Speed Mode)

■ Analog Output Block

The internal negative power supply generation circuit (Figure 9) provides a negative power supply for the internal 2Vrms amplifier. It allows the AK4425A to output an audio signal centered at VSS (0V, typ) as shown in Figure 10. The negative power generation circuit (Figure 9) needs 1.0uF capacitors (Ca, Cb) with low ESR (Equivalent Series Resistance). If this capacitor is polarized, the positive polarity pin should be connected to the CP and VSS1 pins. This circuit operates by clocks generated from MCLK. When MCLK stops, the AK4425A is placed in the reset mode automatically and the analog outputs settle to VSS (0V, typ).

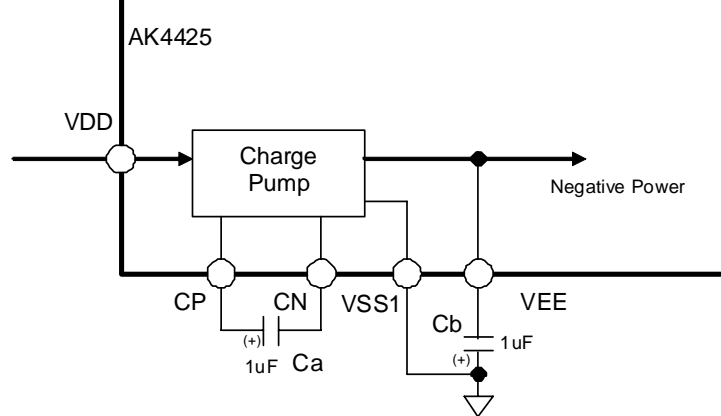


Figure 9. Negative Power Generation Circuit

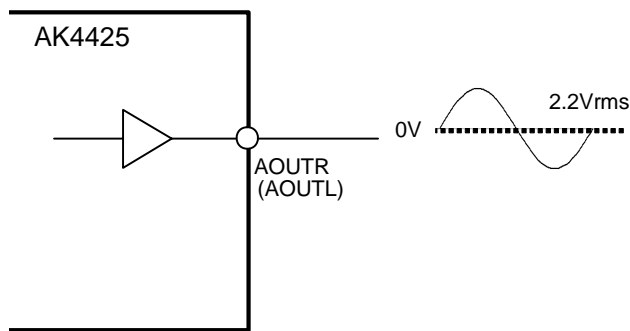


Figure 10. Audio Signal Output

■ Output Volume

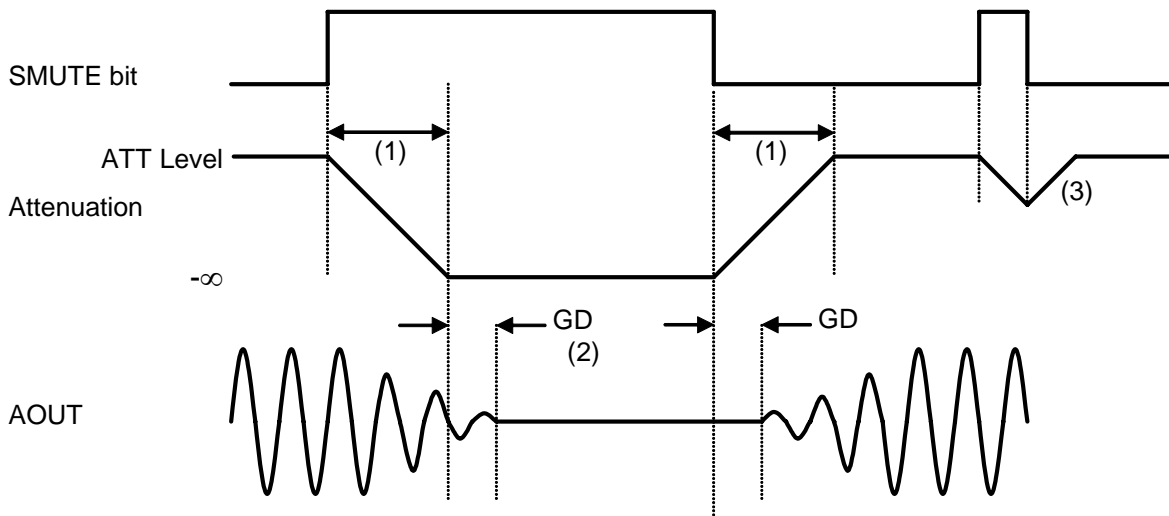
The AK4425A includes channel independent digital output volumes (ATT) with 256 levels at linear step including MUTE. These volumes are in front of the DAC and can attenuate the input data from 0dB to -48dB and mute. When changing levels, transitions are executed via soft changes; thus no switching noise occurs during these transitions. The transition time of 1 level and all 256 levels is shown in Table 8.

Sampling Speed	Transition Time	
	1 Level	255 to 0
Normal Speed Mode	4LRCK	1020LRCK
Double Speed Mode	8LRCK	2040LRCK
Quad Speed Mode	16LRCK	4080LRCK

Table 8. ATT Transition Time

■ Soft Mute Operation

Soft mute operation is performed in digital domain. When the SMUTE bit is set to “1”, the output signal is attenuated by $-\infty$ during ATT_DATA×ATT transition time (Table 8) from the current ATT level. When the SMUTE bit is returned to “0”, the mute is cancelled and the output attenuation gradually changes to the ATT level during ATT_DATA×ATT transition time. If the soft mute is cancelled before attenuating to $-\infty$, the attenuation is discontinued and returned to ATT level by the same cycle. The soft mute is effective for changing the signal source without stopping the signal transmission.



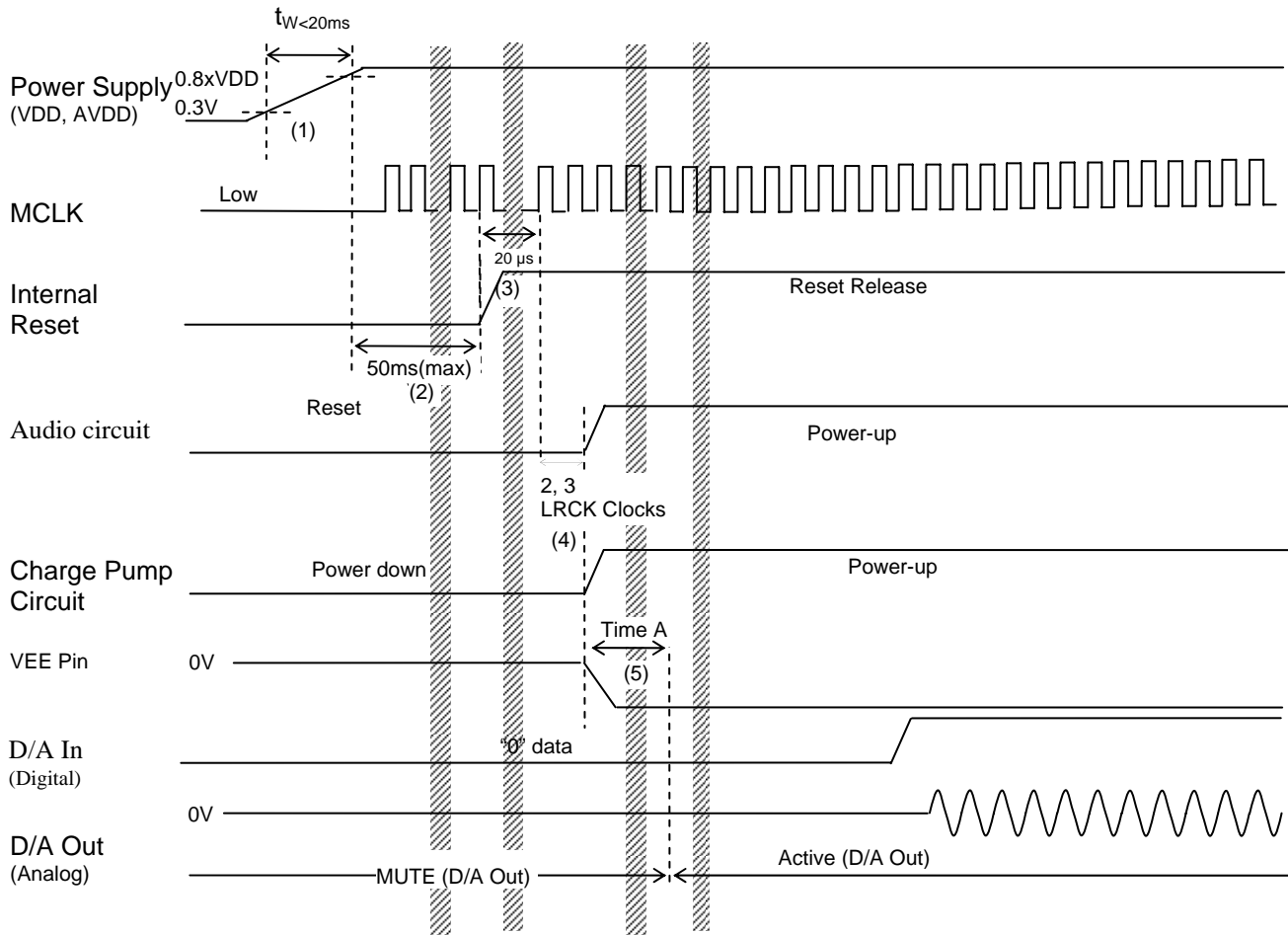
Notes:

- (1) ATT_DATA×ATT transition time (Table 8). For example, in Normal Speed Mode, this time is 1020LRCK cycles (1020/fs) at ATT_DATA=255.
- (2) The analog output corresponding to the digital input has group delay, GD.
- (3) If the soft mute is cancelled before attenuating to $-\infty$ after starting the operation, the attenuation is discontinued and returned to ATT level by the same cycle.

Figure 11. Soft Mute function

■ System Reset

The AK4425A is in power down mode upon power-up. The MCLK should be input after the power supplies are ramped up. The AK4425A is in power-down mode until LRCK are input.



Notes:

- (1) The AK4425A includes an internal Power on Reset Circuit which is used reset the digital logic into a default state after power up. Therefore, the power supply voltage must reach 80% VDD from 0.3V in less than 20msec.
- (2) Register writings are valid after 50ms (max).
- (3) When internal reset is released, approximately 20us after a MCLK input, the internal analog circuit is powered-up.
- (4) The digital circuit and charge pump circuit are powered-up in 2, 3 LRCK cycle when the analog circuit is powered-up.
- (5) The charge pump counter starts after the charge pump circuit is powered-up. The DAC outputs a valid analog signal after Time A.

Time A = $1024 / (f_s \times 16)$: Normal speed mode

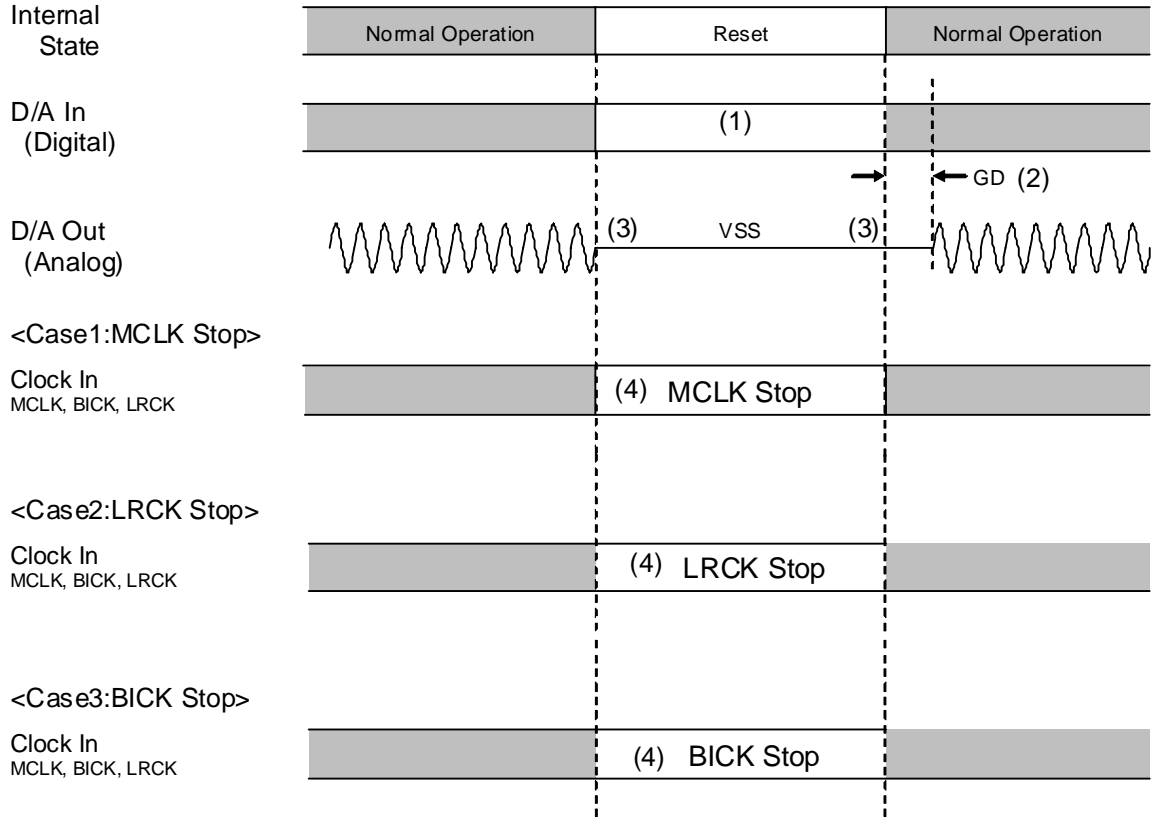
Time A = $1024 / (f_s \times 8)$: Double speed mode

Time A = $1024 / (f_s \times 4)$: Quad speed mode

Figure 12. System Reset Diagram

■ Reset Function

When the MCLK, LRCK or BICK stops, the AK4425A is placed in reset mode and its analog outputs are set to VSS (0V, typ). When the MCLK, LRCK and BICK are restarted, the AK4425A returns to normal operation mode.



Notes:

- (1) Digital data can be stopped. The click noise after MCLK, LRCK and BICK are input again can be reduced by inputting the “0” data during this period.
- (2) The analog output corresponding to a specific digital input has group delay (GD).
- (3) No audible click noise occurs under normal conditions.
- (4) Clocks (MCLK, BICK, LRCK) can be stopped in the reset mode (MCLK or LRCK is stopped).

Figure 13. Reset Timing Example

■ Mode Control Interface

The function of the AK4425A can be controlled by register settings. The register can be accessed 50msec(max) after power up the AK4425A. Internal registers may be written to 3-wire μ P interface pins, CSN, CCLK and CDTI. The data on this interface consists of Chip Address (2bits, C1/0; fixed to "01"), Read/Write (1bit; fixed to "1", Write only), Register Address (MSB first, 5bits) and Control Data (MSB first, 8bits). Address and data are clocked in on the rising edge of CCLK. For write operations, the data is latched after a low-to-high transition of the 16th CCLK. The clock speed of CCLK is 5MHz(max).

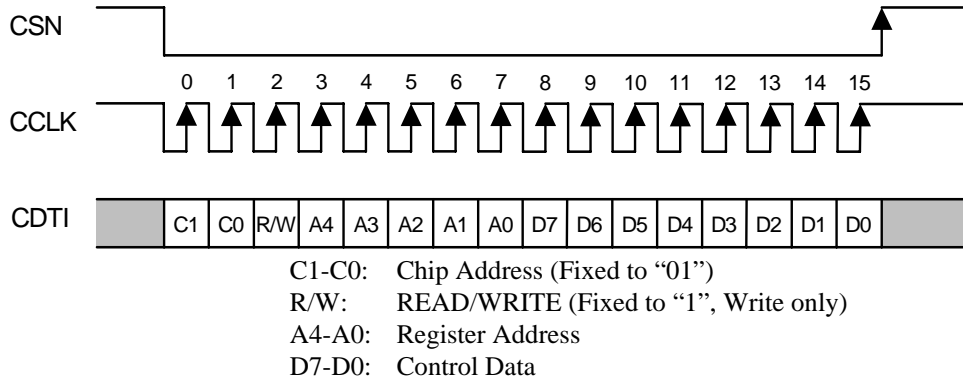


Figure 14. 3-wire Serial Control I/F Timing

■ Register Map

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Control 1	ACKS	0	0	DIF2	DIF1	DIF0	PW	RSTN
01H	Control 2	0	0	SLOW	DFS1	DFS0	DEM1	DEM0	SMUTE
02H	Control 3	RRST	0	0	INVL	INVR	0	0	0
03H	Lch ATT	ATT7	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0
04H	Rch ATT	ATT7	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0

Notes:

Do not write any data to the register over 05H directly.

Writing "1" to D7 and D6 of Addr01H and D2 of Addr02H is ignored.

The bits defined as 0 must contain a "0" value.

When RSTN bit goes "0", the only internal timing is reset and the registers are not initialized to their default values. All data can be written to the register even if PW or RSTN bit is "0".

Do not write the registers within 50msec after the power supplies are fed.

■ Register Definitions

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Control 1	ACKS	0	0	DIF2	DIF1	DIF0	PW	RSTN
	default	1	0	0	0	1	0	1	1

RSTN: Internal timing reset control

0: Reset. All registers are not initialized.

1: Normal Operation

The click noise, which occurs when MCLK frequency or DFS is changed, can be reduced by RSTN bit.

PW: Power down control

0: Power down. All registers are not initialized.

1: Normal Operation

DIF2-0: Audio data interface formats ([Table 6](#))

Initial: "010", Mode 2

ACKS: Master Clock Frequency Auto Setting Mode Enable

0: Disable, Manual Setting Mode

1: Enable, Auto Setting Mode

Master clock frequency is detected automatically at ACKS bit "1". In this case, the settings of DFS1-0 are ignored. When this bit is "0", DFS1-0 set the sampling speed mode.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
01H	Control 2	0	0	SLOW	DFS1	DFS0	DEM1	DEM0	SMUTE
	default	0	0	0	0	0	0	1	0

SMUTE: Soft Mute Enable

0: Normal operation

1: DAC outputs soft muted

DEM1-0: De-emphasis Response ([Table 7](#))

Initial: "01", OFF

DFS1-0: Sampling speed control

00: Normal Speed Mode

01: Double Speed Mode

10: Quad Speed Mode

When changing between Normal/Double Speed Mode and Quad Speed Mode, some click noise occurs.

SLOW: Slow Roll-off Filter Enable

0: Sharp Roll-off Filter

1: Slow Roll-off Filter

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
02H	Control 3	RRST	0	0	INVL	INVR	0	0	0
	default	0	0	0	0	0	0	0	0

INVR: Inverting Lch Output Polarity

0: Normal Output

1: Inverted Output

INVL: Inverting Rch Output Polarity

0: Normal Output

1: Inverted Output

RRST: Register Reset

0: Normal Operation

1: Register Reset (except RRST bit)

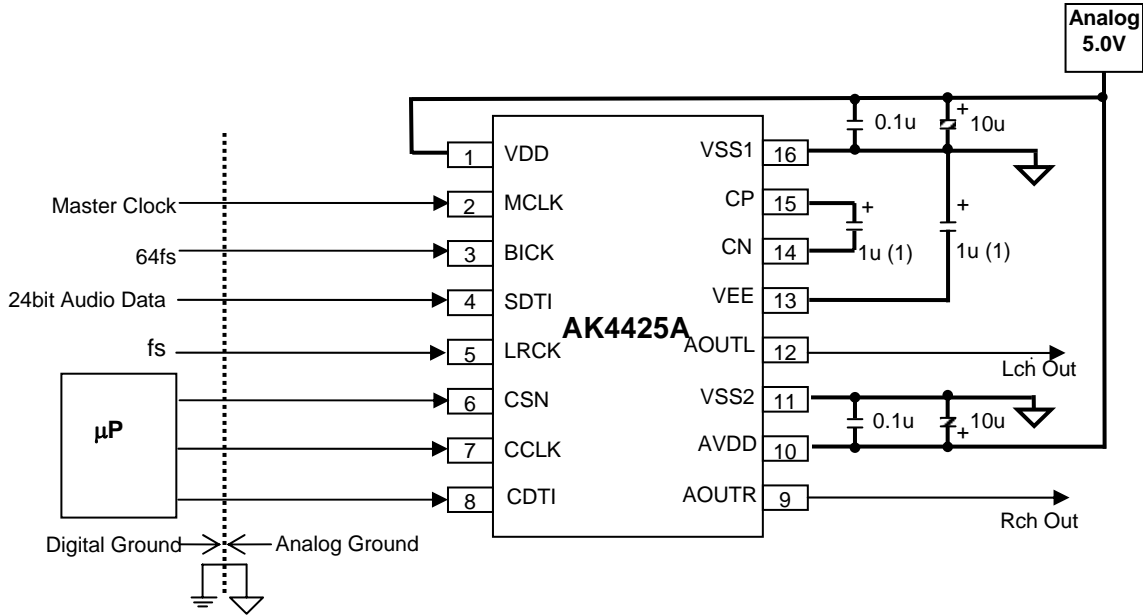
Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
03H	Lch ATT	ATT7	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0
04H	Rch ATT	ATT7	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0
	default	1	1	1	1	1	1	1	1

$ATT = 20 \log_{10} (ATT_DATA / 255)$ [dB]

00H: Mute

SYSTEM DESIGN

Figure 15 shows the system connection diagram. An evaluation board (AKD4425) is available for fast evaluation as well as suggestions for peripheral circuitry.



Note:

- Use low ESR (Equivalent Series Resistance) capacitors. When using polarized capacitors, the positive polarity pin should be connected to the CP and VSS1 pin.
- VSS1 and VSS2 should be separated from digital system ground.
- Digital input pins should not be allowed to float.

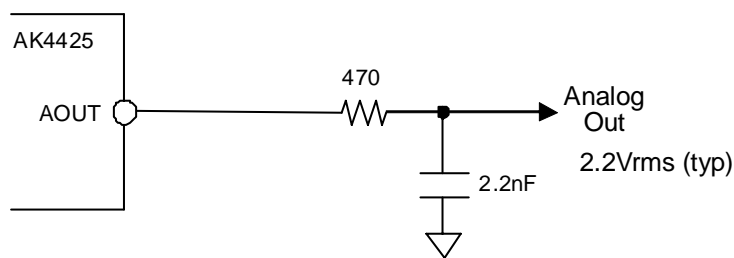
Figure 15. Typical Connection Diagram

1. Grounding and Power Supply Decoupling

VDD and AVDD are supplied from the analog supply and should be separated from the system digital supply. Decoupling capacitors, especially 0.1 μ F ceramic capacitors for high frequency bypass, should be placed as near to VDD and AVDD as possible. The VSS1 and VSS2 must be connected to the same analog ground plane. **Power-up sequence between VDD and AVDD is not critical.**

2. Analog Outputs

The analog outputs are single-ended and centered around the VSS (ground) voltage. The output signal range is typically 2.2V_{rms} (typ @ AVDD=5V). The internal switched-capacitor filter (SCF) and continuous-time filter (CTF) attenuate the noise generated by the delta-sigma modulator beyond the audio passband. Using single a 1st-order LPF (Figure 16) can reduce noise beyond the audio passband.

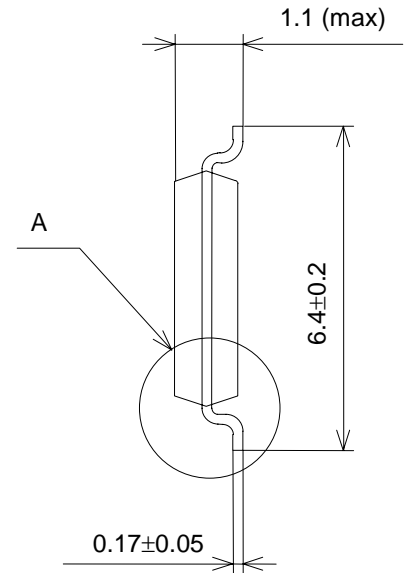
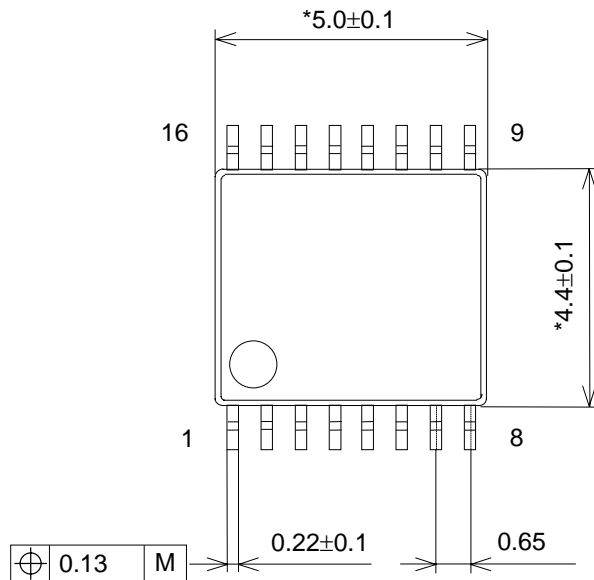


($f_c = 154\text{kHz}$, gain = -0.28dB @ 40kHz, gain = -1.04dB @ 80kHz)

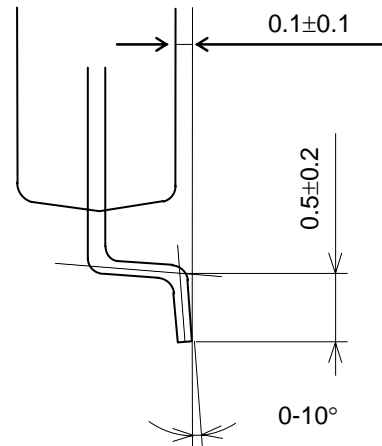
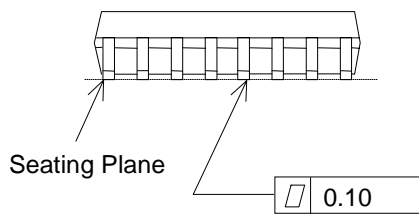
Figure 16. External 1st order LPF Circuit Example

PACKAGE

16pin TSSOP (Unit: mm)



Detail A

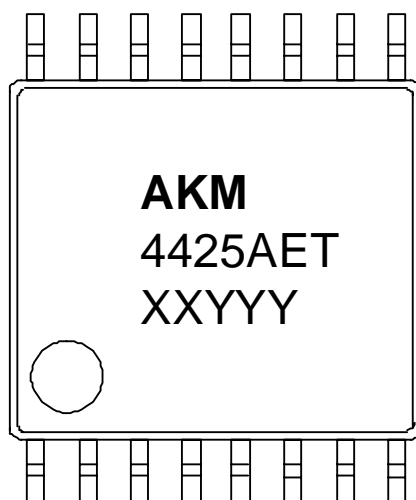


NOTE: Dimension "*" does not include mold flash.

■ Package & Lead frame material

Package molding compound:	Epoxy, Halogen (bromine and chlorine) free
Lead frame material:	Cu
Lead frame surface treatment:	Solder (Pb free) plate

MARKING



- 1) Pin #1 indication
- 2) Date Code : XXYYY (5 digits)
 XX: Lot#
 YYY: Date Code
- 3) Marketing Code : 4425AET
- 4) Asahi Kasei Logo

REVISION HISTORY

Date (YY/MM/DD)	Revision	Reason	Page	Contents
09/09/18	00	First Edition		
11/03/01	01	Error Correction	24	1. Grounding and Power Supply Decoupling The description was changed.

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