D A T A B O O K

Version 1.0
September, 2003

INIC-1622

PCI to Serial ATA
Host Adapter IC

initio

Revision Notes
for INIC-1622 Data Book: P/N 1622X-DS Rev 1.0, 9/24/03

Revision History

Doc Rev 1.0 (P/N 1622X-DS) 09/24/03 (current release)

Technical Information Changes in this Data Book Release

The table below lists technical information that has changed from the *INIC-1622 Data Book* revision **X.0** to the *INIC-1622 Data Book* revision **1.0**. All changes are identified in the manual by change bars in the left-hand column (superficial or non-technical edits are not indicated).

Section Updated	Pages Affected	Change Description
all	all	Initial release.

INIC-1622 Features

PCI 32 bit/66 MHz Interface

- PCI 2.3 compliant interface.
- Burst transfer rate of 264 Mb/s.
- Built in hardware bus master engine.

ATA Interface

- Serial ATA Revision1.0.
- Serial ATA transfer rate of 1.5 Gb/s.
- Supports two SATA channels.

Memory Interface

- Support for 512K FLASH and Serial E^2PROM.

Data FIFO

- 256 Byte data FIFO for each channel.

On Board PCI Bus Master Engine

- On board Bus Master Engine relieve the system processor from book keeping and enhance performance.

Uses Initio's Proprietary Host Adapter Mode of Operation

- Initio Proprietary AutoDMA mode (IDMA)
- Queued/Overlapping ATA Commands Support

Other Features

- Disk RAID 0/1 support.
- SATA hot plug/unplug hardware support.
- Implements Power Management
- Full driver support for all Major Operating Systems.
- BIOS supports DOS and Windows applications without driver involvement.
- Supports Plug and Play allowing users to change configurations without the use of jumpers.

Table of Contents

SECTION 1
Overview

1.1 Introduction

The INIC-1622 provides advanced Host Adapter features in a single 128 pin TQFP package with 2 Serial ATA and a 32 bit/66 MHz PCI 2.3 compliant interface. The third memory interface allows access to FLASH and Serial E^2PROM devices. The Flash interface provides Read/Write access to the attached BIOS. The Serial E^2PROM interface provides Read/Write access to the attached Serial E^2PROM for bus configuration information.

1.1.1 Feature Summary

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- Full driver support for all Major Operating Systems.
- BIOS supports DOS and Windows applications without driver involvement.
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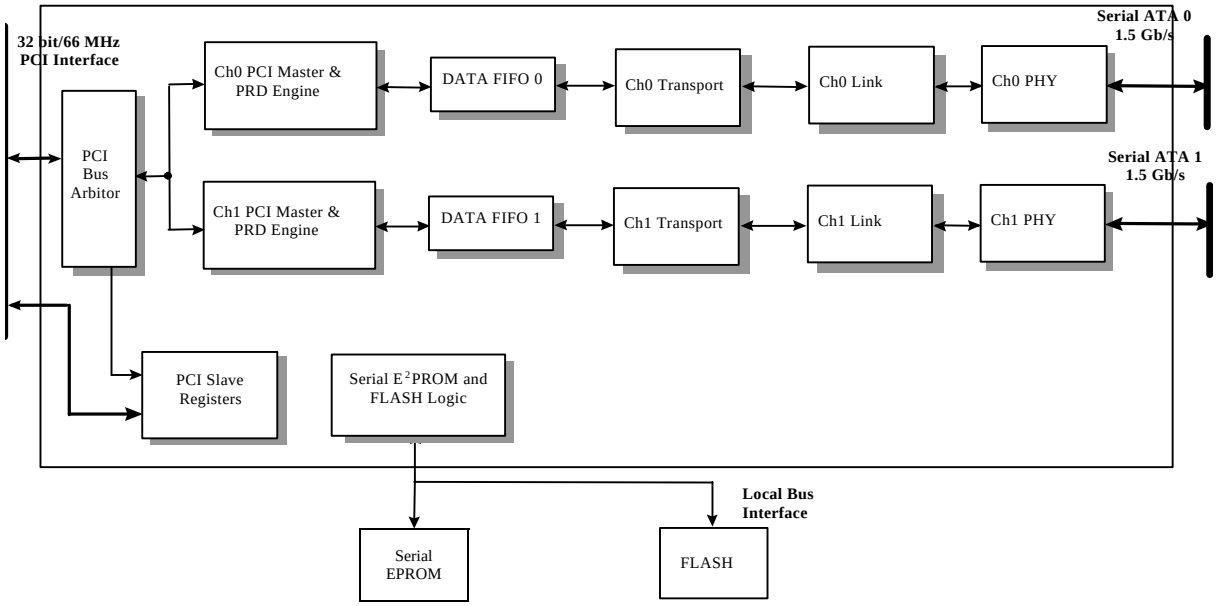

Figure 1-1 INIC-1622 Block Diagram

1.1.2 Reference Documents

- Peripheral Component Interconnect (PCI) Local Bus Interface Specification, Rev. 2.3
- Serial ATA Specification, Revision 1.0
- Serial ATA II: Extension to Serial ATA 1.0 Rev. 1.0

Figure 2-1 shows the pinout of the INIC-1622.

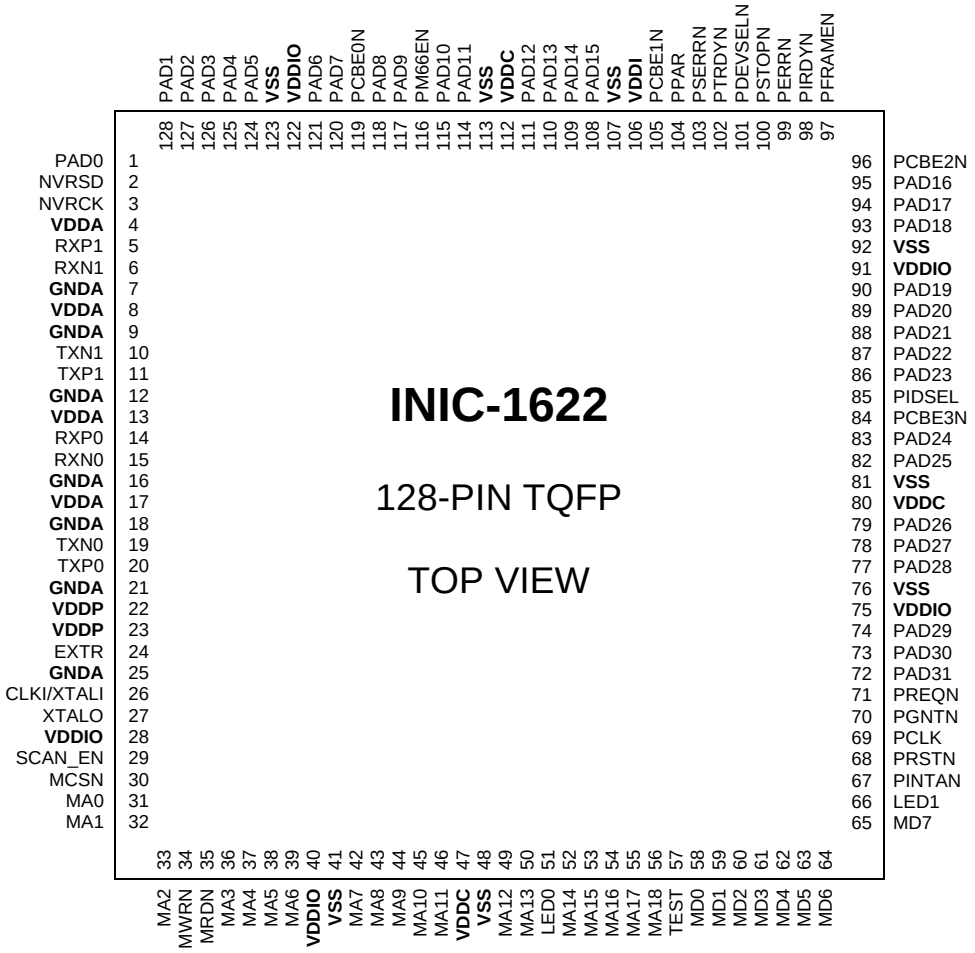

Figure 2-1 INIC-1622 TQFP Pin Assignments

2.1 PCI Interface Pins

Table 2-1 PCI Interface Pins

SYMBOL	TQFP PIN #	TYPE	DESCRIPTION
PAD[31:00]	72-74,77-79,82-83,86-90, 93-95,108-111,114-115, 117-118,120-121,124-128,1	i/o, t/s	PCI Address and Data Bus
PCBEN[3:0]	84,96,105,119	i/o, t/s	Bus Command and Byte enables
PPAR	104	i/o, t/s	Even Parity
PFRAMEN	97	i/o, s/t/s	Cycle Frame
PTRDYN	102	i/o, s/t/s	Target Ready
PIRDYN	98	i/o, s/t/s	Initiator Ready
PIDSEL	85	i	Initialization Device Select
PDEVSELN	101	i/o, s/t/s	Device Select
PSTOPN	100	i/o, s/t/s	Stop current transaction
PREQN	71	o	Bus Request
PGNTN	70	i	Bus Grant
PINTAN	67	o/d	Interrupt A
PERRN	99	i/o, s/t/s	Parity Error
PSERRN	103	o/d	System Error
PCLK	69	i	PCI Clock
PRSTN	68	i	PCI Reset
PM66EN	116	i	PCI 66 MHz Enable

2.1.1 Non Supported PCI-32 Pin Signals

IRQB# TCK
IRQC# TDI
IRQD# TDO
LOCK# TMS
SBO# TRST#
SDONE#

2.2 Memory Interface Pins

Table 2-2 Memory Interface Pins

SYMBOL	TQFP PIN #	TYPE	DESCRIPTION
MA[18:0]	56-52,50,49,46-42,39-36, 33-31	i/o	Memory Address Bus
MD[7:0]	65-58	i/o, t/s	Memory Data Bus
MWRN	34	o	Memory Write Strobe
MRDN	35	o	Memory Read Strobe
MCSN	30	o	BIOS Flash/Eprom Chip Select
NVRCK	3	o	NVRAM serial clock
NVRSD	2	i/o	NVRAM serial data
TEST	57	i	Test Control

2.3 SATA Interface Pins

Table 2-3 SATA Interface Pins

SYMBOL	TQFP PIN #	TYPE	DESCRIPTION
TXP0	20	o	Channel 0 Differential Transmit positive signal line
TXN0	19	o	Channel 0 Differential Transmit negative signal line
RXP0	14	i	Channel 0 Differential Receive negative signal line
RXN0	15	i	Channel 0 Differential Receive negative signal line
TXP1	11	o	Channel 1 Differential Transmit positive signal line
TXN1	10	o	Channel 1 Differential Transmit negative signal line
RXP1	5	i	Channel 1 Differential Receive negative signal line
RXN1	6	i	Channel 1 Differential Receive negative signal line
CLKI/XTALI	26	i	External Clock Input or Crystal Oscillator Output
XTALO	27	o	Crystal Oscillator Output
EXTR	24	i	External Reference Resister
LED0	51	o	Channel 0 activity LED
LED1	66	o	Channel 1 activity LED

2.4 Hardware Configuration Pins

The following signal pins are used during system reset (PRSTN) to select system specific function modes.

Table 2-4 Hardware Configuration Pins

SYMBOL	TQFP PIN #	DESCRIPTION	FUNCTION
MD0	68	Reserved	Reserved
MD1	69	Reserved	Reserved
MD2	70	NVRAM Load Default	Pulldown = load vendor specific configuration space values Pullup = configuration space uses on chip default value
MD3	71	Fast back-to-back Enable	Pulldown = Fast back-to-back disable Pullup = Fast back-to-back enable
MD4	74	PCI 66 MHz Enable	Pulldown = 66 MHz PCI disable Pullup = 66 MHz PCI enable
MD[6:5]	76-75	Reference Clock Select	00 = 100 MHz 01 = 25MHz 10 = 150MHz 11 = 75MHz (default)
MD7	77	Reserved	Reserved

2.5 Power and Ground Pins

Table 2-5 Power and Ground Pins

SYMBOL	TQFP PIN #	TYPE	DESCRIPTION
GNDA	7,9,12,16,18,21,25	gnd	Analog Ground
VSS	41,48,76,81,92,107,113,123	gnd	Digital Ground
VDDA (1.8 V)	4,8,13,17	pwr	Power Supply to Analog I/O’s
VDDC (1.8V)	47,80,112,	pwr	Power Supply for Core
VDDIO (3.3V)	28,40,75,91,106,122	pwr	Power Supply for I/O Drivers
VDDP	22,23	pwr	Power Supply for PLL

3.1 Configuration Spaces Address Map

The Configuration Space is a contiguous block of 256 bytes accessible from the PCI Bus. For PCI accesses to the Configuration space, one of AD[31:11] is connected to pin PIDSEL and AD[10:8] = 000b. The lower 64 bytes of the Configuration Space is the predefined header. The next 32 bytes are INIC-1622 specific.

31 24	**23 16**	**15 08**	**07 00**	
Device ID		Vendor ID		00h
Status		Command		04h
Base Class	Sub Class	Prog. Interface	Revision ID	08h
BIST (NS)	Header Type	Latency Timer	Cache Line Size	0Ch
Base Address 0 (ATA Command-Block Registers for Channel 0)				10h
Base Address 1 (ATA Control-Block Registers for Channel 0)				14h
Base Address 2 (ATA Command-Block Registers for Channel 1)				18h
Base Address 3 (ATA Control-Block Registers for Channel 1)				1Ch
Base Address 4 (ATA Bus Master I/O Registers)				20h
Base Address 5 (ATA Bus Master Memory Mapped Registers)				24h
Reserved				28h
Subsystem ID		Subsystem Vendor ID		2Ch
Expansion ROM Base Address				30h
Reserved			Capabilities Pointer	34h
Reserved				38h
Max_Lat	Min_Gnt	Interrupt Pin	Interrupt Line	3Ch
Reserved addresses 40h through D8h.				40-D8h
Power Management Capabilities		Next Item Pointer	Capabilities ID	DCh
PM Data	PM Bridge Support	Power Management Control/Status		E0h
Manufacture's ID				F8h

Note : (NS) indicates Not Supported.

3.2 ATA Shadow Registers

These registers are accessible through I/O Space only.

3.2.1 Command-Block Register

Command-Block Register for all except the PACKET and SERVICE commands are accessible through I/O base0 for channel 0 and base2 for channel 1.

31 24	23 16	15 08	07 00	
Sector Number	Sector Count	Error/Features	Data Port	00h
Status/Command	Device/Head	Cylinder High	Cylinder Low	04h

3.2.2 Control-Block Register

Control-Block Register for all except the PACKET and SERVICE commands are accessible through I/O base1 for channel 0 and base3 for channel 1.

31 24	23 16	15 08	07 00	
				00h
	Alt. Status/Control			04h

3.2.3 Register for the PACKET and SERVICE Commands

PACKET and SERVICE commands are accessible through I/O base0 for channel 0 and base2 for channel 1.

31 24	23 16	15 08	07 00	
-	-	Error/Features	Data Port	00h
Status/Command	Device Select	Byte Count High	Byte Count Low	04h

3.3 I/O & Memory Mapped Registers Address Map

3.3.1 Page 0 Registers

These registers are accessible through both I/O base4 and Memory Base.

31 24	23 16	15 08	07 00	
LBA Low 0	Sector Cnt 0	Err/Features 0	PIO Data 0	00h
Stat/Cmd 0	Dev/Head 0	LBA High 0	LBA Mid 0	04h
PRD Control 0	Intr. Mask 0	Intr. Stat 0	Alt Stat/Ctrl 0	08h
PRD Address 0				0Ch
PRD Total Transfer Length 0				10h
IDMA Status 0		IDMA Control 0		14h
CPB Lookup Table Address 0				18h
Reply FF Count 0	Reply FF Queue 0	Post FF Count 0	Post FF Queue 0	1Ch
SStatus 0				20h
SError 0				24h
SControl 0				28h
SActive 0				2Ch
				30h
				34h
Scratch				38h
ROM Data Port	ROM Addr 2	ROM Addr 1	ROM Addr 0	3Ch
LBA Low 1	Sector Cnt 1	Err/Features 1	PIO Data 1	40h
Stat/Cmd 1	Dev/Head 1	LBA High 1	LBA Mid 1	44h
PRD Control 1	Intr. Mask 1	Intr. Stat 1	Alt Stat/Ctrl 0	48h
PRD Address 1				4Ch
PRD Total Transfer Length 1				50h
IDMA Status 1		IDMA Control 1		54h
CPB Lookup Table Address 1				58h
Reply FF Count 1	Reply FF Queue 1	Post FF Count 1	Post FF Queue 1	5Ch
SStatus 1				60h
SError 1				64h
SControl 1				68h
SActive 1				6Ch
-	-	-		70h
				74h
Scratch				78h
Global Status		Global Control		7Ch
Reserved				80-BBh
Global Interrupt Mask		Global Interrupt Status		BCh
Reserved				C0-FBh
Reserved	NVRAM Port	*Reserved*	*Reserved*	FCh

3.3.2 Page 1 Registers

These registers are accessible through both I/O base4 and Memory Base.

31 24	23 16	15 08	07 00	
TP_DEBUG0				00h
LK_DEBUG0				04h
DCXA0				08h
Reserved				0Ch
DCXC0				10h
Reserved		FFLAG0		14h
FPDMA_SM_CS0	APRD_SM_CS0	IDMA_SM_CS0		18h
Reserved				1Ch
PHY_DEBUG0				20h
Reserved				24-37h
PHY_CTL0				38h
SSPLL Feedback Div.		SSPLL Input Div.		3Ch
TP_DEBUG1				40h
LK_DEBUG1				44h
DCXA1				48h
Reserved				4Ch
DCXC1				50h
Reserved		FFLAG1		54h
FPDMA_SM_CS1	APRD_SM_CS1	IDMA_SM_CS1		58h
Reserved				5Ch
PHY_DEBUG1				60h
Reserved				64-77h
PHY_CTL1				78h
Global Status		Global Control		7Ch
Reserved				84-BBh
Reserved		SSPLL PLL Loop	SSPLL Modulation Ctrl.	BCh
Reserved				C0-FFh

3.4 Command Parameter Blocks (CPB) Structure Definition

The Command Parameter Blocks (CPB) structure definition is shown in the table below.

31 24	23 16	15 08	07 00	
Control Flags	ATA Status	ATA Error	Response Flags	00h
S S S S S S S S	Total Transfer Length			04h
First PRD pointer (Qword aligned)				08h
Reserved				0Ch
Mirror Control	ATA Device/Head	ATA Ex. Feature	ATA Feature	10h
ATA Ex. Sector Number	ATA Sector Number	ATA Ex. Sector Count	ATA Sector Count	14h
ATA Ex. Cylinder High	ATA Cylinder High	ATA Ex. Cylinder Low	ATA Cylinder Low	18h
Slave ATA Status	Slave ATA Error	ATA Control	ATA Command	20h

3.5 Physical Region Descriptor (PRD) Structure Definition

This register reflects the current physical pointer to a PRD list in the system memory. The descriptor table should be aligned on a Dword boundary and cannot cross a 65,536 boundary in memory.

31 24	23 16	15 08	07 00	
Physical Memory Address				00h
Control Flags	Reserved	Transfer Length		04h

3.6 Summary of Supported PCI Commands

CBE[3:0]	Command	Master / Slave Mode
0000	Interrupt Acknowledge	-
0001	Special Cycle	-
0010	I/O Read	Slave
0011	I/O Write	Slave
0100	*Reserved*	-
0101	*Reserved*	-
0110	Memory Read	Master/ Slave
0111	Memory Write	Master/ Slave
1000	*Reserved*	-
1001	*Reserved*	-
1010	Configuration Read	Slave
1011	Configuration Write	Slave
1100	Memory Read Multiple	Master
1101	Dual Address Cycle	Master
1110	Memory Read Line	Master
1111	Memory Write and Invalidate	Master

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4.1 Configuration Space Register Descriptions

These registers can be read from or written to from the PCI interface when IDSEL is asserted, AD[1:0] = 00b, AD[10:8] = 000b and the PCI command indicated on CBE[3:0]# = 1010b or 1011b.

00h Vendor ID (PVID[1:0])

This register identifies “INITIO” as the Vendor of this device. It will always read “1101h”.

The contents of these registers can be modified just after a power on reset. The new contents of this register will be fetched by on chip hardware from the external NVRAM. For more details, please see bit LDDFLT in register GSTAT.

PVID1		PVID0	
15	VID15 = 0	07	VID07 = 0
14	VID14 = 0	06	VID06 = 0
13	VID13 = 0	05	VID05 = 0
12	VID12 = 1	04	VID04 = 0
11	VID11 = 0	03	VID03 = 0
10	VID10 = 0	02	VID02 = 0
09	VID09 = 0	01	VID01 = 0
08	VID08 = 1	00	VID00 = 1

Bit(s)	rw	reset	Acronym	Definition
15:0	r	1101h	(VID15-0)	Always reads 1101h.

02h Device ID (PDID[1:0])

This register indicates the Device Identification number. The Device Identification number for this device is “1622h”.

The contents of these registers can be modified just after a power on reset. The new contents of this register will be fetched by on chip hardware from the external NVRAM. For more details, please see bit LDDFLT in register GSTAT.

PDID1		PDID0	
31	DID15 = 0	23	DID07 = 0
30	DID14 = 0	22	DID06 = 0
29	DID13 = 0	21	DID05 = 1
28	DID12 = 1	20	DID04 = 0
27	DID11 = 0	19	DID03 = 0
26	DID10 = 1	18	DID02 = 0
25	DID09 = 1	17	DID01 = 1
24	DID08 = 0	16	DID00 = 0

Bit(s)	rw	reset	Acronym	Definition
31:16	r	1622h	(DID15-0)	Always reads 1622h.

04h Command (PCMD[1:0])

The command register provides coarse control over INIC-1622's ability to generate and respond to PCI cycles. When a "00h" is written to this register, the INIC-1622 is logically disconnected from the PCI bus for all accesses except Configuration cycles.

PCMD1		PCMD0	
15	RSVD	07	WCTLEN = 0
14	RSVD	06	PERESEN
13	RSVD	05	VGAEN = 0
12	RSVD	04	MWRIEN
11	RSVD	03	SPECYC = 0
10	INTEN	02	BUSMEN
09	FBTBEN = 0	01	MSPAEN
08	SERREN	00	ISPAEN

Bit(s)	rw	reset	Acronym	Definition
15-11	rw	0	(RSVD)	Always reads 0.
10	rw	0	(INTEN)	INTERRUPT ENABLE: This bit enables the generation of INTx signal whenever there is an interrupt pending.
09	rw	0	(FBTBEN)	MASTER FAST BACK-TO-BACK: This feature is not supported. Always reads 0.
08	rw	0	(SERREN)	SERR# ENABLE: When set will enable the SERR# signal to be asserted when an address parity error is detected on the AD, CBE#, PAR, and PAR64 signal lines during the address phase. When reset, the SERR# signal will not be driven if these above conditions occur.
07	rw	0	(WCTLEN)	WAIT CONTROL ENABLE: This feature is not supported. Always reads 0.
06	rw	0	(PERESEN)	PERR# ENABLE: When set will enable the PERR# signal to be asserted when a data parity error is detected on the AD, CBE#, PAR, and PAR64 signal lines during the address phase and will set the Data Parity Error detected bit in STATUS1 register in the Configuration Space. When reset the Data Parity Error detected bit is set in STATUS1 register in the Configuration Space, if a parity error is detected during the address phase, but the PERR# signal is not asserted.
05	rw	0	(VGAEN)	VGA SNOOP ENABLE: This feature is not supported. Always reads 0.
04	rw	0	(MWRIEN)	MEMORY WRITE AND INVALIDATE COMMAND ENABLE: When set will enable the device to issue Memory Write and Invalidate commands. When reset the device will issue Memory Write Commands.
03	rw	0	(SPECYC)	SPECIAL CYCLE ENABLE: This feature is not supported. Always reads 0.
02	rw	0	(BUSMEN)	BUS MASTER ENABLE: When set, this bit enables the bus master function of the host adapter. When reset, it disables the host from generating any PCI requests.
01	rw	0	(MSPAEN)	MEMORY SPACE ENABLE: When set, enables the device to respond to memory space transactions. When reset, disables the devices ability to respond to memory space transactions.
00	rw	0	(ISPAEN)	I/O SPACE ENABLE: When set, enables the device to respond to I/O space transactions. When reset, disables the devices ability to respond to I/O space transactions.

06h Status (PSTUS[1:0])

The status register is used to record status information for PCI bus related events. To reset any writeable bit, write that bit value with a 1.

PSTUS1		PSTUS0	
31	DPERR	23	FBTBC
30	SSERR	22	RSVD
29	RMABT	21	M66C
28	RTABT	20	CAPLST
27	STABT	19	INTSTAT
26	DEVSEL01 = 0	18	RSVD
25	DEVSEL00 = 1	17	RSVD
24	DPERD	16	RSVD

Bit(s)	rw	reset	Acronym	Definition
31	rw	0	(DPERR)	DETECTED PARITY ERROR STATUS: When set, it indicates that the device detected a 36 bit parity error during the address phase or write data phase as a target, or a parity error during a read data phase as a master.
30	rw	0	(SSERR)	SIGNALED SYSTEM ERROR STATUS: When set, it indicates that the device generated a system error on the SERR# line.
29	rw	0	(RMABT)	RECEIVED MASTER ABORT STATUS: When set it indicates that the device as a bus master received a Master Abort.
28	rw	0	(TRABT)	RECEIVED TARGET ABORT STATUS: When set, it indicates that the device as a bus master received a Target Abort.
27	rw	0	(STABT)	SIGNALED TARGET ABORT STATUS: When set, it indicates to the master that the device as a target is unable to respond due to some fatal condition.
26-25	rw	01	(DEVSEL[01:00])	DEVICE SELECT TIMING STATUS: Device asserts DEVSEL# signal in the medium timing mode for any bus command, i.e., two clocks after FRAME# is asserted.
24	rw	0	(DPERD)	MASTER DATA PARITY ERROR DETECTED: When set, this bit indicates that the device as a Bus Master either observed PERR# asserted, or the Bus Master asserted PERR# and the Parity Error Response bit was enabled in the Command Register in the Configuration Space.
23	rw	0	(FBTBC)	FAST BACK TO BACK STATUS: The device as a target is not capable of fast back to back transactions. With the configuration bit MD3, FBTBC can be enabled or disabled.
22	rw	0	*reserved*	RESERVED. Always reads 0.
21	rw	0	(M66C)	66MHZ CAPABLE STATUS: The device is incapable of running at 66Mhz. With the configuration bit MD4, M66C can be enabled or disabled.
20	rw	1	(CAPLST)	CAPABILITIES LIST: Indicates if the device implements the pointer for a New capabilities link list at offset 34h. Always reads 1.
19	rw	0	(INTSTAT)	INTERRUPT STATUS: Indicates that an interrupt is pending.
18-16	rw	0	*reserved*	RESERVED. Always reads 0.

08h Device Revision ID (PRID)

This register identifies the revision level of the device. It indicates different steppings of the device. For the first step of this device it will read as a 01h. Subsequent steps of the device reflect an increment of 1.

PRID	
07	RID07
06	RID06
05	RID05
04	RID04
03	RID03
02	RID02
01	RID01
00	RID00

Bit(s)	rw	reset	Acronym	Definition
07-00	r	01h	(RID[07:00])	REVISION ID: Indicates the device step number. Every subsequent revision step reflects an increment by 1 with respect to the previous revision step number.

09h Programming Interface (PPI)

This register identifies the Programming Interface the device supports. For IDMA mode, it always reads 00h.

Note: The contents of these registers can be modified just after a power on reset. The new contents of this register will be fetched by on chip hardware from the external NVRAM. For more details, please see bit LDDFLT in register GSTAT.

PRID	
15	PI07 = 0
14	PI06 = 0
13	PI05 = 0
12	PI04 = 0
11	PI03 = 0
10	PI02 = 0
09	PI01 = 0
08	PI00 = 0

Bit(s)	rw	reset	Acronym	Definition
15-08	r	00h	(PI[07:00])	PROGRAMMING INTERFACE

0Ah Sub Class (PSC)

This register identifies the device as a Serial ATA type device. It always reads 06h.

Note: The contents of these registers can be modified just after a power on reset. The new contents of this register will be fetched by on chip hardware from the external NVRAM. For more details, please see bit LDDFLT in register GSTAT.

SC	
23	SC07 = 0
22	SC06 = 0
21	SC05 = 0
20	SC04 = 0
19	SC03 = 0
18	SC02 = 1
17	SC01 = 1
16	SC00 = 0

Bit(s)	rw	reset	Acronym	Definition
23-16	r	06h	(SC[07:00])	SUB CLASS: This register defines the Sub Class of the device. The default value of this register is “06h” meaning Serial ATA device.

0Bh Base Class (PBC)

This register identifies the device as a Mass Storage Controller. It always reads 01h.

Note: The contents of these registers can be modified just after a power on reset. The new contents of this register will be fetched by on chip hardware from the external NVRAM. For more details, please see bit LDDFLT in register GSTAT.

SC	
31	BC07 = 0
30	BC06 = 0
29	BC05 = 0
28	BC04 = 0
27	BC03 = 0
26	BC02 = 0
25	BC01 = 0
24	BC00 = 1

Bit(s)	rw	reset	Acronym	Definition
31-24	r	01h	(BC[07:00])	BASE CLASS: This register defines the Base Class of the device. It always reads “01h” indicating that the device is a Mass Storage Controller.

0Ch Cache Line Size (PCLS)

This register specifies the system Cache Line Size in 32-bit words only if the Memory Write and Invalidate enable bit is set to a 1 in the Command register. In this case the device will issue either Memory Write and Invalidate, Memory Read Line or Memory Read Multiple Commands. If this bit is reset then the device will issue either Memory Write or Memory Read Commands. The device uses the value stored in the Cache Line Size register to determine when to issue Cache commands at Cache Line boundries.

PCLS	
07	CLS07
06	CLS06
05	CLS05
04	CLS04
03	CLS03
02	CLS02
01	CLS01
00	CLS00

Bit(s)	rw	reset	Acronym	Definition
07-00	rw	01h	(CLS[07:00])	CACHE LINE SIZE: The value stored in the Cache Line Register determines when the INIC-1622 issues Cache Line referenced commands based on the number of data bytes stored in the Data Fifo internal to the chip.

0Dh Latency Timer (PLT)

This register specifies the Master Latency Timer value for a PCI Master when the device is on the PCI bus. The least three significant bits are hard wired to 0, resulting in a PCLK granularity of 8 PCLK's.

PLT	
15	LT07
14	LT06
13	LT05
12	LT04
11	LT03
10	LT02 = 0
09	LT01 = 0
08	LT00 = 0

Bit(s)	rw	reset	Acronym	Definition
15-11	rw	0	(LT[07:03])	LATENCY TIMER [07:03]: Indicates the Bus Master latency period in PCLK time units.
10-08	r	0	(LT[02:00])	LATENCY TIMER [02:00]: These 3 bits always read 0, setting the granularity to 8 PCLK's.

0Eh Header Type (PHDT)

This register identifies the layout of bytes beginning at offset 10h in the PCI configuration space. In addition, this register specifies whether the device is a single or multi function device.

PHDT	
23	MFDEV = 0
22	HDT06 = 0
21	HDT05 = 0
20	HDT04 = 0
19	HDT03 = 0
18	HDT02 = 0
17	HDT01 = 0
16	HDT00 = 0

Bit(s)	rw	reset	Acronym	Definition
23	r	0	(MFDEV)	MULTI FUNCTION STATUS: This device is a single function device. It always reads 0.
22-16	r	0	(HDT[06:00])	HEADER TYPE [06:00]: These 5 bits always read 0, to indicate the layout of bytes 10h-3Fh in the configuration space.

0Fh Built In Self Test (BIST)

This register is used to control the invocation of a PCI device's BIST and to report the status of BIST. This device does not support BIST and always reads 0.

PBIST	
31	BIST07 = 0
30	BIST06 = 0
29	BIST05 = 0
28	BIST04 = 0
27	BIST03 = 0
26	BIST02 = 0
25	BIST01 = 0
24	BIST00 = 0

Bit(s)	rw	reset	Acronym	Definition
31-24	r	0	(BIST[31:24])	BUILT IN SELF TEST: This device does not support BIST. It always reads 0.

10h Base Address 0 (PBASE0)

This register allows a PCI devices's I/O functions to be dynamically mapped into a system's I/O address space.

PBASE0							
31	BAIO31	23	BAIO23	15	BAIO15	07	BAIO07 = 0
30	BAIO30	22	BAIO22	14	BAIO14	06	BAIO06 = 0
29	BAIO29	21	BAIO21	13	BAIO13	05	BAIO05 = 0
28	BAIO28	20	BAIO20	12	BAIO12	04	BAIO04 = 0
27	BAIO27	19	BAIO19	11	BAIO11	03	BAIO03 = 0
26	BAIO26	18	BAIO18	10	BAIO10	02	BAIO02 = 0
25	BAIO25	17	BAIO17	09	BAIO09	01	RSVD = 0
24	BAIO24	16	BAIO16	08	BAIO08	00	IOSPIND = 1

Bit(s)	rw	reset	Acronym	Definition
31-08	rw	00h	(BAIO[31:08])	I/O BASE ADDRESS [31:08]: These are read/write bits allowing the system to access channel 0 Command Block Registers.
07-02	r	00h	(BAIO[07:02])	RESERVED: These bits always read 0.
01	r	0	*reserved*	RESERVED: This bit always reads 0.
00	r	1	(IOSPIND)	I/O ADDRESS SPACE INDICATOR: This bit always reads 1 indicating that the device's base address register is requesting I/O space.

14h Base Address 1 (PBASE1)

This register allows a PCI devices's I/O functions to be dynamically mapped into a system's I/O address space.

PBASE1							
31	BAIO31	23	BAIO23	15	BAIO15	07	BAIO07 = 0
30	BAIO30	22	BAIO22	14	BAIO14	06	BAIO06 = 0
29	BAIO29	21	BAIO21	13	BAIO13	05	BAIO05 = 0
28	BAIO28	20	BAIO20	12	BAIO12	04	BAIO04 = 0
27	BAIO27	19	BAIO19	11	BAIO11	03	BAIO03 = 0
26	BAIO26	18	BAIO18	10	BAIO10	02	BAIO02 = 0
25	BAIO25	17	BAIO17	09	BAIO09	01	RSVD = 0
24	BAIO24	16	BAIO16	08	BAIO08	00	IOSPIND = 1

Bit(s)	rw	reset	Acronym	Definition
31-08	rw	00h	(BAIO[31:08])	I/O BASE ADDRESS [31:08]: These are read/write bits allowing the system to access channel 0 Control Block Registers.
07-02	r	00h	(BAIO[07:02])	RESERVED: These bits always read 0.
01	r	0	*reserved*	RESERVED: This bit always reads 0.
00	r	1	(IOSPIND)	I/O ADDRESS SPACE INDICATOR: This bit always reads 1 indicating that the device's base address register is requesting I/O space.

18h Base Address 2 (PBASE2)

This register allows a PCI devices's I/O functions to be dynamically mapped into a system's I/O address space.

PBASE2							
31	BAIO31	23	BAIO23	15	BAIO15	07	BAIO07 = 0
30	BAIO30	22	BAIO22	14	BAIO14	06	BAIO06 = 0
29	BAIO29	21	BAIO21	13	BAIO13	05	BAIO05 = 0
28	BAIO28	20	BAIO20	12	BAIO12	04	BAIO04 = 0
27	BAIO27	19	BAIO19	11	BAIO11	03	BAIO03 = 0
26	BAIO26	18	BAIO18	10	BAIO10	02	BAIO02 = 0
25	BAIO25	17	BAIO17	09	BAIO09	01	RSVD = 0
24	BAIO24	16	BAIO16	08	BAIO08	00	IOSPIND = 1

Bit(s)	rw	reset	Acronym	Definition
31-08	rw	00h	(BAIO[31:08])	I/O BASE ADDRESS [31:08]: These are read/write bits allowing the system to access channel 1 Command Block Registers.
07-02	r	00h	(BAIO[07:02])	RESERVED: These bits always read 0.
01	r	0	*reserved*	RESERVED: This bit always reads 0.
00	r	1	(IOSPIND)	I/O ADDRESS SPACE INDICATOR: This bit always reads 1 indicating that the device's base address register is requesting I/O space.

1Ch Base Address 3 (PBASE3)

This register allows a PCI devices's I/O functions to be dynamically mapped into a system's I/O address space.

PBASE3							
31	BAIO31	23	BAIO23	15	BAIO15	07	BAIO07 = 0
30	BAIO30	22	BAIO22	14	BAIO14	06	BAIO06 = 0
29	BAIO29	21	BAIO21	13	BAIO13	05	BAIO05 = 0
28	BAIO28	20	BAIO20	12	BAIO12	04	BAIO04 = 0
27	BAIO27	19	BAIO19	11	BAIO11	03	BAIO03 = 0
26	BAIO26	18	BAIO18	10	BAIO10	02	BAIO02 = 0
25	BAIO25	17	BAIO17	09	BAIO09	01	RSVD = 0
24	BAIO24	16	BAIO16	08	BAIO08	00	IOSPIND = 1

Bit(s)	rw	reset	Acronym	Definition
31-08	rw	00h	(BAIO[31:08])	I/O BASE ADDRESS [31:08]: These are read/write bits allowing the system to access channel 1 Control Block Registers.
07-02	r	00h	(BAIO[07:02])	RESERVED: These bits always read 0.
01	r	0	*reserved*	RESERVED: This bit always reads 0.
00	r	1	(IOSPIND)	I/O ADDRESS SPACE INDICATOR: This bit always reads 1 indicating that the device's base address register is requesting I/O space.

20h Base Address 4 (PBASE4)

This register allows a PCI devices's I/O functions to be dynamically mapped into a system's I/O address space.

PBASE4							
31	BAIO31	23	BAIO23	15	BAIO15	07	BAIO07 = 0
30	BAIO30	22	BAIO22	14	BAIO14	06	BAIO06 = 0
29	BAIO29	21	BAIO21	13	BAIO13	05	BAIO05 = 0
28	BAIO28	20	BAIO20	12	BAIO12	04	BAIO04 = 0
27	BAIO27	19	BAIO19	11	BAIO11	03	BAIO03 = 0
26	BAIO26	18	BAIO18	10	BAIO10	02	BAIO02 = 0
25	BAIO25	17	BAIO17	09	BAIO09	01	RSVD = 0
24	BAIO24	16	BAIO16	08	BAIO08	00	IOSPIND = 1

Bit(s)	rw	reset	Acronym	Definition
31-08	rw	00h	(BAIO[31:08])	I/O BASE ADDRESS [31:08]: These are read/write bits allowing the system to access IDMA I/O registers.
07-02	r	00h	(BAIO[07:02])	RESERVED: These bits always read 0.
01	r	0	*reserved*	RESERVED: This bit always reads 0.
00	r	1	(IOSPIND)	I/O ADDRESS SPACE INDICATOR: This bit always reads 1 indicating that the device's base address register is requesting I/O space.

24h Memory Base Address (PBAM)

This register allows a PCI devices's memory functions to be dynamically mapped into a system's memory address space. These are the lower 32 bits of the Memory Space Base Address of a 64-bit address space.

PBAM							
31	BAM031	23	BAM023	15	BAM015	07	BAM007 = 0
30	BAM030	22	BAM022	14	BAM014	06	BAM006 = 0
29	BAM029	21	BAM021	13	BAM013	05	BAM005 = 0
28	BAM028	20	BAM020	12	BAM012	04	BAM004 = 0
27	BAM027	19	BAM019	11	BAM011 = 0	03	PREFETCH = 0
26	BAM026	18	BAM018	10	BAM010 = 0	02	MEMTYP1 = 0
25	BAM025	17	BAM017	09	BAM009 = 0	01	MEMTYP0 = 0
24	BAM024	16	BAM016	08	BAM008 = 0	00	MSPIND = 1

Bit(s)	rw	reset	Acronym	Definition
31-08	rw	00h	(BAM0[31:12])	MEMORY BASE ADDRESS [31:12]: These are the 32 read/write address bits allowing the system to map the device into a 32-bit address space.
07-04	r	0h	(BAM0[11:04])	MEMORY BASE ADDRESS [11:04]: These bits always read 0 indicating a request for a 4 Kbyte block of memory address space.
03	r	0	(PREFETCH)	PREFETCHABLE: This bit always reads 0, indicating that its memory is not prefetchable.
02-01	r	00b	(MEMTYP[01:00])	MEMORY TYPE: These bit always read 00b, indicating that the device's base address register is 32 bits and is requesting a Memory Space Base address anywhere within the 32-bit Memory Space.
00	r	0	(MSPIND)	MEMORY ADDRESS SPACE INDICATOR: This bit always reads 0 indicating that the device is requesting memory space.

2Ch Sub System Vendor ID, Sub System ID (PSUBVID[1:0], PSUBID[1:0])

The Subsystem Vendor ID and Subsystem ID registers are used to uniquely identify the add-in board or subsystem where the PCI device resides. They provide a way for add-in card vendors to distinguish their cards from one another even when the cards have the same PCI controller installed.

Note: The contents of these registers can be modified just after a power on reset. The new contents of this register will be fetched by on chip hardware from the external NVRAM. For more details, please see bit LDDFLT in register GSTAT.

PSUBID[1:0]				PSUBVID[1:0]			
31	PSUBID15 = 0	23	PSUBID07 = 0	15	PSUBVID15 = 0	07	PSUBVID07 = 0
30	PSUBID14 = 0	22	PSUBID06 = 0	14	PSUBVID14 = 0	06	PSUBVID06 = 0
29	PSUBID13 = 0	21	PSUBID05 = 1	13	PSUBVID13 = 0	05	PSUBVID05 = 0
28	PSUBID12 = 1	20	PSUBID04 = 0	12	PSUBVID12 = 1	04	PSUBVID04 = 0
27	PSUBID11 = 0	19	PSUBID03 = 0	11	PSUBVID11 = 0	03	PSUBVID03 = 0
26	PSUBID10 = 1	18	PSUBID02 = 0	10	PSUBVID10 = 0	02	PSUBVID02 = 0
25	PSUBID09 = 1	17	PSUBID01 = 1	09	PSUBVID09 = 0	01	PSUBVID01 = 0
24	PSUBID08 = 0	16	PSUBID00 = 0	08	PSUBVID08 = 1	00	PSUBVID00 = 1

Bit(s)	rw	reset	Acronym	Definition
31-16	r	1622h	(PSUBID[1:0])	SUBSYSTEM ID: Default always reads 1622h.
15-00	r	1101h	(PSUBVID[1:0])	SUBSYSTEM VENDOR ID: Default always reads 1101h.

30h Expansion ROM Base Address (PBAR)

This register allows a PCI device's expansion ROM to be mapped into a system's physical address space. A maximum of 512K bytes ROM space is supported.

PBAR							
31	BAR31	23	BAR23	15	BAR15 = 0	07	RSVD = 0
30	BAR30	22	BAR22	14	BAR14 = 0	06	RSVD = 0
29	BAR29	21	BAR21	13	BAR13 = 0	05	RSVD = 0
28	BAR28	20	BAR20	12	BAR12 = 0	04	RSVD = 0
27	BAR27	19	BAR19	11	BAR11 = 0	03	RSVD = 0
26	BAR26	18	BAR18 = 0	10	RSVD = 0	02	RSVD = 0
25	BAR25	17	BAR17 = 0	09	RSVD = 0	01	RSVD = 0
24	BAR24	16	BAR16 = 0	08	RSVD = 0	00	EXROMEN

Bit(s)	rw	reset	Acronym	Definition
31-19	rw	00h	(BAR[31:19])	EXPANSION ROM BASE ADDRESS [31:19]: These are read/write bits allowing the system to map in increments of 512K bytes of Expansion ROM space. Base Address may share a decoder with the I/O and Memory Base Address Register, device independent software should not access any other base address register of this device while the expansion ROM decode for this device is enabled.
07-02	r	00h	(BAR[18:11])	EXPANSION ROM BASE ADDRESS [18:11]. Always read 0 to set the maximum size of the Expansion ROM device to be 512 Kbytes.
10-01	r	00h	*reserved*	RESERVED: This bit always reads 0.

00	rw	0	(EXROMEN)	EXPANSION ROM DECODE ENABLE: When set it enables the decode of the Expansion ROM within System memory address space. Bit 1 of this device's Command register, the Memory Space Control bit, has precedence over this bit. It must be set to a value of 1 for this bit to enable the expansion ROM address decode.

34h Capabilities Pointer (CAPPTR)

This register is the pointer for the PCI Power management capability offset.

CAPPTR	
07	CAPPTR07 = 1
06	CAPPTR06 = 1
05	CAPPTR05 = 0
04	CAPPTR04 = 1
03	CAPPTR03 = 1
02	CAPPTR02 = 1
01	CAPPTR01 = 0
00	CAPPTR00 = 0

Bit(s)	rw	reset	Acronym	Definition
07-00	r	DCh	(CAPPTR[07:00])	CAPABILITIES POINTER: This pointer points to the PCI Power management capability offset.

3Ch Interrupt Line Select (PIL)

This register identifies which interrupt request line of a system interrupt controller the PCI device's interrupt line is connected to. Note that these encodings specify the physical pin on the system interrupt controller that the interrupt line is connected to. These encodings do not specify the interrupt vector that is generated by the interrupt controller.

PIL	
07	IL07
06	IL06
05	IL05
04	IL04
03	IL03
02	IL02
01	IL01
00	IL00

Bit(s)	rw	reset	Acronym	Definition
07-00	rw	0	(IL[07:00])	INTERRUPT LINE VALUE: Values between 00h:FEh is the interrupt line number that the device is connected to. A value of FFh indicates that the device's interrupt line is not connected to a system interrupt controller.

3Dh Interrupt Pin Select (PIP)

This register identifies which interrupt pin, INTA# through INTD#, a device function uses. This register assists in the proper initialization of the Interrupt Line register.

PIP	
15	IP07 = 0
14	IP06 = 0
13	IP05 = 0
12	IP04 = 0
11	IP03 = 0
10	IP02 = 0
09	IP01 = 0
08	IP00 = 1

Bit(s)	rw	reset	Acronym	Definition
15-08	r	01h	(IP[07:00])	INTERRUPT PIN: This register always reads 01h indicating that the device uses interrupt pin INTA#.

3Eh Minimum Grant (PMG)

This register specifies the burst period (assuming a clock rate of 33Mhz) required by the device. The value is specified in increments of 250ns (0.25us).

PMG	
23	MG07 = 0
22	MG06 = 0
21	MG05 = 0
20	MG04 = 0
19	MG03 = 0
18	MG02 = 0
17	MG01 = 0
16	MG00 = 0

Bit(s)	rw	reset	Acronym	Definition
23-16	r	00h	(MG[07:00])	MINIMUM GRANT VALUE: Always reads 0.

3Fh Maximum Latency (PML)

This register specifies how often (assuming a clock rate of 33Mhz) the device needs to gain access to the PCI Bus. The value is specified in 250ns increments (0.25us).

PML	
31	ML07 = 0
30	ML06 = 0
29	ML05 = 0
28	ML04 = 0
27	ML03 = 0
26	ML02 = 0
25	ML01 = 0
24	ML00 = 0

Bit(s)	rw	reset	Acronym	Definition
31-24	r	00h	(ML[07:00])	MAXIMUM LATENCY VALUE: Always reads 0.

DCh Capability ID (CID)

CID	
07	CID7 = 0
06	CID6 = 0
05	CID5 = 0
04	CID4 = 0
03	CID3 = 0
02	CID2 = 0
01	CID1 = 0
00	CID0 = 1

Bit(s)	rw	reset	Acronym	Definition
07-00	r	01h	(CID)	CAPABILITY ID: Indicates that the device supports PCI PMS.

DDh Next Item Pointer (NIP)

NIP	
07	NIP7
06	NIP6
05	NIP5
04	NIP4
03	NIP3
02	NIP2
01	NIP1
00	NIP0

Bit(s)	rw	reset	Acronym	Definition
07-00	r	00h	(NIP)	NEXT ITEM POINTER: The next capability points to the next capability; 00h indicates the end of the link list of capabilities.

DEh Power Management Capabilities (PMC)

PMC			
15	PMC15 = 0	07	PMC07 = 0
14	PMC14 = 0	06	PMC06 = 0
13	PMC13 = 1	05	PMC05 = 0
12	PMC12 = 0	04	PMC04 = 0
11	PMC11 = 0	03	PMC03 = 1
10	PMC10 = 1	02	PMC02 = 0
09	PMC09 = 0	01	PMC01 = 1
08	PMC08 = 0	00	PMC00 = 0

Bit(s)	rw	reset	Acronym	Definition
15-14	r	0	*reserved*	RESERVED: Always reads 0.
13	r	1	(PMC13)	PMC [13]: This bit when set to one indicates that the IDMA may assert PME# from the D2 state if the signal UINTRQ (unsolicited interrupt) is asserted on either channel.
11-12	r	0	*reserved*	RESERVED: Always reads 0.
10	r	1	(PMC10)	PMC [10]: This bit when set to one indicates that IDMA supports the D2 (standby) state.
09-04	r	0	*reserved*	RESERVED: Always reads 0.
03	r	1	(PMC03)	PMC [03]: This bit when set to one indicates that the IDMA requires a PCI clock to assert PME#.
02-00	r	010b	(PMC00/01/02)	PMC [02/01/00]: These bits when set to 010b indicate that the IDMA complies with version 1.1 of the PCI PMS.

E0h Power Management Control/Status (PMCS)

PMCS			
15	PMCS15	07	RSVD = 0
14	RSVD = 0	06	RSVD = 0
13	RSVD = 0	05	RSVD = 0
12	RSVD = 0	04	RSVD = 0
11	RSVD = 0	03	RSVD = 0
10	RSVD = 0	02	RSVD = 0
09	RSVD = 0	01	PMCS01
08	PMCS08	00	PMCS00

Bit(s)	rw	reset	Acronym	Definition
15	rw	0	(PMCS[15])	PMCS [15]: Indicates whether PME# can be asserted from power state D3-Cold. Fixed to zero indicating that the IDMA does not support PME# assertion from the D3-Cold state.
14-09	r	00h	*reserved*	RESERVED: Always reads 0.
08	rw	0	(PMCS[08])	PME# ENABLE: Controls the enable and disable of PME#. When this bit is set to one, PME# is enabled. When this bit is cleared to zero, PME# is disabled.

07-02	r	00h	*reserved*	RESERVED: Always reads 0.
01-00	rw	00	(PMCS[01/00])	PMC STATE CONTROL: Power Management State Control bits.

E2h Power Management Bridge Support Extension (BSE)

BSE	
07	BSE07 = 0
06	BSE06 = 0
05	BSE05 = 0
04	BSE04 = 0
03	BSE03 = 0
02	BSE02 = 0
01	BSE01 = 0
00	BSE00 = 0

Bit(s)	rw	reset	Acronym	Definition
07-00	r	00h	(BSE)	BRIDGE SUPPORT EXTENSION

E3h Power Management Data (PMDR)

PMDR	
07	PMDR07 = 0
06	PMDR06 = 0
05	PMDR05 = 0
04	PMDR04 = 0
03	PMDR03 = 0
02	PMDR02 = 0
01	PMDR01 = 0
00	PMDR00 = 0

Bit(s)	rw	reset	Acronym	Definition
07-00	r	00h	(PMDR)	IDMA POWER MANAGEMENT DATA

F8h Manufacture’s ID (MFTID)

MFTID							
31	MFTID31	23	MFTID23	15	MFTID15	07	MFTID07
30	MFTID30	22	MFTID22	14	MFTID14	06	MFTID06
29	MFTID29	21	MFTID21	13	MFTID13	05	MFTID05
28	MFTID28	20	MFTID20	12	MFTID12	04	MFTID04
27	MFTID27	19	MFTID19	11	MFTID11	03	MFTID03
26	MFTID26	18	MFTID18	10	MFTID10	02	MFTID02
25	MFTID25	17	MFTID17	09	MFTID09	01	MFTID01
24	MFTID24	16	MFTID16	08	MFTID08	00	MFTID00

Bit(s)	rw	reset	Acronym	Definition
31-00	r	1101 1101	(MFTID[31:00])	MANUFACTURE’S ID: Always reads 1101 1101h.

4.2 Page 0 I/O & Memory Mapped Register Descriptions

These registers are accessible through the first page of PCI Base Address Space 4 using IO cycles or PCI Base Address Space 5 by memory cycles. The register page is selected through GCTRL (offset 7C) bit 15. When this bit is cleared, page 0 is selected.

Base4/5 + 00h (Ch 0) ATA Data Port (ADATA)
Base4/5 + 40h (Ch 1)

Reset: HW Reset

This 16 bit register provides a data port for ATA PIO data transfer.

An 8-bit write to address 00 will perform a write to the lower 8 bits of ATA data.

A 16-bit write to address 00 will perform a word write to the entire 16 bits of ATA data.

ADATA1		ADATA0	
15	ADATA15	07	ADATA07
14	ADATA14	06	ADATA06
13	ADATA13	05	ADATA05
12	ADATA12	04	ADATA04
11	ADATA11	03	ADATA03
10	ADATA10	02	ADATA02
09	ADATA09	01	ADATA01
08	ADATA08	00	ADATA00

Bit(s)	rw	reset	Acronym	Definition
15:00	rw	00h	(ADATA[15:00])	ATA DATA: ATA PIO transfer data port.

Base4/5 + 01h (Ch 0) ATA Error/Feature (AERR/AFEAT)
Base4/5 + 41h (Ch 1)

Reset: HW Reset

This register is a dual purpose ATA register. When write, it is the ATA Features register whose function is command dependent. When read, it serves as the ATA Error register which reports the status of the current command.

AFEAT		AERR	
15	AFEAT07	15	AERR07
14	AFEAT06	14	AERR06
13	AFEAT05	13	AERR05
12	AFEAT04	12	AERR04
11	AFEAT03	11	AERR03
10	AFEAT02	10	AERR02
09	AFEAT01	09	AERR01
08	AFEAT00	08	AERR00

Bit(s)	rw	reset	Acronym	Definition
15:08	w	00h	(AFEAT[07:00])	ATA FEATURES: ***Write only*** and the content is command dependent.
15:08	r	00h	(AERR[07:00])	ATA ERROR: ***Read only*** and the content is command dependent.

Base4/5 + 02h (Ch 0) ATA Sector Count (ASECCNT)
Base4/5 + 42h (Ch 1)

Reset: HW Reset

This register corresponds to the ATA Sector Count register.

ASECCNT	
23	ASECCNT07
22	ASECCNT06
21	ASECCNT05
20	ASECCNT04
19	ASECCNT03
18	ASECCNT02
17	ASECCNT01
16	ASECCNT00

Bit(s)	rw	reset	Acronym	Definition
23:16	rw	00h	(ASECCNT[07:00])	ATA SECTOR COUNT: The content is command dependent.

Base4/5 + 03h (Ch 0) ATA LBA Low (ALBAL)
Base4/5 + 43h (Ch 1)

Reset: HW Reset

This register corresponds to the ATA LBA Low register.

ALBAL	
31	ALBAL07
30	ALBAL06
29	ALBAL05
28	ALBAL04
27	ALBAL03
26	ALBAL02
25	ALBAL01
24	ALBAL00

Bit(s)	rw	reset	Acronym	Definition
31:24	rw	00h	(ALBAL[07:00])	ATA LBA LOW: The content is command dependent.

Base4/5 + 04h (Ch 0) ATA LBA Mid (ALBAM)
Base4/5 + 44h (Ch 1)

Reset: HW Reset

This register corresponds to the ATA LBA Mid register.

ALBAM	
07	ALBAM07
06	ALBAM06
05	ALBAM05
04	ALBAM04
03	ALBAM03
02	ALBAM02
01	ALBAM01
00	ALBAM00

Bit(s)	rw	reset	Acronym	Definition
07:00	rw	00h	(ALBAM[07:00])	ATA LBA MID: The content is command dependent.

Base4/5 + 05h (Ch 0) ATA LBA High (ALBAH)
Base4/5 + 45h (Ch 1)

Reset: HW Reset

This register corresponds to the ATA LBA High register.

ALBAH	
15	ALBAH07
14	ALBAH06
13	ALBAH05
12	ALBAH04
11	ALBAH03
10	ALBAH02
09	ALBAH01
08	ALBAH00

Bit(s)	rw	reset	Acronym	Definition
15:08	rw	00h	(ALBAH[07:00])	ATA LBA HIGH: The content is command dependent.

Base4/5 + 06h (Ch 0) ATA Device (ADEV)
Base4/5 + 46h (Ch 1)

Reset: HW Reset

This register corresponds to the ATA Device register.

ADEV	
23	ADEV07
22	ADEV06
21	ADEV05
20	ADEV04
19	ADEV03
18	ADEV02
17	ADEV01
16	ADEV00

Bit(s)	rw	reset	Acronym	Definition
23:16	rw	00h	(ADEV[07:00])	ATA DEVICE: The content is command dependent.

Base4/5 + 07h (Ch 0) ATA Status/Command (ACMD/ASTAT)
Base4/5 + 47h (Ch 1)

Reset: HW Reset

This register is a dual purpose ATA register. When write, it is the ATA Command register. When read, it serves as the ATA Status register which reports the status of the current command.

ACMD		ASTAT	
31	ACMD07	31	ASTAT07
30	ACMD06	30	ASTAT06
29	ACMD05	29	ASTAT05
28	ACMD04	28	ASTAT04
27	ACMD03	27	ASTAT03
26	ACMD02	26	ASTAT02
25	ACMD01	25	ASTAT01
24	ACMD00	24	ASTAT00

Bit(s)	rw	reset	Acronym	Definition
31:24	w	00h	(ACMD[07:00])	ATA COMMAND: ***Write only*** and it contains the command code being sent to the device.
31:24	r	00h	(ASTAT[07:00])	ATA STATUS: ***Read only*** and the content is device status. The content is updated to reflect the current state of the device and the progress of any command being executed.

Base4/5 + 08h (Ch 0) ATA AlternateStatus/Control (ACTRL/AASTAT)
Base4/5 + 48h (Ch 1)

Reset: HW Reset

This register is a dual purpose ATA register. When write, it is the ATA Device Control register. When read, it serves as the ATA Alternate Status register which reports the status of the current command.

ACTRL		AASTAT	
07	ACTRL07	07	AASTAT07
06	ACTRL06	06	AASTAT06
05	ACTRL05	05	AASTAT05
04	ACTRL04	04	AASTAT04
03	ACTRL03	03	AASTAT03
02	ACTRL02	02	AASTAT02
01	ACTRL01	01	AASTAT01
00	ACTRL00	00	AASTAT00

Bit(s)	rw	reset	Acronym	Definition
07:00	w	00h	(ACTRL[07:00])	ATA DEVICE CONTROL: ***Write only*** it allows the host to software reset attached devices and to enable/disable INTRQ signals. Both devices respond to a single write to this register.
07:00	r	00h	(AASTAT[07:00])	ATA ALTERNATE STATUS: ***Read only*** and it contains the same value as the Status register at address 07h.

Base4/5 + 09h (Ch 0) ATA Interrupt Status (INTSTAT)
Base4/5 + 49h (Ch 1)

Reset: HW Reset & Channel Reset

This register contains the interrupt status of the corresponding SATA channel.

INTSTAT	
15	CHINTP
14	RSVD
13	CHQINT
12	CHUIRQ
11	FTLINT
10	CHCINT
09	CHON
08	CHOFF

Bit(s)	rw	reset	Acronym	Definition
15	r	0	(CHINTP)	CHANNEL INTERRUPT PENDING: This bit reflects the masked interrupt status of the SATA channel.
14	r	0	*reserved*	RESERVED: Always reads 0.
13	r	0	(CHQINT)	CHANNEL QUEUE INTERRUPT: Channel Reply FIFO queue not empty interrupt.
12	r	0	(CHUIRQ)	CHANNEL UNSOLICITED INTERRUPT: Channel Unsolicited interrupt (ATAINT).
11	r	0	(FTLINT)	FATAL ERROR INTERRUPT: Fatal Error interrupt.
10	r	0	(CHCINT)	CHANNEL COMPLETE INTERRUPT: Channel Complete interrupt.
09	r	0	(CHON)	SATA CHANNEL ON: SATA Channel detected a device being plugged in.
08	r	0	(CHOFF)	SATA CHANNEL OFF: SATA Channel detected a device being unplugged.

Base4/5 + 0Ah (Ch 0) ATA Mask Interrupt Status (MINTSTAT)
Base4/5 + 4Ah (Ch 1)

Reset: HW Reset

This register is used to mask the corresponding SATA channel interrupts.

MINTSTAT	
23	RSVD
22	RSVD
21	MCHQINT
20	MCHUIRQ
19	MFTLINT
18	MCHCINT
17	MCHON
16	MCHOFF

Bit(s)	rw	reset	Acronym	Definition
23-22	r	0	*reserved*	RESERVED: Always reads 0.
21	rw	0	(MCHQINT)	MASK CHANNEL QUEUE INTERRUPT: Mask Channel Reply FIFO queue empty interrupt.
20	rw	0	(MCHUIRQ)	MASK CHANNEL UNSOLICITED INTERRUPT: Mask Channel Unsolicited interrupt.
19	rw	0	(MFTLINT)	MASK FATAL ERROR INTERRUPT: Mask channel fatal error interrupt.
18	rw	0	(MCHCINT)	MASK CHANNEL COMPLETE INTERRUPT: Mask Channel Complete interrupt.
17	rw	0	(MCHON)	MASK SATA CHANNEL ON: Mask SATA Channel detected a device being plugged in.
16	rw	0	(MCHOFF)	MASK SATA CHANNEL OFF: Mask SATA Channel detected a device being unplugged.

Base4/5 + 0Bh (Ch 0) Physical Region Descriptor (PRD) Control (PRDCTL)
Base4/5 + 4Bh (Ch 1)

Reset: HW Reset

This register provides controls for PRD modes of operations.

PRDCTL	
31	DMAEN
30	RSVD
29	RSVD
28	RSVD
27	DIR
26	RSVD
25	RSVD
24	Start/Stop

Bit(s)	rw	reset	Acronym	Definition
31	rw	0	(DMAEN)	DMA TRANSFER ENABLE: If set to 1, DMA transfer is used. If cleared, PIO transfer is used.
30-28	r	000b	*reserved*	RESERVED: Should return to zero on read.
27	rw	0	(DIR)	DIRECTION: This bit sets the direction of the bus master transfer. When Clear, PCI master reads are performed. When set to one, PCI master writes are performed.
26-25	r	00b	*reserved*	RESERVED: Should return to zero on read.
24	rw	0	(Start/Stop)	BUS MASTER: Bus Master operation of the adapter is enabled by setting this bit to one. Master operation may be halted by clearing this bit to zero. All state information is lost when a zero is written.

Base4/5 + 0Ch (Ch 0) Physical Region Descriptor (PRD) Table Pointer
Base4/5 + 4Ch (Ch 1) (PRDTP)

Reset: HW Reset

This register reflects the current physical address of the system memory. In the scatter/gather mode, when bit 7 of the DMA Command register is set, this register contains the current physical pointer to the scatter/gather list. The descriptor table should be aligned on a Dword boundary and cannot cross a 65,536 boundary in memory.

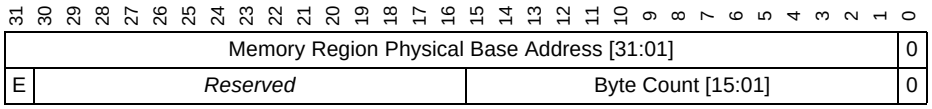
DPRDTP							
31	PRDTP31	23	PRDTP23	15	PRDTP15	07	PRDTP07
30	PRDTP30	22	PRDTP22	14	PRDTP14	06	PRDTP06
29	PRDTP29	21	PRDTP21	13	PRDTP13	05	PRDTP05
28	PRDTP28	20	PRDTP20	12	PRDTP12	04	PRDTP04
27	PRDTP27	19	PRDTP19	11	PRDTP11	03	PRDTP03
26	PRDTP26	18	PRDTP18	10	PRDTP10	02	PRDTP02
25	PRDTP25	17	PRDTP17	09	PRDTP09	01	PRDTP01 = 0
24	PRDTP24	16	PRDTP16	08	PRDTP08	00	PRDTP00 = 0

Bit(s)	rw	reset	Acronym	Definition
31-02	rw	0	(PRDTP[31:02])	PRD TABLE ADDRESS: Base address of Physical Descriptor table.
01-00	r	0	(PRDTP[01:00])	RESERVED: Always reads 0.

Physical Region Descriptor Table Entry

The memory region specified by the descriptor should not straddle a 65,536 boundary. The byte count is 16 bits long and a value of zero indicates 65,536. Bit 7 of the last byte indicates the end of table. The bus master operation should be terminated when this bit is set.

The sum of the descriptor byte count must be equal to or greater than the size of the disk transfer request.



Base4/5 + 10h (Ch 0) Physical Region Descriptor (PRD) Total Transfer Base4/5 + 50h (Ch 1) Length (PXFRCNT)

Reset: HW Reset

This register reflects the total transfer length of the entire PRD chain.

PXFRCNT							
31	PXFRCNTS07	23	PXFRCNT23	15	PXFRCNT15	07	PXFRCNT07
30	PXFRCNTS06	22	PXFRCNT22	14	PXFRCNT14	06	PXFRCNT06
29	PXFRCNTS05	21	PXFRCNT21	13	PXFRCNT13	05	PXFRCNT05
28	PXFRCNTS04	20	PXFRCNT20	12	PXFRCNT12	04	PXFRCNT04
27	PXFRCNTS03	19	PXFRCNT19	11	PXFRCNT11	03	PXFRCNT03
26	PXFRCNTS02	18	PXFRCNT18	10	PXFRCNT10	02	PXFRCNT02
25	PXFRCNTS01	17	PXFRCNT17	09	PXFRCNT09	01	PXFRCNT01
24	PXFRCNTS00	16	PXFRCNT16	08	PXFRCNT08	00	PXFRCNT00

Bit(s)	rw	reset	Acronym	Definition
31-24	rw	0	(PXFRCNTS[07:00])	PRD REMAIN COUNT SIGN BITS: These sign bits will be updated after every PRD chain completion.
23-00	rw	0	(PXFRCNT[23:00])	PRD TOTAL TRANSFER COUNT: This counter will be updated after every PRD chain completion

Base4/5 + 14h (Ch 0) IDMA Control (IDMCTL) Base4/5 + 54h (Ch 1)

Reset: HW Reset

IDMCTL			
15	MMSTR	07	aGO
14	MSLVSEL1	06	aPSE
13	MSLVSEL0	05	aRSTADM
12	MSLV	04	aABT
11	RSVD	03	aAUTEN
10	RSVD	02	aRSTA
09	HWFRZEN	01	UNFREZ
08	aIEN	00	FREZEN

Bit(s)	rw	reset	Acronym	Definition
15	rw	0	(MMSTR)	MIRROR MASTER: If set to 1 indicates the current SATA channel will act as the mirroring master.
14:13	rw	01b	(MSLVSEL[01:00])	SLAVE INDEX: If the current channel is selected to be the master, this 2 bits register selects which channel will act as the mirror slave. 00 = channel 0; 01 = channel 1; 10 = reserved; 11 = reserved Note: Setting a channel to be both mirror master and slave is prohibited.
12	rw	0	(MSLV)	MIRROR SLAVE: If set to 1 indicates the current SATA channel will act as a mirroring slave.

11-10	r	0	*reserved*	RESERVED: Always reads 0.
09	rw	0	(HWFRZEN)	HARDWARE FREEZE ENABLE: If set to 1, it will enable hardware to automatically freeze IDMA engine if an error status occurs. If cleared, software has full control of when to freeze the IDMA engine. This bit is used in conjunction with FREZEN (bit 00 of this register).
08	rw	0	(aIEN)	PCI CHANNEL INTERRUPT DISABLE: When clear, in the ATA register mode the interrupts generated by the channel are propagated through to the PCI bus. When set, interrupts are not propagated to the PCI bus.
07	rw	0	(aGO)	ADMA GO: When set, the ADMA start to run. When clear, the channel operates only in ATA register mode.
06	rw	0	(aPSE)	ADMA PAUSE: When set, the AMDA does not follow the CPB chain nor access the CPB Lookup table. The software shall pause operations before modifying the CPB chain pointers by the use of aPSE and aPAD
05	rw	0	(aRSTADM)	RESET ADMA: Set by the host to indicate a reset. Cleared by the host after 1us to allow the ADMA to come out of the IDLE state. This reset signal will reset the IDMA engine and abort all PCI master controller activities.
04	rw	0	(aABT)	ABORT PENDING COMMANDS: A self clearing bit that is set by host software to abort all pending commands.
03	rw	0	(aAUTEN)	ADMA AUTO-POLL ENABLE: This bit is used to enable a device to assert a Service Interrupt in an overlapped/queued situation.
02	rw	0	(aRSTA)	ATA HARD RESET: When set, the ATA reset signal is asserted. If the host set this bit to one, wait for a minimum reset time, and then clear this bit to zero. This reset signal will reset all ATA shadow registers and the PHY layer.
01	rw	0	(UNFREZ)	UNFREEZE IDMA: A self clearing bit that will unfreeze the IDMA operation after an error condition.
00	rw	0	(FREZEN)	FREEZE ENABLE: This bit works in conjunction with HWFRZEN (bit 09 of this register) as shown below:

HWFRZEN	FREZEN	
0	0	IDMA normal operations
0	1	IDMA engine is frozen by software until FREZEN is cleared.
1	0	IDMA normal operations
1	1	If device returns an error status, IDMA will be frozen until software writes a 1 to the UNFREZ bit to unfreeze the IDMA engine.

Base4/5 + 16h (Ch 0) IDMA Status (IDMSTAT)
Base4/5 + 56h (Ch 1)

Reset: HW Reset & Channel Reset

IDMSTAT			
31	RSVD	23	aDONE
30	RSVD	22	aPSD
29	RSVD	21	aSTPD
28	RSVD	20	aUIRQ
27	RSVD	19	aLGCY
26	RSVD	18	RSVD
25	RSVD	17	aCPBERR
24	RSVD	16	aPERR

Bit(s)	rw	reset	Acronym	Definition
31-24	r	0	*reserved*	RESERVED: Always reads 0.
23	r	0	(aDONE)	ADMA DONE: In PRD mode, when set, it indicates that the PRD has completed. In IDMA mode, it indicates the AMDA has finished one or more CPBs.
22	r	1	(aPSD)	ADMA PAUSE: When set, indicates the ADMA has stopped as a result of aPSE being set and the current transfer has been completed.
21	r	1	(aSTPD)	ADMA STOPPED: When set, indicates the AMDA has stopped as a result of aGO being cleared, an error occurring, or no more valid CPBs to be processed.
20	r	x	(aUIRQ)	ATA UNSOLICITED IRQ: When set, indicates the ATA unsolicited interrupt line is active.
19	r	1	(aLGCY)	ADMA LEGACY: When set, indicates that the ADMA is in ATA register mode.
18	r	0	*reserved*	RESERVED: Always reads 0.
17	r	0	(aCPBERR)	ADMA CPB ERROR: When set, indicates that at least one of the CPB-error response flags in he CPB has been set to one exception the case of cPSEXC and pIGEX set to one.
16	r	0	(aPERR)	PCI ERROR MODE: When set, indicates a PCI error has occurred.

Base4/5 + 18h (Ch 0) CPB Lookup Table Address (CPBLAR)
Base4/5 + 58h (Ch 1)

Reset: HW Reset & Channel Reset

The CPB Lookup Table Address is only used in overlapped or queued operation. It is initialized by the system software with the physical address of the CPB Lookup Table.

CPBLAR							
31	CPBLAR31	23	CPBLAR23	15	CPBLAR15	07	CPBLAR07
30	CPBLAR30	22	CPBLAR22	14	CPBLAR14	06	CPBLAR06
29	CPBLAR29	21	CPBLAR21	13	CPBLAR13	05	CPBLAR05
28	CPBLAR28	20	CPBLAR20	12	CPBLAR12	04	CPBLAR04
27	CPBLAR27	19	CPBLAR19	11	CPBLAR11	03	CPBLAR03
26	CPBLAR26	18	CPBLAR18	10	CPBLAR10	02	CPBLAR02
25	CPBLAR25	17	CPBLAR17	09	CPBLAR09	01	CPBLAR01
24	CPBLAR24	16	CPBLAR16	08	CPBLAR08	00	CPBLAR00

Bit(s)	rw	reset	Acronym	Definition
31-00	rw	0	(CPBLAR[31:00])	IDMA LOOKUP TABLE ADDRESS: IDMA Lookup Table Register Address.

Base4/5 + 1Ch (Ch 0) Posting Queue FIFO (PTQFIFO)
Base4/5 + 5Ch (Ch 1)

Reset: HW Reset & Channel Reset

This register is used to post Command Tag's by the Host to the INIC-1622. It is written by the Host and read by the DMA engine. Hardware must insure that the Host has access to this register for writes without having to stop the DMA engine. This FIFO queue can hold up to 32 Command Tag's. The posting FIFO can be read by the Host if necessary.

PTQFIFO	
07	RSVD
06	RSVD
05	RSVD
04	PTQFIFO04
03	PTQFIFO03
02	PTQFIFO02
01	PTQFIFO01
00	PTQFIFO00

Bit(s)	rw	reset	Acronym	Definition
07-05	r	0	*reserved*	RESERVED: Always reads 0.
04:00	rw	*	(PTQFIFO[04:00])	POSTING QUEUE FIFO: This is a window into a 32-byte FIFO.

NOTE: Reading this register when the FIFO is empty returns FFh.

Base4/5 + 1Dh (Ch 0) Posting Queue FIFO Count (PTQCNT)
Base4/5 + 5Dh (Ch 1)

Reset: HW Reset & Channel Reset

This ***read-only*** register keeps a count of the number of Command Tag's in the Posting Queue FIFO.

PTQCNT	
15	RSVD
14	RSVD
13	PTQCNT05
12	PTQCNT04
11	PTQCNT03
10	PTQCNT02
09	PTQCNT01
08	PTQCNT00

Bit(s)	rw	reset	Acronym	Definition
15-14	r	0	*reserved*	RESERVED: Always reads 0.
13-08	r	0	(PTQCNT[05:00])	POSTING QUEUE FIFO COUNT: Keeps track of the number of Command Tag entries in the Posting Queue FIFO.

Base4/5 + 1Eh (Ch 0) Reply Queue FIFO (RPQFIFO)
Base4/5 + 5Eh (Ch 1)

Reset: HW Reset & Channel Reset

This register is used to reply Command Tag's by the INIC-1622 to the Host. It is written by the DMA engine and read by the Host. Hardware must insure that the Host has access to this register for reads without having to stop the DMA engine. This FIFO queue can hold up to 32 Command Tag's. This FIFO is ***read-only*** by the Host.

RPQFIFO	
23	RSVD
22	RSVD
21	RSVD
20	RPQFIFO04
19	RPQFIFO03
18	RPQFIFO02
17	RPQFIFO01
16	RPQFIFO00

Bit(s)	rw	reset	Acronym	Definition
23-21	r	0	*reserved*	RESERVED: Always reads 0.
20-16	r	0	(RPQFIFO[04:00])	REPLY QUEUE FIFO: This is a window into a 32 bytes FIFO.

Note: Reading this register when the FIFO is empty returns FFh.

Base4/5 + 1Fh (Ch 0) Reply Queue FIFO Count (RPQCNT)
Base4/5 + 5Fh (Ch 1)

Reset: HW Reset & Channel Reset

This ***read-only*** register keeps a count of the number of Command Tag's in the Reply Queue FIFO.

RPQCNT	
31	RSVD
30	RSVD
29	RPQCNT05
28	RPQCNT04
27	RPQCNT03
26	RPQCNT02
25	RPQCNT01
24	RPQCNT00

Bit(s)	rw	reset	Acronym	Definition
31-30	r	0	*reserved*	RESERVED: Always reads 0.
29-24	r	0	(RPQCNT[05:00])	REPLY QUEUE FIFO COUNT: Keeps track of the number of completed Command Tag entries in the Reply Queue FIFO.

Base4/5 + 20h (Ch 0) Serial ATA Interface Status (SSTATUS)
Base4/5 + 60h (Ch 1)

Reset: HW Reset & Channel Reset

This is a ***read only*** register which conveys the current state of the interface and host adapter. The content of the register is updated continuously and asynchronously by the host adapter.

SSTATUS							
31	RSVD	23	RSVD	15	RSVD	07	SPD03
30	RSVD	22	RSVD	14	RSVD	06	SPD02
29	RSVD	21	RSVD	13	RSVD	05	SPD01
28	RSVD	20	RSVD	12	RSVD	04	SPD00
27	RSVD	19	RSVD	11	IPM03	03	DET03
26	RSVD	18	RSVD	10	IPM02	02	DET02
25	RSVD	17	RSVD	09	IPM01	01	DET01
24	RSVD	16	RSVD	08	IPM00	00	DET00

Bit(s)	rw	reset	Acronym	Definition
31-12	r	0	*reserved*	RESERVED: Always reads 0.
11-08	r	0	(IPM[03:00])	INTERFACE POWER MANAGEMENT STATE: 0000b = Device not present or communication not established. 0001b = Interface in active state. 0010b = Interface in PARTIAL power management state. 0110b = Interface in SLUMBER power management state. All other values reserved.
07-04	r	0	(SPD[03:00])	NEGOTIATED INTERFACE COMMUNICATION SPEED: 0000b = No negotiated speed (device not present or communication not established. 0001b = Generation 1 communication rate negotiated. All other values reserved.
03-00	r	0	(DET[03:00])	INTERFACE DEVICE DETECTION AND PHY STATE: 0000b = No device detected and Phy communication not established. 0001b = Device presence detected but Phy communication not established. 0011b = Device presence detected but Phy communication established. 0100b = Phy in offline mode as a result of the interface being disabled or running in a BIST loopback mode All other values reserved.

NOTE: The interface must be in the active state for the DET value to be accurate. When the interface is in the partial or slumber state, no communication between the host and target is established resulting in a DET value corresponding to no device present or no communication established. As a result, the insertion or removal of a device may not be accurately detected under all conditions.

Base4/5 + 24h (Ch 0) Serial ATA Error (SERROR)
Base4/5 + 64h (Ch 1)

Reset: HW Reset & Channel Reset

This register conveys the supplemental interface error information to complement the error information available in the Shadow Register block Error Register.

SERROR							
31	RSVD	23	DIAGS	15	RSVD	07	RSVD
30	RSVD	22	DIAGH	14	RSVD	06	RSVD
29	RSVD	21	DIAGC	13	RSVD	05	RSVD
28	RSVD	20	DIAGD	12	RSVD	04	RSVD
27	RSVD	19	DIAGB	11	ERRE	03	RSVD
26	RSVD	18	DIAGW	10	ERRP	02	RSVD
25	DIAGF	17	DIAGI	09	ERRC	01	ERRM
24	DIAGT	16	DIAGN	08	ERRT	00	ERRI

Bit(s)	rw	reset	Acronym	Definition
31-26	r	00h	*reserved*	RESERVED: Always reads 0.
25	rw	0	(DIAGF)	UNRECOGNISED FIS TYPE: When set to 1, this bit indictates that since the bit was last cleared, one or more FIS's were received by the transport layer with good CRC but had a FIS type field that was not recognized.
24	rw	0	(DIAGT)	TRANSPORT STATE TRANSITION ERROR: When set to 1, it indicates that an error has occurred in the transition from one state to another within the Transport layer since the last time this bit was cleared.
23	rw	0	(DIAGS)	LINK SEQUENCER ERROR
22	rw	0	(DIAGH)	HANDESHAKE ERROR
21	rw	0	(DIAGC)	CRC ERROR
20	rw	0	(DIAGD)	DISPARITY ERROR
19	rw	0	(DIAGB)	10B TO 8B DECODE ERROR
18	rw	0	(DIAGW)	COMM WAKE
17	rw	0	(DIAGI)	PHY INTERNAL ERROR
16	rw	0	(DIAGN)	PHYRDY CHANGE
15-12	r	0h	*reserved*	RESERVED: Always reads 0.
11	rw	0	(ERRE)	INTERNAL ERROR
10	rw	0	(ERRP)	PROTOCOL ERROR
09	rw	0	(ERRC)	NON-RECOVERED PERSISTENT COMMUNICATION OR DATA INTEGRITY ERROR
08	rw	0	(ERRT)	NON-RECOVERED TRANSIENT DATA INTEGRITY ERROR
07-02	r	00h	*reserved*	RESERVED: Always reads 0.
01	rw	0	(ERRM)	RECOVERED COMMUNICATION ERROR
00	rw	0	(ERRI)	RECOVERED DATA INTEGRITY ERROR

Base4/5 + 28h (Ch 0) Serial ATA Control (SCONTROL)
Base4/5 + 68h (Ch 1)

Reset: HW Reset

This register is the interface by which software controls the SATA interface capabilities.

SVONTROL							
31	RSVD	23	RSVD	15	RSVD	07	SPD03
30	RSVD	22	RSVD	14	RSVD	06	SPD02
29	RSVD	21	RSVD	13	RSVD	05	SPD01
28	RSVD	20	RSVD	12	RSVD	04	SPD00
27	RSVD	19	RSVD	11	IPM03	03	DET03
26	RSVD	18	RSVD	10	IPM02	02	DET02
25	RSVD	17	RSVD	09	IPM01	01	DET01
24	RSVD	16	RSVD	08	IPM00	00	DET00

Bit(s)	rw	reset	Acronym	Definition
31-12	r	0	*reserved*	RESERVED: Always reads 0.
11:08	rw	0	(IPM[03:00])	ENABLED INTERFACE POWER MANAGEMENT STATE: This can be invoked via SATA interface power management capabilities. 0000b = No interface power management state restrictions. 0001b = Transition to PARTIAL power management state disabled. 0010b = Transition to SLUMBER power management state disabled. 0110b = Transition to both PARTIAL and SLUMBER power management state disabled. All other values reserved.
07:04	rw	0	(SPD[03:00])	HIGHEST ALLOWED COMMUNICATION SPEED: 0000b = No speed negotiation restrictions. 0001b = Limit speed negotiation to a rate not greater than Generation 1 communication rate. All other values reserved.
03:00	rw	0	(DET[03:00])	DEVICE DETECTION AND INTERFACE INITIALIZATION CONTROL: 0000b = No device detection or initialization action requested. 0001b = Perform interface initialization communication initialization sequence to establish communication. 0100b = Disable the SATA interface and put Phy in offline mode. All other values reserved.

Base4/5 + 2Ch (Ch 0) Serial ATA Active (SACTIVE)
Base4/5 + 6Ch (Ch 1)

Reset: HW Reset & Channel Reset

This register shows the status of the SATA interface.

SACTIVE							
31	SACTIVE31	23	SACTIVE23	15	SACTIVE15	07	SACTIVE07
30	SACTIVE30	22	SACTIVE22	14	SACTIVE14	06	SACTIVE06
29	SACTIVE29	21	SACTIVE21	13	SACTIVE13	05	SACTIVE05
28	SACTIVE28	20	SACTIVE20	12	SACTIVE12	04	SACTIVE04
27	SACTIVE27	19	SACTIVE19	11	SACTIVE11	03	SACTIVE03
26	SACTIVE26	18	SACTIVE18	10	SACTIVE10	02	SACTIVE02
25	SACTIVE25	17	SACTIVE17	09	SACTIVE09	01	SACTIVE01
24	SACTIVE24	16	SACTIVE16	08	SACTIVE08	00	SACTIVE00

Bit(s)	rw	reset	Acronym	Definition
31-00	rw	0	(SACTIVE[31:00])	SERIAL ATA ACTIVE: Bit positions are set to one for each command TAG still outstanding. Device clears bit positions when command is completed.

Base4/5 + 3Ch External EEPROM Address (EPAD)

Reset: HW Reset

This register provides the address for the external BIOS. It also provides Auto Address Increment Control.

EPAD					
23	RSVD	15	EPAD15	07	EPAD07
22	RSVD	14	EPAD14	06	EPAD06
21	RSVD	13	EPAD13	05	EPAD05
20	RSVD	12	EPAD12	04	EPAD04
19	RSVD	11	EPAD11	03	EPAD03
18	EPAD18	10	EPAD10	02	EPAD02
17	EPAD17	09	EPAD09	01	EPAD01
16	EPAD16	08	EPAD08	00	EPAD00

Bit(s)	rw	reset	Acronym	Definition
23-19	r	00h	*reserved*	RESERVED: Always reads 0.
18:00	rw	0	(EPAD[18:00])	E^2PROM ADDRESS: These bits are used to provide the address offset for the device's BIOS.

Base4/5 + 3Fh External EEPROM Data Port (EPDATA)

Reset: HW Reset

This register provides a data port to read/write data from/to the external BIOS.

EPDATA	
31	EPDATA07
30	EPDATA06
29	EPDATA05
28	EPDATA04
27	EPDATA03
26	EPDATA02
25	EPDATA01
24	EPDATA00

Bit(s)	rw	reset	Acronym	Definition
31:24	rw	*	(EPDATA[07:00])	E^2PROM DATA PORT: These bits provide a port to read/write data from/ to the E^2PROM BIOS.

Base4/5 + 7Ch Global Control (GCTRL)

Reset: HW Reset

This register controls various functions of the INIC-1622.

GCTRL			
15	RPGSEL	07	RSVD
14	SINT	06	RSVD
13	SOFTRST	05	LED1
12	PWRDWN	04	LED0
11	FTHD1	03	SWLED
10	FTHD0	02	MIREN
09	RSVD = 0	01	EEPRG
08	GINTDIS	00	MRMUL

Bit(s)	rw	reset	Acronym	Definition
15	rw	0	(RPGSEL)	REGISTER PAGE SELECT: 0 = Register Page 0 will be accessible; 1 = Register Page 1 will be accessible
14	rw	0	(SINT)	SOFTWARE INTERRUPT SET: This is a self clearing bit that enables the software interrupt, SOFTINT, in the GINT register.
13	rw	0	(SOFTRST)	SOFTWARE RESET: A self clearing bit that generates a warm reset to the entire chip. The duration of the software reset equals 3 PCI clock wide. This reset signal will reset the entire chip except the PCI configuration registers and PHY layer.
12	rw	0	(PWRDWN)	POWERDOWN: When set, the LINK-PHY interface will go into power-down mode. When clear, LINK-PHY interface will resume operation in normal mode.

11:10	rw	00b	(FTDH[1:0])	FIFO THRESHOLD These two bits determine the point at which a PCI burst transfer occurs. The definitions are as follows : = 00 - FIFO ¾ Full during a read FIFO ¾ Empty during write = 01 - FIFO Full during a read FIFO Empty during a write = 10 - FIFO ½ Full during a read FIFO ½ Empty during a write = 11 - Reserved
09	r	0	*reserved*	RESERVED: These bits are reserved for future definition. Always reads 0.
08	rw	0	(GINTDIS)	GLOBAL INTERRUPT DISABLE: When set to 1, PCI interrupt will be disabled. When set to 0, PCI Interrupt is enabled.
07-06	r	0	*reserved*	RESERVED: These bits are reserved for future definition. Always reads 0.
05	rw	0	(LED1)	LED1 CONTROL: When HWLED is set, this port allows software to control the LED flash frequency.
04	rw	0	(LED0)	LED0 CONTROL: When HWLED is set, this port allows software to control the LED flash frequency.
03	rw	0	(SWLED)	SOFTWARE CONTROL LED ENABLE: When set, software has full control of LED activity. When clear, the LED's are controlled by hardware.
02	rw	0	(MIREN)	MIRRORING ENABLE: When set to 1, write data will be mirrored to both channel 0 & channel 1.
01	rw	0	(EEPRG)	ENABLE EEPROM PROGRAMMING: When set, the external EEPROM can be programmed. When reset, the external EEPROM cannot be programmed. This bit being set also allows the Subclass, subsystem device ID and subsystem vendor ID registers to be programmed.
00	rw	0	(MRMUL)	ENABLE MEMORY READ MULTIPLE COMMAND: When set, the device as a bus master will use this command to fetch multiple cache lines. When reset, the device will use the Memory Read Command instead.

Base4/5 + 7Eh Global Status (GSTAT)

Reset: HW Reset & Channel Reset

This register indicates the type of ATA connector being used.

GSTAT			
31	RSVD	23	RSVD
30	RSVD	22	RSVD
29	CH1IDLE	21	RSVD
28	CH0IDLE	20	RSVD
27	RSVD	19	RSVD
26	RSVD	18	RSVD
25	SATAPST1	17	RSVD
24	SATAPST0	16	LDDFLT

Bit(s)	rw	reset	Acronym	Definition
31-30	r	0	*reserved*	RESERVED: Always reads 0.

29	r	1	(CH1IDLE)	CHANNEL 1 IDLE: When set, this bit indicates thatChannel 1 is idle and there is no pending command
28	r	1	(CH0IDLE)	CHANNEL 0 IDLE: When set, this bit indicates thatChannel 0 is idle and there is no pending command
27-26	r	00b	*reserved*	RESERVED: Always reads 0.
25	r	0	(SATAPST1)	SECONDARY DEVICE PRESENT: 1 = device present 0 = no device plugged in
24	r	0	(SATAPST0)	PRIMARY DEVICE PRESENT: 1 = device present 0 = no device plugged in
23-17	r	00h	*reserved*	RESERVED: Always reads 0.
16	r	*	(LDDFLT)	LOAD DEFAULT STATUS: This bit is set with the value sensed on pin MD2 after a power on reset. MD2 needs to be pulled down if the hardware is to retain the default power on reset values for the following registers: Sub System ID, Sub System Vendor ID, Sub Class, Vendor ID and Device ID. If the sensed value of pin MD2 after a power on reset is a one (default), then the hardware will load the 72 bit shifted in value from the Non Volatile Serial EEPROM. The format for this data in the Non Volatile SEEPROM is as follows: Bytes 0-1 Sub System Vendor ID Bytes 2-3 Sub System ID Byte 4 Sub Class Bytes 5-6 Vendor ID Bytes 7-8 Device ID

Base4/5 + BCh Global Interrupt Status (GINTS)

Reset: HW Reset & Channel Reset

This register provides the global status of the interrupt inside the INIC-1622.

GINTS			
15	GINT	07	RSVD
14	SOFTINT	06	RSVD
13	RSVD	05	RSVD
12	RSVD	04	RSVD
11	RSVD	03	RSVD
10	RSVD	02	RSVD
09	RSVD	01	CH1INT
08	RSVD	00	CH0INT

Bit(s)	rw	reset	Acronym	Definition
15	r	0	(GINT)	GLOBAL INTERRUPT:

14	r	0	(SOFTINT)	SOFTWARE INTERRUPT: This bit will be set while software writes ‘1’ to SINT in GCTRL register. When software writes ‘1’, this bit will be cleared.
13-02	r	00h	*reserved*	RESERVED: Always reads 0.
01	r	0	(CH1INT)	CHANNEL 1 INTERRUPT: This bit reflects Channel 1 Interrupt Status[7]. (Offset 49[7]) is the masked interrupt status of SATA channel 1.
00	r	0	(CH0INT)	CHANNEL 0 INTERRUPT: This bit reflects Channel 0 Interrupt Status[7]. (Offset 09[7]) is the masked interrupt status of SATA channel 0.

Base4/5 + BEh Global Interrupt Mask (GIMSK)

Reset: HW Reset

This register provides the global interrupt mask for various interrupt sources.

GIMSK			
31	RSVD	23	RSVD
30	MSOFTINT	21	RSVD
29	RSVD	20	RSVD
28	RSVD	20	RSVD
27	RSVD	19	RSVD
26	RSVD	18	RSVD
25	RSVD	17	MCH1INT
24	RSVD	16	MCH0INT

Bit(s)	rw	reset	Acronym	Definition
31	r	0	*reserved*	RESERVED: Always reads 0.
30	r/w	1	(MSOFTINT)	MASK SOFTWARE INTERRUPT
29-18	r	0h	*reserved*	RESERVED: Always reads 0.
17	r/w	1	(MCH1INT)	MASK CHANNEL 1 INTERRUPT
16	r/w	0	(MCH0INT)	MASK CHANNEL 0 INTERRUPT

Base4/5 + FEh Non Volatile RAM Port (NVRAM)

Reset: HW Reset

This register provides a mechanism to access the Non Volatile RAM data.

NVRAM	
23	RSVD = 0
21	RSVD = 0
20	RSVD = 0
20	RSVD = 0
19	NVRCK
18	NVRDO
17	NVREN
16	NVRDI

Bit(s)	rw	reset	Acronym	Definition
23:20	r	0	*reserved*	RESERVED: Always reads 0.
19	r/w	1	(NVRCK)	NON VOLATILE RAM CLOCK: This bit is toggled by the controlling driver to clock serial data into and out of the Non Volatile RAM.
18	r/w	0	(NVRDO)	NON VOLATILE RAM WRITE DATA: This bit is used to write serial data out to the Non Volatile RAM.
17	r/w	1	(NVREN)	NON VOLATILE RAM DATA OUTPUT ENABLE: When set the NVRDI output driver will be enabled. When cleared, NVRDI will be in input mode.
16	r/w	0	(NVRDI)	NON VOLATILE RAM READ DATA: This bit is used to read serial data in from the Non Volatile RAM.

4.3 Page 1 I/O & Memory Mapped Register Descriptions

These registers are accessible through the first page of PCI Base Address Space 4 using IO cycles or PCI Base Address Space 5 by memory cycles. The register page is selected through GCTRL (offset 7C) bit 15. When this bit is cleared, page 1 is selected.

Base4/5 + 00h (Ch 0) Transport Layer Debug Bus (TP_DEBUG)
Base4/5 + 40h (Ch 1)

Reset: HW Reset

This 32-bit register is used for debugging purposes. It provides a read port for various transport layer signals.

	TP_DB3		TP_DB2		TP_DB1		TP_DB0
31	TP_DB31	23	TP_DB23	15	TP_DB15	07	TP_DB07
30	TP_DB30	22	TP_DB22	14	TP_DB14	06	TP_DB06
29	TP_DB29	21	TP_DB21	13	TP_DB13	05	TP_DB05
28	TP_DB28	20	TP_DB20	12	TP_DB12	04	TP_DB04
27	TP_DB27	19	TP_DB19	11	TP_DB11	03	TP_DB03
26	TP_DB26	18	TP_DB18	10	TP_DB10	02	TP_DB02
25	TP_DB25	17	TP_DB17	09	TP_DB09	01	TP_DB01
24	TP_DB24	16	TP_DB16	08	TP_DB08	00	TP_DB00

Bit(s)	rw	reset	Acronym	Definition
31-00	r	00h	(TP_DB[31:00])	TRANSPORT LAYER DEBUG BUS

Base4/5 + 04h (Ch 0) Link Layer Debug Bus (LK_DEBUG)
Base4/5 + 44h (Ch 1)

Reset: HW Reset

This 32-bit register is used for debugging purposes. It provides a read port for various link layer signals.

	LK_DB3		LK_DB2		LK_DB1		LK_DB0
31	LK_DB31	23	LK_DB23	15	LK_DB15	07	LK_DB07
30	LK_DB30	22	LK_DB22	14	LK_DB14	06	LK_DB06
29	LK_DB29	21	LK_DB21	13	LK_DB13	05	LK_DB05
28	LK_DB28	20	LK_DB20	12	LK_DB12	04	LK_DB04
27	LK_DB27	19	LK_DB19	11	LK_DB11	03	LK_DB03
26	LK_DB26	18	LK_DB18	10	LK_DB10	02	LK_DB02
25	LK_DB25	17	LK_DB17	09	LK_DB09	01	LK_DB01
24	LK_DB24	16	LK_DB16	08	LK_DB08	00	LK_DB00

Bit(s)	rw	reset	Acronym	Definition
31-00	r	00h	(LK_DB[31:00])	LINK LAYER DEBUG BUS

Base4/5 + 08h (Ch 0) Current PCI Bus Master Address (DCXA)
Base4/5 + 48h (Ch 1)

Reset: HW Reset

This 32-bit register provides the current PCI bus master address.

	DCXA3		DCXA2		DCXA1		DCXA0
31	DCXA31	23	DCXA23	15	DCXA15	07	DCXA07
30	DCXA30	22	DCXA22	14	DCXA14	06	DCXA06
29	DCXA29	21	DCXA21	13	DCXA13	05	DCXA05
28	DCXA28	20	DCXA20	12	DCXA12	04	DCXA04
27	DCXA27	19	DCXA19	11	DCXA11	03	DCXA03
26	DCXA26	18	DCXA18	10	DCXA10	02	DCXA02
25	DCXA25	17	DCXA17	09	DCXA09	01	DCXA01
24	DCXA24	16	DCXA16	08	DCXA08	00	DCXA00

Bit(s)	rw	reset	Acronym	Definition
31-00	r	00h	(DCXA[31:00])	CURRENT PCI BUS MASTER ADDRESS

Base4/5 + 10h (Ch 0) Current PCI Bus Master Transfer Count (DCXC)
Base4/5 + 50h (Ch 1)

Reset: HW Reset

This 32-bit register provides the current PCI bus master transfer count.

	Reserved		DCXC2		DCXC1		DCXC0
31	RSVD	23	DCXC23	15	DCXC15	07	DCXC07
30	RSVD	22	DCXC22	14	DCXC14	06	DCXC06
29	RSVD	21	DCXC21	13	DCXC13	05	DCXC05
28	RSVD	20	DCXC20	12	DCXC12	04	DCXC04
27	RSVD	19	DCXC19	11	DCXC11	03	DCXC03
26	RSVD	18	DCXC18	10	DCXC10	02	DCXC02
25	RSVD	17	DCXC17	09	DCXC09	01	DCXC01
24	RSVD	16	DCXC16	08	DCXC08	00	DCXC00

Bit(s)	rw	reset	Acronym	Definition
31-24	r	00h	*reserved*	RESERVED: Always reads 0.
23-00	r	00h	(DCXC[23:00])	CURRENT PCI BUS MASTER TRANSFER COUNT

Base4/5 + 14h (Ch 0) Current PCI FIFO Count (FFLAG)
Base4/5 + 54h (Ch 1)

Reset: HW Reset

This register provides the current PCI data FIFO count status.

	FFLAG1		FFLAG0
15	RSVD	07	FFLAG07
14	RSVD	06	FFLAG06
13	RSVD	05	FFLAG05
12	RSVD	04	FFLAG04
11	RSVD	03	FFLAG03
10	RSVD	02	FFLAG02
09	RSVD	01	FFLAG01
08	FFLAG08	00	FFLAG00

Bit(s)	rw	reset	Acronym	Definition
15:09	r	00h	*reserved*	RESERVED: Always reads 0.
08-00	r	00h	(FFLAG[08:00])	CURRENT PCI DATA FIFO COUNT STATUS

Base4/5 + 18h (Ch 0) Current IDMA State Machine State (IDMA_SM_CS)
Base4/5 + 58h (Ch 1)

Reset: HW Reset

This register provides the IDMA engine state machine current state.

	IDMA_SM_CS1		IDMA_SM_CS0
15	RSVD	07	IDMA_SM_CS07
14	IDMA_SM_CS14	06	IDMA_SM_CS06
13	IDMA_SM_CS13	05	IDMA_SM_CS05
12	IDMA_SM_CS12	04	IDMA_SM_CS04
11	IDMA_SM_CS11	03	IDMA_SM_CS03
10	IDMA_SM_CS10	02	IDMA_SM_CS02
09	IDMA_SM_CS09	01	IDMA_SM_CS01
08	IDMA_SM_CS08	00	IDMA_SM_CS00

Bit(s)	rw	reset	Acronym	Definition
15	r	0	*reserved*	RESERVED: Always reads 0.
14-00	r	00h	(IDMA_SM_CS[14:00])	CURRENT IDMA STATE MACHINE STATE

Base4/5 + 1Ah (Ch 0) Current APRD State Machine State (APRD_SM_CS)
Base4/5 + 5Ah (Ch 1)

Reset: HW Reset

This register provides the APRD state machine current state.

	APRD_SM_CS1		APRD_SM_CS0
31	FPDMA_SM_CS07	23	APRD_SM_CS07
30	FPDMA_SM_CS06	22	APRD_SM_CS06
29	FPDMA_SM_CS05	21	APRD_SM_CS05
28	FPDMA_SM_CS04	20	APRD_SM_CS04
27	FPDMA_SM_CS03	19	APRD_SM_CS03
26	FPDMA_SM_CS02	18	APRD_SM_CS02
25	FPDMA_SM_CS01	17	APRD_SM_CS01
24	APRD_SM_CS08	16	APRD_SM_CS00

Bit(s)	rw	reset	Acronym	Definition
31-25	r	00h	(FPDMA_SM_CS[07:01])	CURRENT FPDMA STATE MACHINE STATE
24-16	r	00h	(APRD_SM_CS[08:00])	CURRENT APRD STATE MACHINE STATE

Base4/5 + 20h (Ch 0) Physical Layer Debug Bus (PHY_DEBUG)
Base4/5 + 60h (Ch 1)

Reset: HW Reset

This 32-bit register is used for debugging purposes. It provides a read port for various PHY layer signals.

	PHY_DB3		PHY_DB2		PHY_DB1		PHY_DB0
31	PHY_DB31	23	PHY_DB23	15	PHY_DB15	07	PHY_DB07
30	PHY_DB30	22	PHY_DB22	14	PHY_DB14	06	PHY_DB06
29	PHY_DB29	21	PHY_DB21	13	PHY_DB13	05	PHY_DB05
28	PHY_DB28	20	PHY_DB20	12	PHY_DB12	04	PHY_DB04
27	PHY_DB27	19	PHY_DB19	11	PHY_DB11	03	PHY_DB03
26	PHY_DB26	18	PHY_DB18	10	PHY_DB10	02	PHY_DB02
25	PHY_DB25	17	PHY_DB17	09	PHY_DB09	01	PHY_DB01
24	PHY_DB24	16	PHY_DB16	08	PHY_DB08	00	PHY_DB00

Bit(s)	rw	reset	Acronym	Definition
31-00	r	00h	(PHY_DEBUG[31:00])	PHYSICAL LAYER DEBUG BUS

Base4/5 + 38h (Ch 0) Physical Layer Control (PHYCTL)
Base4/5 + 78h (Ch 1)

Reset: HW Reset

This 32-bit register is used for debugging purposes. It provides a read/write port for various PHY layer control signals.

	PHYCTL3		PHYCTL2		PHYCTL1		PHYCTL0
31	PHYCTL31	23	PHYCTL23	15	PHYCTL15	07	PHYCTL07
30	PHYCTL30	22	PHYCTL22	14	PHYCTL14	06	PHYCTL06
29	PHYCTL29	21	PHYCTL21	13	PHYCTL13	05	PHYCTL05
28	PHYCTL28	20	PHYCTL20	12	PHYCTL12	04	PHYCTL04
27	PHYCTL27	19	PHYCTL19	11	PHYCTL11	03	PHYCTL03
26	PHYCTL26	18	PHYCTL18	10	PHYCTL10	02	PHYCTL02
25	PHYCTL25	17	PHYCTL17	09	PHYCTL09	01	PHYCTL01
24	PHYCTL24	16	PHYCTL16	08	PHYCTL08	00	PHYCTL00

Bit(s)	rw	reset	Acronym	Definition
31-00	rw	00h	(PHYCTL[31:00])	PHYSICAL LAYER CONTROL BUS

4.4 IDMA SSPLL I/O Register Descriptions

All the IDMA SSPLL I/O registers are accessible through the second page of the PCI Base Address Space 4 using I/O cycles or PCI Base Address Space 5 by memory cycles.

These registers control the internal Spread Spectrum PLL (SSPLL) functions.

Only word writes are valid for the SSPLL registers. Any byte writes will be ignored. Writes to address offset 3C-3F will not take effect until a write to address offset BC-BF is being performed. At that moment, all 5 registers will be written as a 64-bit entity.

Base4/5 + 3Ch SSPLL Input Divider (SIDIV)

Reset: HW Reset

SIDIV			
15	RSVD	07	IND07
14	RSVD	06	IND06
13	RSVD	05	IND05
12	RSVD	04	IND04
11	RSVD	03	IND03
10	INPR01	02	IND02
09	INPR00	01	IND01
08	IND08	00	IND00

Bit(s)	rw	reset	Acronym	Definition
15:11	r	0	*reserved*	RESERVED: Always reads 0.
10-09	r/w	10b	(INPR[01:00])	PROGRAMMABLE INPUT PRE-SCALER
08-00	r/w	0C0h	(IND[08:00])	PROGRAMMABLE INPUT DIVIDER VALUE

Base4/5 + 3Eh SSPLL Feedback Divider (SFDIV)

Reset: HW Reset

SFDIV			
31	RSVD	23	FBD07
30	FBPR01	22	FBD06
29	FBPR00	21	FBD05
28	FBD12	20	FBD04
27	FBD11	19	FBD03
26	FBD10	18	FBD02
25	FBD09	17	FBD01
24	FBD08	16	FBD00

Bit(s)	rw	reset	Acronym	Definition
31	r	0	*reserved*	RESERVED: Always reads 0.
30-29	r/w	10b	(FBPR[01:00])	PROGRAMMABLE FEEDBACK PRE-SCALER
28-16	r/w	0D80h	(FBD[12:00])	PROGRAMMABLE FEEDBACK DIVIDER VALUE

Base4/5 + BCh SSPLL Modulation Control (SMCTL)

Reset: HW Reset

The power on default is down spread 0.5%.

SMCTL	
07	RSVD
06	SSMOD05
05	SSMOD04
04	SSMOD03
03	SSMOD02
02	SSMOD01
01	SSMOD00
00	SSON

Bit(s)	rw	reset	Acronym	Definition
07	r	0	*reserved*	RESERVED: Always reads 0.
06-01	r/w	01h	(SSMOD[05:00])	SSP CONTROL
00	r/w	0	(SSON)	SSP ENABLE: When set, SSP is enabled. When cleared, SSP is disabled.

Base4/5 + BDh SSPLL PLL Loop (SPLOOP)

Reset: HW Reset

SPLOOP	
23	RSVD
22	RSVD
21	IS000
20	LRPI
19	MRPI
18	SRPI
17	VCO01
16	VCO00

Bit(s)	rw	reset	Acronym	Definition
23-22	r	00b	*reserved*	RESERVED: Always reads 0.
21	r/w	0	(IS100)	SSPLL VCO CURRENT 100µA ENABLE
20	r/w	0	(LRPI)	LOOP FILTER RESISTOR CONTROL 2
19	r/w	0	(MRPI)	LOOP FILTER RESISTOR CONTROL 1
18	r/w	0	(SRPI)	LOOP FILTER RESISTOR CONTROL 0
17-16	r/w	01b	(VCO[01:00])	SVCO GAIN CONTROL

4.5 Command Parameter Blocks (CPB) Register Descriptions

The Command Parameter Blocks, which reside in the system memory, is the mechanism through which software uses to issue commands to the host engine. Based on the CPB parameters, host hardware will issue the appropriate commands to the storage devices. When the command is completed, hardware will update the CPB structure in the system memory with the command status. The CPB structure is described below.

00h Response Flags (RFLAG)

The Response Flags describe the status of completed commands. After each command is completed, the Response Flags will be updated by PCI bus master communicating the command status to the host software.

RFLAG	
07	cCPBER
06	cPSEXC
05	cPSDEF
04	cSPNT
03	cATERR
02	cIGNRD
01	cREL
00	cDONE

Bit(s)	rw	reset	Acronym	Definition
07	rw	0	(cCPBER)	CPB ERROR FLAG: When set indicates the CPB is inconsistent.
06	rw	0	(cPSEXC)	APRD EXCESS LENGTH ERROR FLAG: The IDMA engine will set this bit to 1 if the APRD data transfer length is in excess of that required to complete the command.
05	rw	0	(cPSDEF)	APRD DEFICIENCY LENGTH ERROR: The IDMA engine will set this bit to 1 if the APRD data transfer lengths are insufficient to complete the command.
04	rw	0	(cSPNT)	ATA SPURIOUS INTERRUPT ERROR: IDMA engine dected a spurious interrupt on the ATA INTRQ signal during execution of a command.
03	rw	0	(cATERR)	ATA COMMAND ERROR FLAG: If ATA ERR is set to one during execution of the command, this bit will be set.
02	rw	0	(cIGNRD)	CPB IGNORED: If the cVLD, cREL and cDONE are all cleared. This bit will be set.
01	rw	0	(cREL)	ATA RELEASE FLAG: If the command is released, this bit will be set.
00	rw	0	(cDONE)	ATA COMMAND COMPLETE FLAG: This bit will be set by the IDMA engine when the command is completed.

01h ATA Error Shadow (ATAERR)

When the Host programs the CPB, this byte of data is ignored. At the end of a command, the IDMA engine will update the content of this register to reflect the content of the ATA Error register after status update.

ATAERR	
07	ATAERR07
06	ATAERR06
05	ATAERR05
04	ATAERR04
03	ATAERR03
02	ATAERR02
01	ATAERR01
00	ATAERR00

Bit(s)	rw	reset	Acronym	Definition
07:00	rw	0	(ATAERR[07:00])	ATA ERROR: ATA Error register content.

02h ATA Status Shadow (ATASTAT)

When the Host programs the CPB, this byte of data is ignored. At the end of a command, the IDMA engine will update the content of this register to reflect the content of the ATA Status register after status update.

ATAERR	
07	ATASTAT07
06	ATASTAT06
05	ATASTAT05
04	ATASTAT04
03	ATASTAT03
02	ATASTAT02
01	ATASTAT01
00	ATASTAT00

Bit(s)	rw	reset	Acronym	Definition
07:00	rw	0	(ATASTAT[07:00])	ATA STATUS: ATA Status register content.

03h Control Flags (CFLAG)

The Control Flags describe the validity and command type of each CPB.

CFLAG	
07	RSVD
06	RSVD
05	RSVD
04	DEVDIR
03	cIEN
02	RSVD
01	cQUE
00	cVLD

Bit(s)	rw	reset	Acronym	Definition
07-05	r	0	*reserved*	RESERVED: Always reads 0.

04	rw	0	(DEVDIR)	DEVICE DIRECTION CONTROL: 0 = PRD decide direction 1 = device control direction.
03	rw	0	(cIEN)	PCI INTERRUPT ENABLE: When set will enable command complete interrupt.
02	r	0	*reserved*	RESERVED: Always reads 0.
01	rw	0	(cQUE)	QUEUED COMMAND: This bit should be set for queued commands and cleared otherwise.
00	rw	0	(cVLD)	CPB VALID: It is used in conjuction with cDONE and cREL to control the processing of the CPB by the IDMA engine. When cDONE is set, the CPB will not be processed.

04h Total Transfer Length (cTLEN)

The Total Transfer Length is the number of total bytes to be transfered.

cTLEN							
31	cSIGN07	23	cTLEN23	15	cTLEN15	07	cTLEN07
30	cSIGN06	22	cTLEN22	14	cTLEN14	06	cTLEN06
29	cSIGN05	21	cTLEN21	13	cTLEN13	05	cTLEN05
28	cSIGN04	20	cTLEN20	12	cTLEN12	04	cTLEN04
27	cSIGN03	19	cTLEN19	11	cTLEN11	03	cTLEN03
26	cSIGN02	18	cTLEN18	10	cTLEN10	02	cTLEN02
25	cSIGN01	17	cTLEN17	09	cTLEN09	01	cTLEN01
24	cSIGN00	16	cTLEN16	08	cTLEN08	00	cTLEN00

Bit(s)	**rw**	**reset**	**Acronym**	**Definition**
31-24	rw	0	(cSIGN[07:00])	SIGN BITS: Sign bit duplicated on all 8 bits.
23-00	rw	0	(cTLEN[23:00])	TRANSFER LENGTH: The total transfer length in bytes of the CPB command.

08h First PRD Address Pointer (cPRD)

The First PRD Address Pointer points to first PRD structure in the system memory.

cPRD							
31	cPRD31	23	cPRD23	15	cPRD15	07	cPRD07
30	cPRD30	22	cPRD22	14	cPRD14	06	cPRD06
29	cPRD29	21	cPRD21	13	cPRD13	05	cPRD05
28	cPRD28	20	cPRD20	12	cPRD12	04	cPRD04
27	cPRD27	19	cPRD19	11	cPRD11	03	cPRD03
26	cPRD26	18	cPRD18	10	cPRD10	02	cPRD02
25	cPRD25	17	cPRD17	09	cPRD09	01	cPRD01
24	cPRD24	16	cPRD16	08	cPRD08	00	cPRD00

Bit(s)	**rw**	**reset**	**Acronym**	**Definition**
31-00	rw	0	(cPRD[31:00])	FIRST PRD ADDRESS POINTER: Host memory Address of the first PRD for this CPB. Shall be Qword aligned.

10h ATA Shadow Register Block

The register order is shown in the CPB Structure Definition table (Section 4.5).

13h Mirror Control (MIRCTL)

The Mirror Control register controls the hardware mirroring functions of the IDMA engine.

MIRCTL	
31	MMSTR
30	SLVIDX01
29	SLVIDX00
28	RSVD
27	RSVD
26	RSVD
25	RSVD
24	RSVD

Bit(s)	rw	reset	Acronym	Definition
31	rw	0	(MMSTR)	MIRROR MASTER: If set to 1 indicates the current bus master will act as a mirroring master.
30-29	rw	00b	(SLVIDX)	SLAVE INDEX: If the current channel is selected to be the master, this 2-bit register selects which channel will act as the mirror slave. 00 = channel 0 01 = channel 1 10 = reserved 11 = reserved Note: Setting a channel to be both mirror master and slave is prohibited.
28-24	r	0	*reserved*	RESERVED: Always reads 0.

22h Slave ATA Error Shadow (SATAERR)

When the Host programs the CPB, this byte of data is ignored. At the end of a mirror write command, the IDMA engine will update the content of this register to reflect the content of the Slave ATA Error register after status update.

SATAERR	
07	SATAERR07
06	SATAERR06
05	SATAERR05
04	SATAERR04
03	SATAERR03
02	SATAERR02
01	SATAERR01
00	SATAERR00

Bit(s)	rw	reset	Acronym	Definition
07:00	rw	0	(SATAERR[07:00])	SLAVE ATA ERROR: Slave ATA Error register content.

23h Slave ATA Status Shadow (SATASTAT)

When the Host programs the CPB, this byte of data is ignored. At the end of a mirror write command, the IDMA engine will update the content of this register to reflect the content of the Slave ATA Status register after status update.

SATASTAT	
07	SATASTAT07
06	SATASTAT06
05	SATASTAT05
04	SATASTAT04
03	SATASTAT03
02	SATASTAT02
01	SATASTAT01
00	SATASTAT00

Bit(s)	rw	reset	Acronym	Definition
07:00	rw	0	(SATASTAT[07:00])	SLAVE ATA STATUS: Slave ATA Status register content.

4.6 PRD Structure Register Descriptions

The Physical Region Descriptors, which reside in the system memory, provide the location and the amount of data to be transferred. The PRD structure is described below.

00h Physical Memory Address (pMAD)

pMAD							
31	pMAD31	23	pMAD23	15	pMAD15	07	pMAD07
30	pMAD30	22	pMAD22	14	pMAD14	06	pMAD06
29	pMAD29	21	pMAD21	13	pMAD13	05	pMAD05
28	pMAD28	20	pMAD20	12	pMAD12	04	pMAD04
27	pMAD27	19	pMAD19	11	pMAD11	03	pMAD03
26	pMAD26	18	pMAD18	10	pMAD10	02	pMAD02
25	pMAD25	17	pMAD17	09	pMAD09	01	pMAD01
24	pMAD24	16	pMAD16	08	pMAD08	00	pMAD00

Bit(s)	rw	reset	Acronym	Definition
31-00	rw	0	(pMAD[31:00])	PHYSICAL MEMORY ADDRESS: This is the Physical Memory Address of the start of a physically contiguous memory region. It should be Qword aligned. If an I/O transfer, the I/O address of the source or destination of the data.

04h Transfer Length (pLEN)

pLEN			
15	pLEN15	07	pLEN07
14	pLEN14	06	pLEN06
13	pLEN13	05	pLEN05
12	pLEN12	04	pLEN04
11	pLEN11	03	pLEN03
10	pLEN10	02	pLEN02
09	pLEN09	01	pLEN01
08	pLEN08	00	pLEN00

Bit(s)	rw	reset	Acronym	Definition
15-00	rw	0	(pLEN[15:00])	TRANSFER LENGTH: If pPKT is cleared to zero, pLEN indicates the length, in Qwords, of the transfer segment. If pPKT is set to one and pDINT is cleared to zero, pLEN indicates the length, in words, of the packet command CDB to be transferred. If DINT is set to one, pLEN contains a 32-bit message.

07h Control Flags (pFLAG)

pFLAG	
31	pEND
30	pIOM
29	RSVD
28	pORD
27	pDINT
26	pPKT
25	pIGEX
24	RSVD

Bit(s)	rw	reset	Acronym	Definition
31	rw	0	(pEND)	APRD CHAIN END: End of APRD chain indicator. 1 = end of chain.
30	rw	0	(pIOM)	IO/MEMORY TRANSFER: Set to one for I/O transfer, cleared to zero for memory transfer.
29	r	0	*reserved*	RESERVED: Always reads 0.
28	rw	0	(pORD)	DATA TRANSFER METHOD: Set to one for Ulta-DMA, cleared to zero for DMA assisted PIO.
27	rw	0	(pDINT)	DIRECT INTERRUPT: Set to one to indicate that a Directed Interrupt is to be performed, if a non-error interrupt event occurs.
26	rw	0	(pPKT)	PACKET COMMAND POINTER: When set, indicates that pMAD is a pointer to a Packet. pLEN indicates the length of the packet command CDB to be transferred. PDINT shall be cleared to zero when pPKT is set to one.
25	rw	0	(pIGEX)	IGNORE DATA EXCESS: When set, indicates to ADMA that data excess occurring in this APRD is not an error. This is primarily used when reading the results from certain ATAPI packet commands that return unknown or odd lengths of data. cPSEXC will be set but no error interrupt will be generated and the IDMA continues exexution.
24	r	0	*reserved*	RESERVED: Always reads 0.

5.1 Absolute Maximum Ratings

Table 5-1 Absolute Maximum Ratings

Parameter		Minimum	Maximum	Units
Environment	Storage Temperature	-40	150	°C
	Operating Temperature	0	115	°C
	ESD Immunity	2.0 KV human model		
Voltage Levels	I/O Logic Power Supply (3.3V)	-0.3	3.9	V
	Core Logic Power Supply (1.8V)	-0.3	2.0	V
	Inputs	-0.3	Vcc+0.3	V
	Outputs	-0.3	Vcc+0.3	V

NOTE: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

5.2 Recommended Operating Conditions

Ta = 0°C to +115°C

VCC_3.3 = 3.3V ± 5%

VCC_1.8 = 1.8V ± 5%

GND = 0V

Table 5-2 Device Recommended Operating Conditions

Symbol	Parameter	Minimum	Maximum	Units	Conditions
VCC_3.3	I/O Logic Supply Voltage	3.14	3.46	V	
VCC_1.8	Core Logic Supply Voltage	1.71	1.89	V	
V_{IL}	Low level input voltage CMOS Input TTL Input	 -0.5 -0.5	 $0.3*V_{CC}$ 0.8	V	 Guaranteed Input Low Voltage
V_{IH}	High level input voltage CMOS Input TTL Input	 $0.7V*V_{CC}$ 2.0	 VDD + 0.5 VDD + 0.5	V	 Guaranteed Input High Voltage
T_J	Junction Temperature	0	100	°C	

5.3 General DC Characteristics

Ta = 0°C to +115°C

VCC_3.3 = 3.3V ± 5%

VCC_1.8 = 1.8V ± 5%

GND = 0V

Table 5-3 General DC Characteristics

Symbol	Parameter	Minimum	Typical	Maximum	Units
I_{IL}	Input Leakage Current	-10	-	10	µA
I_{OZ}	Tri-state Leakage Current	-10	-	10	µA
C_{IN}	Input Capacitance		3.1		pF
C_{OUT}	Output Capacitance	2.7	3.1	4.9	pF
C_{BID}	Bi-directional Buffer Capacitance	2.7	3.1	4.9	pF

5.4 PCI DC Parameters

Ta = 0°C to +75°C

VCC = 3.3V ± 5%

VCC_1.8 = 1.8V ± 5%

GND = 0V

Table 5-4 5V Signaling DC Parameters

Symbol	Parameter	Conditions	Minimum	Maximum	Units	Notes
V_{ih}	Input High Voltage		2.0	V_{cc} +0.5	V	
V_{il}	Input Low Voltage		-0.5	0.8	V	
I_{ih}	Input High Leakage Current	V_{in} = 2.7		70	µA	1
I_{il}	Input Low Leakage Current	V_{in} = 0.5		-70	µA	1
V_{oh}	Output High Voltage	I_{out} = -2 mA	2.4		V	
V_{ol}	Output Low Voltage	I_{out} = 3 mA, 6 mA		0.55	V	
C_{in}	Input Pin Capacitance			10	pF	
C_{clk}	**CLK** Pin Capacitance		5	12	pF	
C_{IDSEL}	**IDSEL** Pin Capacitance			8	pF	

Table 5-5 3.3V Signaling DC Parameters

Symbol	Parameter	Conditions	Minimum	Maximum	Units	Notes
V_{ih}	Input High Voltage		$0.5V_{CC}$	V_{CC} + 0.5	V	
V_{il}	Input Low Voltage		-0.5	$0.3V_{CC}$	V	
V_{ipu}	Input Pull-up Voltage		$0.7V_{CC}$	70	V	
I_{il}	Input Leakage Current	$0 < V_{in} < V_{CC}$		±10	µA	1
V_{oh}	Output High Voltage	I_{out} = -0.5 mA	$0.9V_{CC}$		V	
V_{ol}	Output Low Voltage	I_{out} = 1.5 mA		$0.1V_{CC}$	V	
C_{in}	Input Pin Capacitance			10	pF	
C_{clk}	**CLK** Pin Capacitance		5	12	pF	
C_{IDSEL}	**IDSEL** Pin Capacitance			8	pF	

NOTES:

1. Input currents include hi-Z output leakage for all bi-directional buffers with tri-state outputs (AD [31:0], C/BE [3:0] #, PAR, FRAME#, TRDY#, IRDY#, DEVSEL#, STOP#, PERR#, SERR#).

5.5 PCI AC Parameters

Ta = 0°C to +75°C

VCC = 3.3V ± 5%

VCC_1.8 = 1.8V ± 5%

GND = 0V

Table 5-6 5V Signaling AC Parameters

Symbol	Parameter	Conditions	Minimum	Maximum	Units	Notes
I_{oh} (AC)	Switching Current High	$0 < V_{out} \leq 1.4$	-44		mA	1
		$1.4 < V_{out} \leq 2.4$	$-44+(V_{out}-1.4)/0.024$		mA	1
		$3.1< V_{out}< V_{cc}$		Eqt'n A		1
	(Test Point)	$V_{out} = 3.1$		-142	mA	
I_{ol} (AC)	Switching Current Low	$V_{out} \geq 2.2$	95		mA	1
		$2.2 > V_{out} > 0.55$	$V_{out}/0.023$		mA	1
		$0.71 > V_{out} > 0$		Eqt'n B		1
	(Test Point)	$V_{out} = 0.71$		206	mA	
I_{cl}	Low Clamp Current	$-5 < V_{in} \leq -1$	$-25+(V_{in}+1)/0.015$		mA	
$slew_r$	Output Rise Slew Rate	0.4V to 2.4V load	1	5	V/ns	
$slew_r$	Output Fall Slew Rate	2.4V to 0.4V load	1	5	V/ns	

Table 5-7 3.3V Signaling AC Parameters

Symbol	Parameter	Conditions	Minimum	Maximum	Units	Notes
I_{oh} (AC)	Switching Current High	$0 < V_{out} \leq 0.3V_{CC}$	$-12V_{CC}$		mA	1
		$0.3V_{CC} < V_{out} \leq 0.9V_{CC}$	$-17.1(V_{CC}-Vout)$		mA	1
		$0.7V_{CC} < V_{out} < V_{cc}$		Eqt'n C		1
	(Test Point)	$V_{out} = 0.7V_{CC}$		$-32V_{CC}$	mA	
I_{ol} (AC)	Switching Current Low	$V_{CC} > V_{out} \geq 0.6V_{CC}$	$16V_{CC}$		mA	1
		$0.6V_{CC} > V_{out} > 0.1V_{CC}$	$26.7V_{out}$		mA	1
		$0.18V_{CC} > V_{out} > 0$		Eqt'n D		1
	(Test Point)	$V_{out} = 0.18V_{CC}$		$-38V_{CC}$	mA	
I_{cl}	Low Clamp Current	$-3 < V_{in} \leq -1$	$-25+(V_{in}+1)/0.015$		mA	
I_{ch}	High Clamp Current	$V_{CC}+4 > V_{in} \geq V_{CC}+1$	$25+(V_{in}-V_{CC}-1)/0.015$		mA	
$slew_r$	Output Rise Slew Rate	$0.2V_{CC}$ - $0.6V_{CC}$ load	1	4	V/ns	
$slew_f$	Output Fall Slew Rate	$0.6V_{CC}$ - $0.2V_{CC}$ load	1	4	V/ns	

NOTES:

1. Refer to the V/I curves. This specification does not apply to CLK and RST# which are system outputs. "Switching Current High" specifications are not relevant to SERR#, and INTA# which are open drain outputs.

6.1 General Timing

Timing values in the ‘Preliminary’ Data Sheet are derived from timing simulation. After AC Characterization of the device, the Data Sheet’s timing values reflect characterization data (unless noted otherwise), at which time ‘Preliminary’ is removed from the Data Sheet title and footers.

6.1.1 AC Input/Output Timing Parameters

Symbol	Parameter	Values Min	Typ	Max	Units	Notes
TF	Signal Fall Time			5	ns	Cap loading @ 20pF
TR	Signal Rise Time			5	ns	

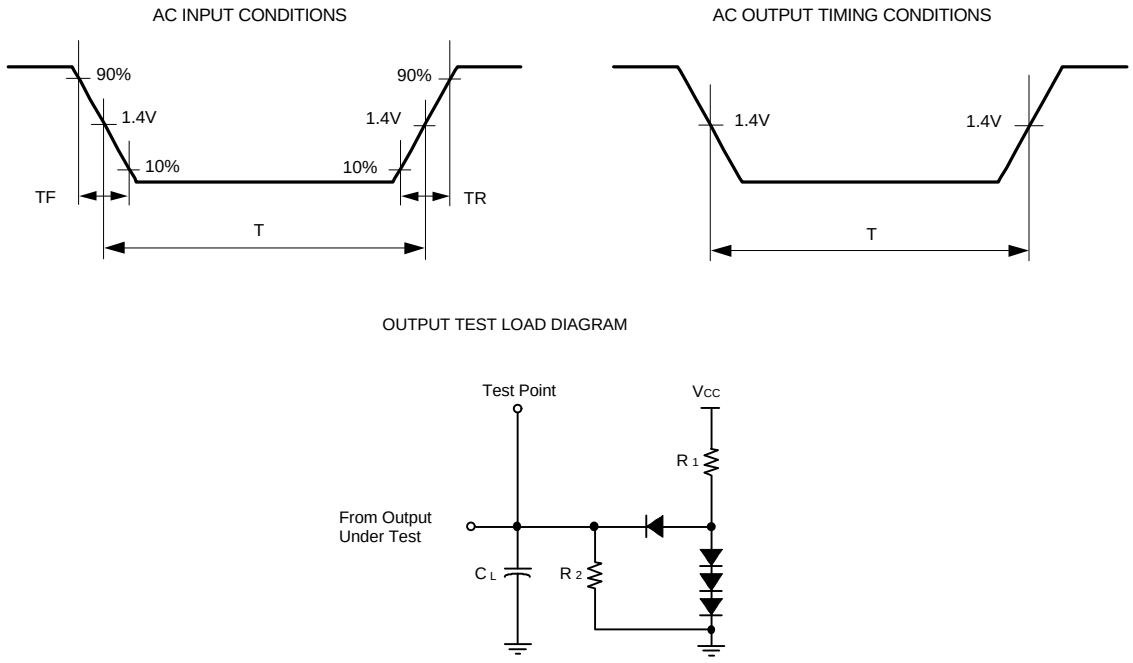


Figure 6-1 AC Input/Output Timing

6.1.2 Clock Timing Parameters

		66 MHz		33 MHz			
Symbol	**Parameter**	**Min**	**Max**	**Min**	**Max**	**Units**	**Notes**
T_{CYC}	Clock (PCLK) Period	15	30	30	∞	ns	
T_{HIGH}	Clock High Pulse Width	6		11		ns	
T_{LOW}	Clock Low Pulse Width	6		11		ns	
-	Clock Slew Rate	1.5	4	1	4	V/ns	1
Spread Spectrum Requirements							
F_{MOD}	Modulation Frequency	30	33			kHz	
F_{SPREAD}	Frequency Spread	-1	0			%	

1. Rise and fall times are specified in terms of the edge rate measured in V/ns.

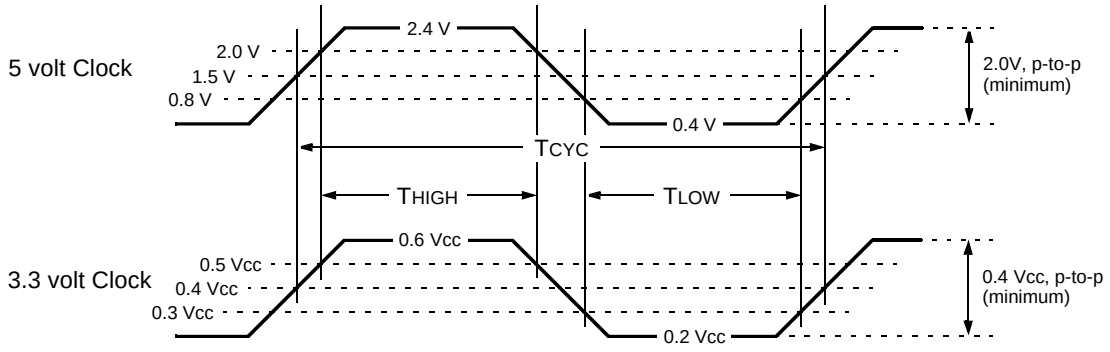


Figure 6-2 Clock Timing

6.1.3 Clock Skew Timing Parameters

Symbol	**Parameter**	**66 MHz 3.3V Signaling**	**33 MHz 3.3V Signaling**	**Units**	**Notes**
V_{TEST}	Test Voltage	0.4 V_{CC}	0.4 V_{CC}	V	
T_{SKEW}	Clock Skew	1 (max)	2 (max)	ns	

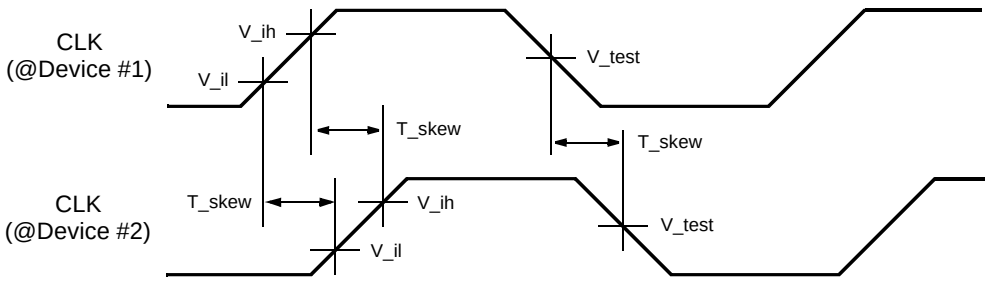


Figure 6-3 Clock Skew Timing

6.2 PCI Bus Timing

Shown below is the timing diagrams that applies to the 66 MHz and 33 MHz timing parameter table (refer to Table 6-1).

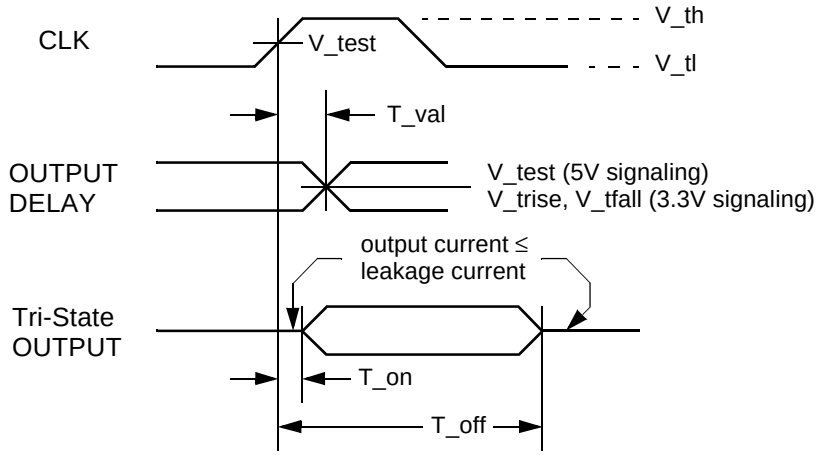


Figure 6-4 Output Timing Measurement Conditions

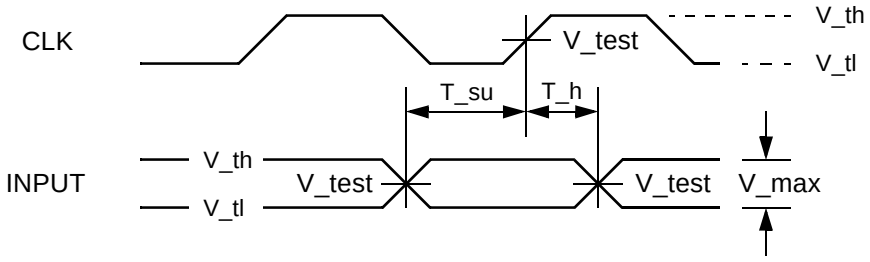


Figure 6-5 Input Timing Measurement Conditions

Table 6-1 PCI Bus 66 MHz and 33 MHz Timing Parameters

		66 MHz		33 MHz			
Symbol	**Parameter**	**Min**	**Max**	**Min**	**Max**	**Units**	**Notes**
T_{VAL}	CLK to Signal Valid Delay - bused signals	2	6	2	11	ns	1
T_{VAL}(ptp)	CLK to Signal Valid Delay - point to point signals	2	6	2	12	ns	1
T_{ON}	Float to Active Delay	2		2		ns	
T_{OFF}	Active to Float Delay		14		28	ns	
T_{SU}	Input Set up Time to CLK - bused signals	3		7		ns	1
T_{SU}(ptp)	Input Set up Time to CLK - point to point signals	5		10, 12		ns	1
T_{H}	Input Hold Time from CLK	0		0		ns	
T_{RST}	Reset Active Time after power stable	1		1		ms	
$T_{RST-CLK}$	Reset Active Time After CLK stable	100		100		µs	
$T_{RST-OFF}$	Reset Active to output float delay		40		40	ns	
T_{RRSU}	REQ64# ti RST# setup time	$10T_{CYC}$		$10T_{CYC}$		ns	
T_{RRH}	RST# to REQ64# hold time		50		50	ns	
T_{RHFA}	RST# high to first Configuration access	2^{25}		2^{25}		clocks	
T_{RGFF}	RST# high to first FRAME# assertion	5		5		clocks	

NOTES:

1. PREQ# and PGNT# are point-to-point signals, and have different input setup times than do bused signals. PREQ# and PGNT# have a setup of 5ns at 66MHz and 12ns and 10ns respectively at 33MHz. All other signals are bused.

7.1 INIC-1622 TQFP Packaging Specifications

Figure 7-1 shows the physical outline of the 128-pin TQFP package. Table 7-1 shows the package's dimensions.

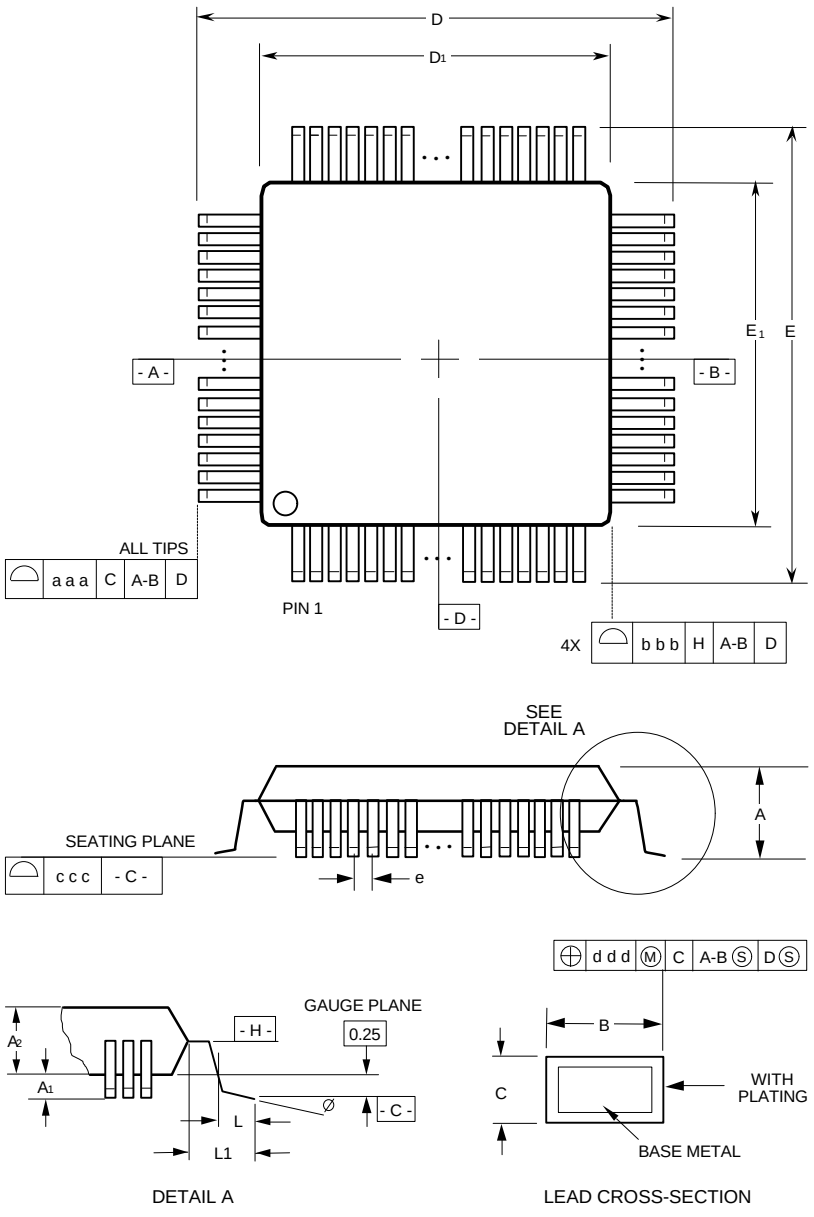


Figure 7-1 128 Pin TQFP Package Outline

Table 7-1 128-Pin TQFP Package Dimensions

SYMBOL	MM			INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	-	-	1.20	-	-	0.047
A1	0.05	-	0.15	0.002	-	0.006
A2	0.95	1.00	1.05	0.037	0.039	0.041
B	0.13	0.18	0.23	0.005	0.007	0.09
C	0.09	-	0.20	0.004	-	0.008
D	16.00 BSC			0.866 BSC		
D1	14.00 BSC			0.787 BSC		
E	16.00 BSC			0.866 BSC		
E1	14.00 BSC			0.787 BSC		
e	0.40 BSC			0.016 BSC		
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF			0.039 REF		
Ø	0 deg	3.5 deg	7 deg	0 deg	3.5 deg	7 deg
aaa	0.20			0.008		
bbb	0.20			0.008		
ccc	0.08			0.003		
ddd	0.08			0.003		

**NOTES:*

1. *Dimensions per JEDEC specification MS-026 issue C.*
2. *Controlling dimensions are in millimeters (mm).*
3. *The top package body size may be smaller than the bottom package body size by as much as 0.15 mm.*
4. *Datums A-B and -D- to be determined at datum plane -H-.*
5. *Reference plane -H- is located at mold parting line and is coincident with bottom of lead where it exits plastic body.*
6. *Dimensions D and E to be determined at seating plane -C-.*
7. *Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25 mm per side. Dimensions D1 and E1 are maximum plastic body size dimensions including mold mismatch.*
8. *Dimension B does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum B dimension by more than 0.08 mm. Dambar can not be located on the lower radius or the foot. Minimum space between protrusion and an adjacent lead is 0.07 mm.*
9. *The dimensions shown in lead cross-section apply to the flat section of the lead between 0.10 mm and 0.25 mm from the lead tip.*
10. *Dimension A1 is defined as the distance from the seating plane to the lowest point of the package body.*
11. *Solder plate thickness shall be 200 microinches minimum.*

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