



STD38NH02L STD38NH02L-1

N-channel 24V - 0.011Ω - 38A - DPAK/IPAK
STripFET™ III Power MOSFET

General features

| Type | V _{DSS} | R _{DS(on)} | I _D |
|--------------|------------------|---------------------|----------------|
| STD38NH02L-1 | 24V | <0.0135Ω | 38A |
| STD38NH02L | 24V | <0.0135Ω | 38A |

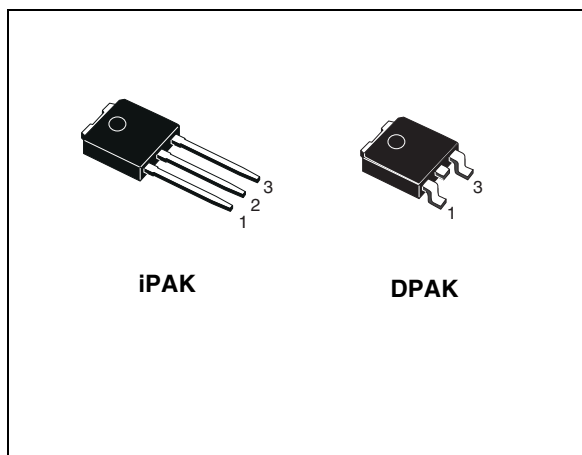
- Logic level device
- R_{DS(ON)} * Q_G Industry's benchmark
- Conduction losses reduced
- Switching losses reduced
- Low threshold drive

Description

This device utilizes the latest advanced design rules of ST's proprietary STripFET™ technology. This is suitable for the most demanding DC-DC converter application where high efficiency is to be achieved.

Applications

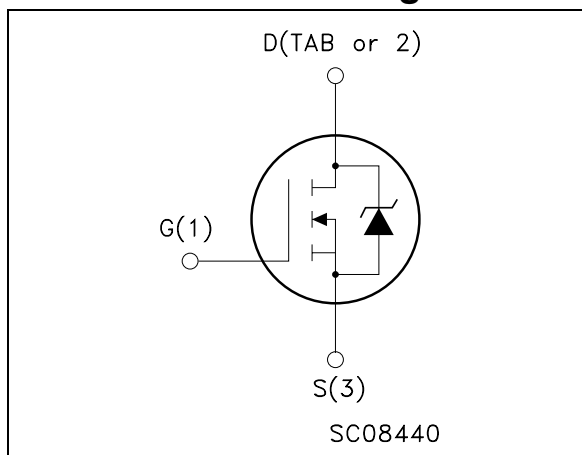
- Switching application



Order codes

| Part number | Marking | Package | Packaging |
|--------------|----------|---------|-------------|
| STD38NH02L-1 | D38NH02L | IPAK | Tube |
| STD38NH02LT4 | D38NH02L | DPAK | Tape & reel |

Internal schematic diagram



Contents

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1 Electrical ratings

Table 1. Absolute maximum ratings

| Symbol | Parameter | Value | Unit |
|--------------------------|--|------------|-----------------------|
| $V_{\text{spike}}^{(1)}$ | Drain-source voltage rating | 30 | V |
| V_{DS} | Drain-source voltage ($V_{\text{GS}} = 0$) | 24 | V |
| V_{DGR} | Drain-gate voltage ($R_{\text{GS}} = 20 \text{ k}\Omega$) | 24 | V |
| V_{GS} | Gate- source voltage | ± 20 | V |
| I_{D} | Drain current (continuous) at $T_{\text{C}} = 25^{\circ}\text{C}$ | 38 | A |
| I_{D} | Drain current (continuous) at $T_{\text{C}} = 100^{\circ}\text{C}$ | 27 | A |
| $I_{\text{DM}}^{(2)}$ | Drain current (pulsed) | 152 | A |
| P_{tot} | Total dissipation at $T_{\text{C}} = 25^{\circ}\text{C}$ | 40 | W |
| | Derating Factor | 0.27 | W/ $^{\circ}\text{C}$ |
| $E_{\text{AS}}^{(3)}$ | Single pulse avalanche energy | 250 | mJ |
| T_{stg} | Storage temperature | -55 to 175 | $^{\circ}\text{C}$ |
| T_{j} | Max. operating junction temperature | | |

1. Guaranteed when external $R_{\text{g}}=4.7 \Omega$ and $t_{\text{f}} < t_{\text{fmax}}$.

2. Pulse width limited by safe operating area.

3. Starting $T_{\text{j}} = 25^{\circ}\text{C}$, $I_{\text{D}} = 19\text{A}$, $V_{\text{DD}} = 18\text{V}$

Table 2. Thermal data

| | | | |
|-----------------------|--|------|-----------------------------|
| $R_{\text{thj-case}}$ | Thermal resistance junction-case max | 3.75 | $^{\circ}\text{C}/\text{W}$ |
| $R_{\text{thj-amb}}$ | Thermal resistance junction-ambient max | 100 | $^{\circ}\text{C}/\text{W}$ |
| T_{J} | Maximum lead temperature for soldering purpose | 275 | $^{\circ}\text{C}$ |

2 Electrical characteristics

($T_{CASE}=25^{\circ}C$ unless otherwise specified)

Table 3. On/off states

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---------------|--|--|------|----------------|-----------------|----------------------|
| $V_{(BR)DSS}$ | Drain-source breakdown voltage | $I_D = 25mA, V_{GS} = 0$ | 24 | | | V |
| I_{DSS} | Zero gate voltage drain current ($V_{GS} = 0$) | $V_{DS} = 20V$ $V_{DS} = 20V, T_C = 125^{\circ}C$ | | | 1 10 | μA μA |
| I_{GSS} | Gate-body leakage current ($V_{DS} = 0$) | $V_{GS} = \pm 20V$ | | | ± 100 | nA |
| $V_{GS(th)}$ | Gate threshold voltage | $V_{DS} = V_{GS}, I_D = 250\mu A$ | 1 | 1.8 | 2.5 | V |
| $R_{DS(on)}$ | Static drain-source on resistance | $V_{GS} = 10V, I_D = 19A$ $V_{GS} = 5V, I_D = 9.5A$ | | 0.011 0.015 | 0.0135 0.025 | Ω Ω |

Table 4. Dynamic

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|--|------|---------------------|------|----------------------|
| $g_{fs}^{(1)}$ | Forward transconductance | $V_{DS} = 10V, I_D = 19A$ | | 19 | | S |
| C_{iss} C_{oss} C_{rss} | Input capacitance Output capacitance Reverse transfer capacitance | $V_{DS} = 25V, f = 1MHz,$ $V_{GS} = 0$ | | 1070 305 45 | | pF pF pF |
| R_G | Gate Input Resistance | $f = 1 MHz$ Gate DC Bias = 0 Test Signal Level = 20 mV Open Drain | | 1 | | Ω |
| $t_{d(on)}$ t_r $t_{d(off)}$ t_f | Turn-on delay time Rise time Turn-off delay time Fall time | $V_{DD} = 10V, I_D = 19A$ $R_G = 4.7\Omega, V_{GS} = 10V$ (see Figure 13) | | 7 62 25 12 | | ns ns ns ns |
| Q_g Q_{gs} Q_{gd} | Total gate charge Gate-source charge Gate-drain charge | $0.44V \leq V_{DD} \leq 10V,$ $I_D = 38A,$ $V_{GS} = 10V, R_G = 4.7\Omega$ (see Figure 14) | | 18 4 2.5 | 24 | nC nC nC |
| $Q_{oss}^{(2)}$ | Output charge | $V_{DS} = 16 V, V_{GS} = 0 V$ | | 6.5 | | nC |

1. Pulsed: Pulse duration = 300 μs , duty cycle 1.5 %.

2. $Q_{oss} = C_{oss} \cdot \Delta V_{in}$, $C_{oss} = C_{gd} + C_{ds}$. See [Chapter 4: Appendix A](#)

Table 5. Source drain diode

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|-----------------------------------|--|--|------|-----------------|-----------|---------------|
| I_{SD} $I_{SDM}^{(1)}$ | Source-drain current Source-drain current (pulsed) | | | | 38 152 | A A |
| $V_{SD}^{(2)}$ | Forward on voltage | $I_{SD} = 19A, V_{GS} = 0$ | | | 1.3 | V |
| t_{rr} Q_{rr} I_{RRM} | Reverse recovery time Reverse recovery charge Reverse recovery current | $I_{SD} = 38A, di/dt = 100A/\mu s,$ $V_{DD} = 18V, T_j = 150^\circ C$ (see Figure 15) | | 27 22 1.6 | | ns nC A |

1. Pulse width limited by safe operating area.
2. Pulsed: Pulse duration = 300 μs , duty cycle 1.5 %

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

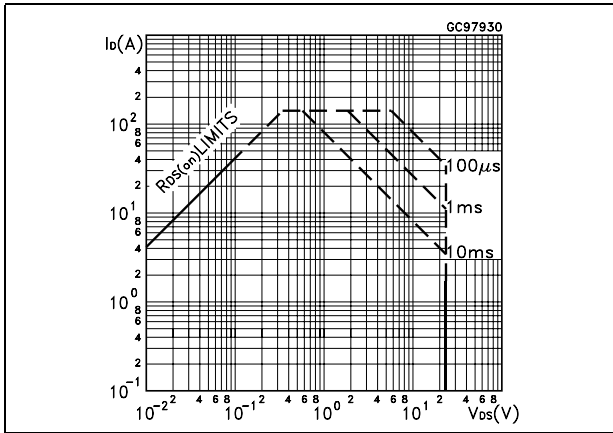


Figure 2. Thermal impedance

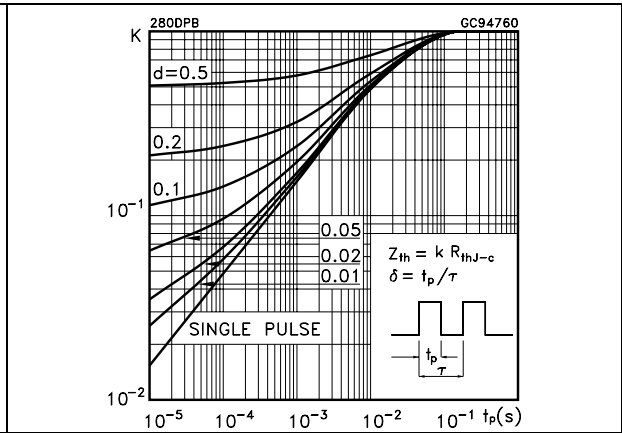


Figure 3. Output characteristics

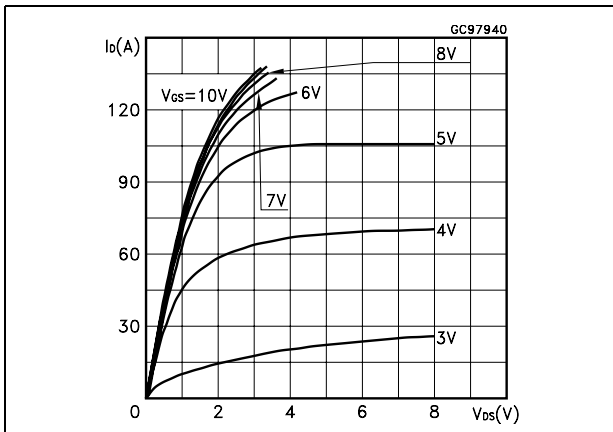


Figure 4. Transfer characteristics

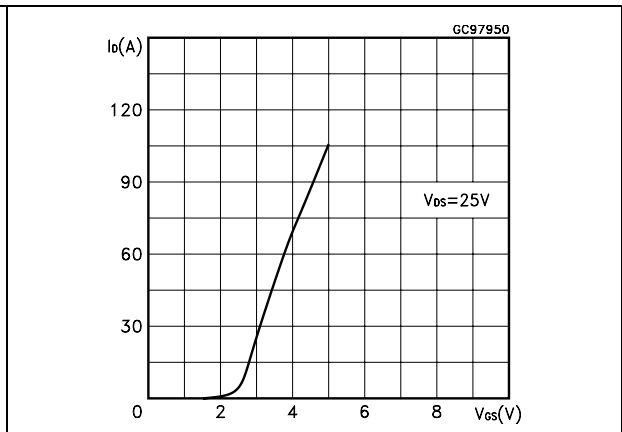


Figure 5. Transconductance

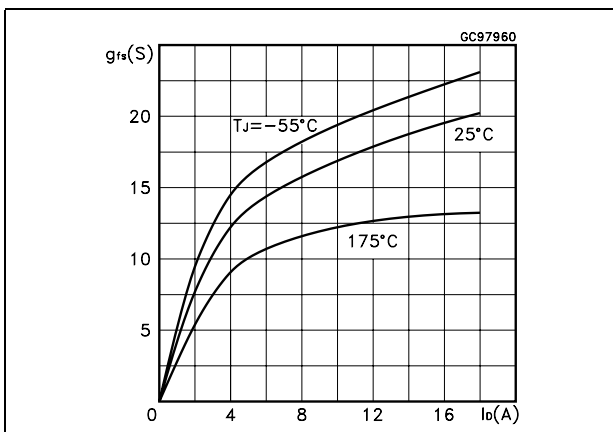


Figure 6. Static drain-source on resistance

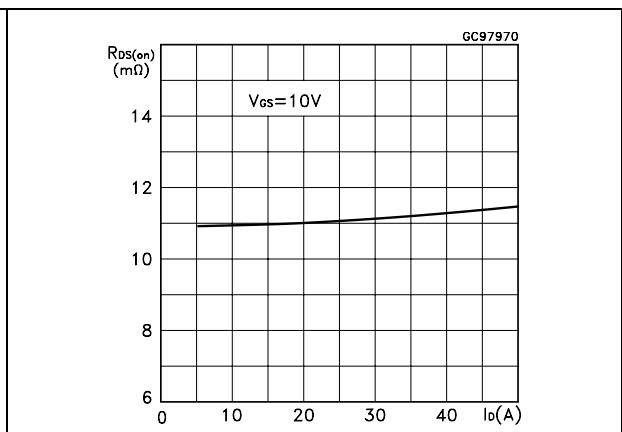


Figure 7. Gate charge vs gate-source voltage Figure 8. Capacitance variations

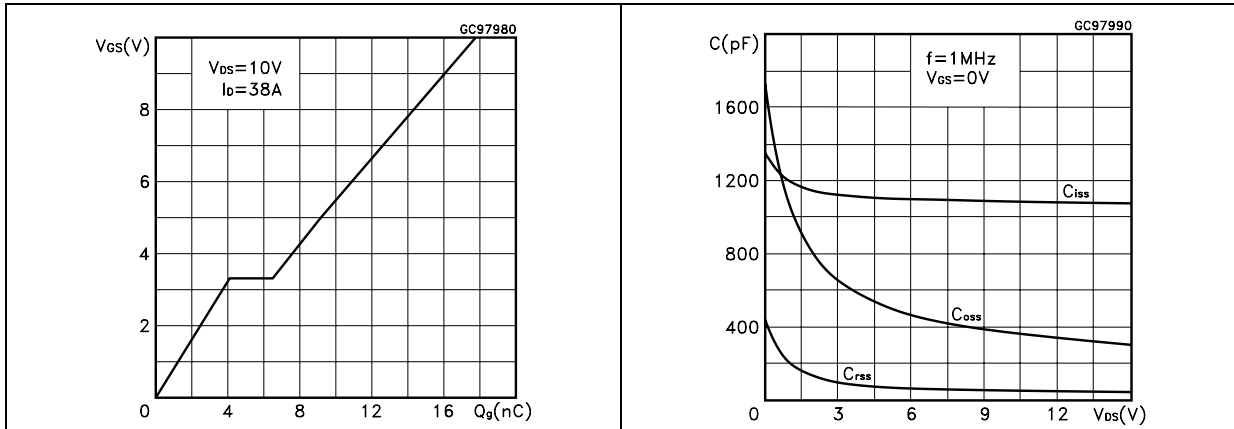


Figure 9. Normalized gate threshold voltage vs temperature Figure 10. Normalized on resistance vs temperature

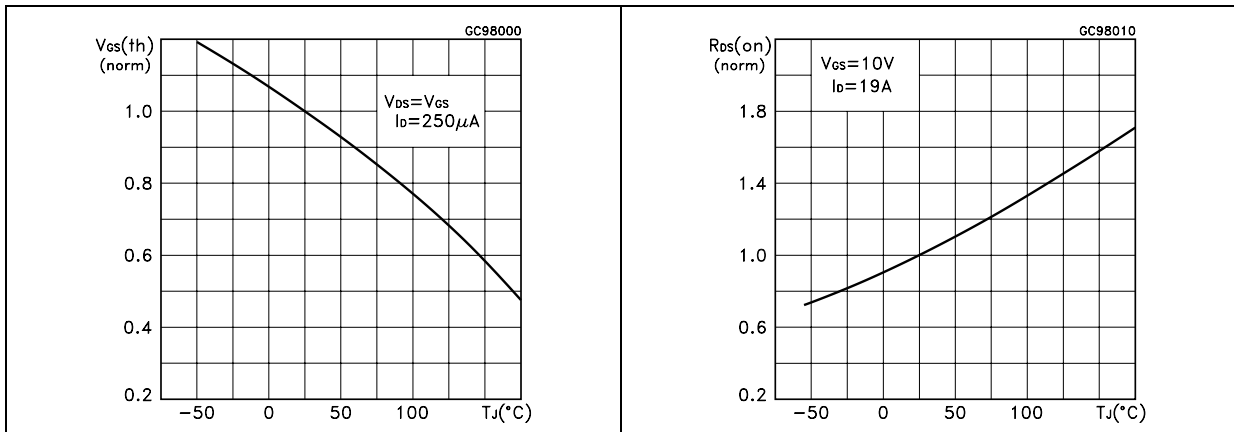
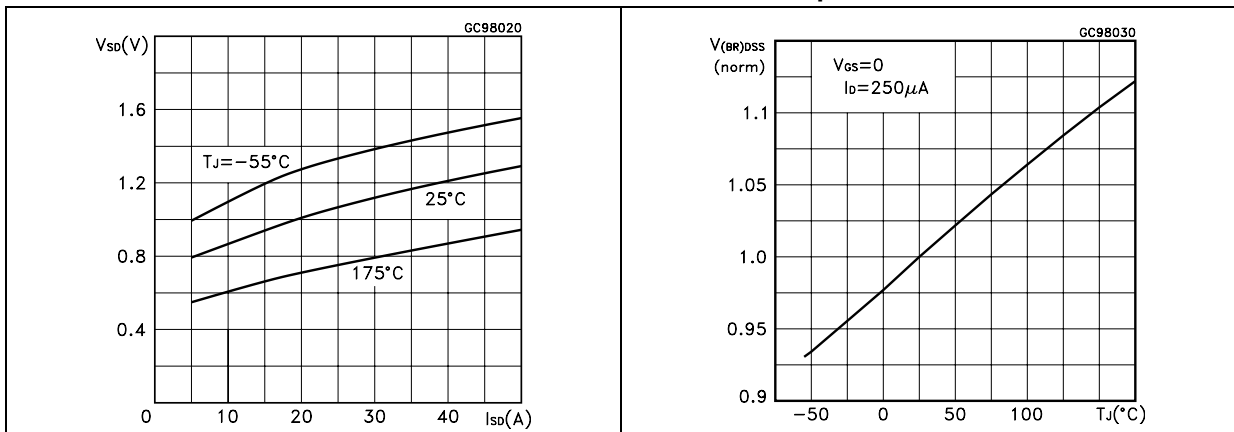


Figure 11. Source-drain diode forward characteristics Figure 12. Normalized breakdown voltage vs temperature



3 Test circuit

Figure 13. Switching times test circuit for resistive load

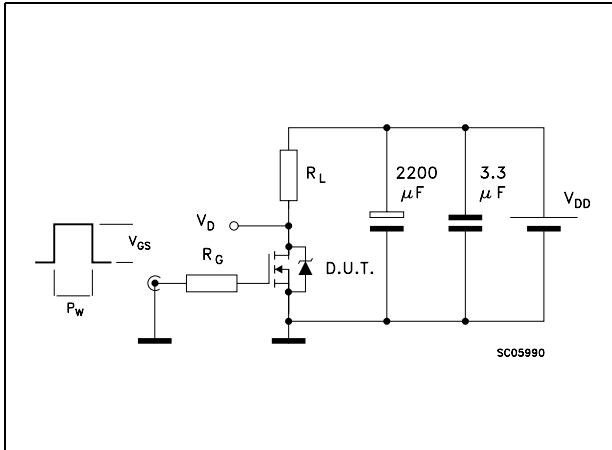


Figure 14. Gate charge test circuit



Figure 15. Test circuit for inductive load switching and diode recovery times

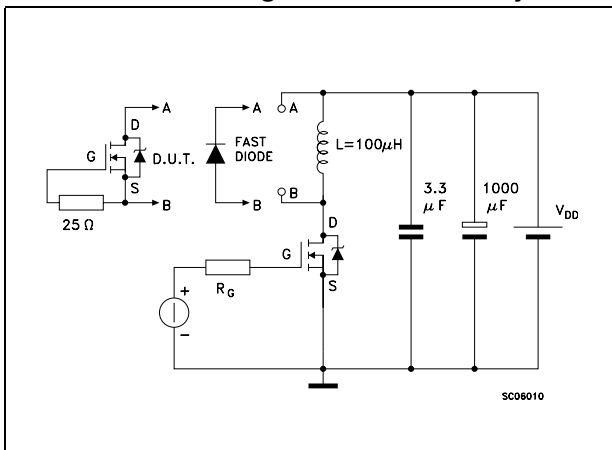


Figure 16. Unclamped Inductive load test circuit

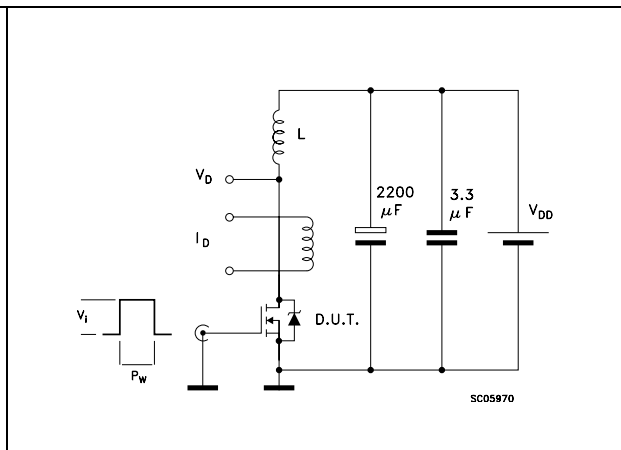


Figure 17. Unclamped inductive waveform

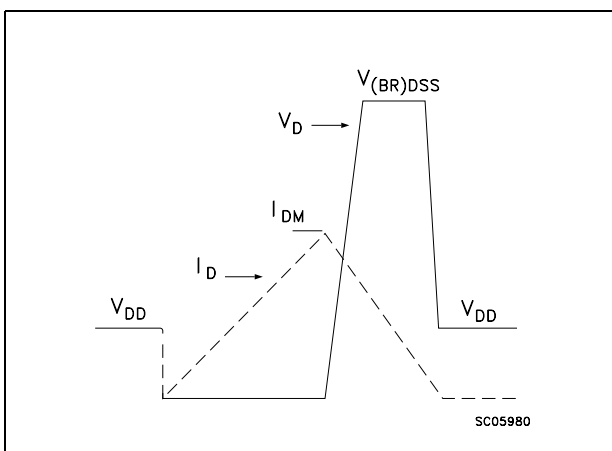
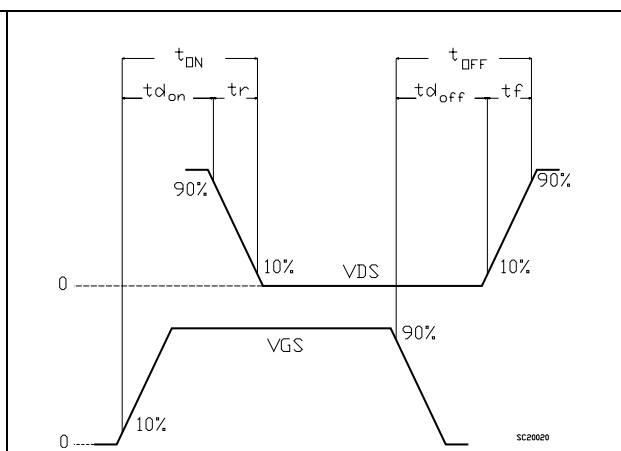
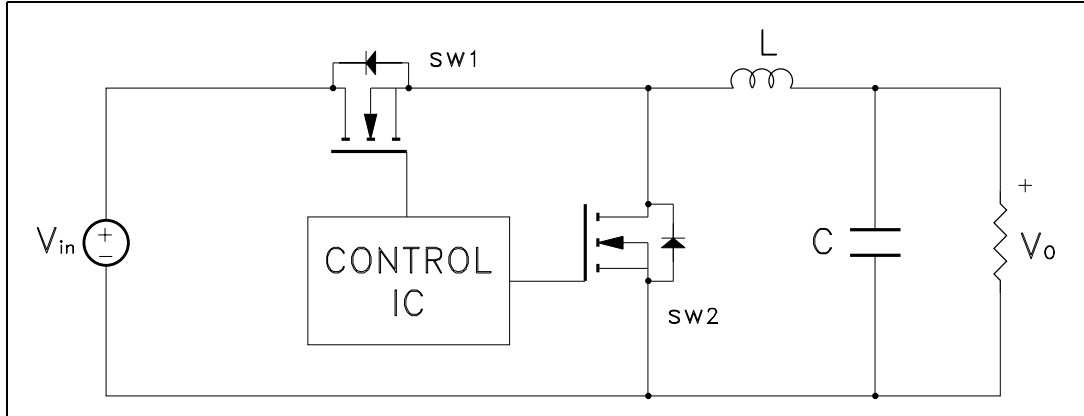


Figure 18. Switching time waveform



4 Appendix A

Figure 19. Buck converter: power losses estimation



The power losses associated with the FETs in a synchronous buck converter can be estimated using the equations shown in the table below. The formulas give a good approximation, for the sake of performance comparison, of how different pairs of devices affect the converter efficiency. However a very important parameter, the working temperature, is not considered. The real device behavior is really dependent on how the heat generated inside the devices is removed to allow for a safer working junction temperature.

- The low side (SW2) device requires:
 - Very low $R_{DS(on)}$ to reduce conduction losses
 - Small Q_{gl} to reduce the gate charge losses
 - Small C_{oss} to reduce losses due to output capacitance
 - Small Q_{rr} to reduce losses on SW1 during its turn-on
 - The C_{gd}/C_{gs} ratio lower than V_{th}/V_{gg} ratio especially with low drain to source voltage to avoid the cross conduction phenomenon;
- The high side (SW1) device requires:
 - Small R_g and L_s to allow higher gate current peak and to limit the voltage feedback on the gate
 - Small Q_g to have a faster commutation and to reduce gate charge losses
 - Low $R_{DS(on)}$ to reduce the conduction losses.

Table 6. Power losses calculation

| | | High side switching (SW1) | Low side switch (SW2) |
|------------------------|--------------|--|--|
| Pconduction | | $R_{DS(on)SW1} * I_L^2 * \delta$ | $R_{DS(on)SW2} * I_L^2 * (1 - \delta)$ |
| Pswitching | | $V_{in} * (Q_{gsth(SW1)} + Q_{gd(SW1)}) * f * \frac{I_L}{I_g}$ | Zero Voltage Switching |
| Pdiode | Recovery (1) | Not applicable | $V_{in} * Q_{rr(SW2)} * f$ |
| | Conduction | Not applicable | $V_{f(SW2)} * I_L * t_{deadtime} * f$ |
| Pgate(Q _G) | | $Q_{g(SW1)} * V_{gg} * f$ | $Q_{gls(SW2)} * V_{gg} * f$ |
| P _{Qoss} | | $\frac{V_{in} * Q_{oss(SW1)} * f}{2}$ | $\frac{V_{in} * Q_{oss(SW2)} * f}{2}$ |

1. Dissipated by SW1 during turn-on

Table 7. Parameters meaning

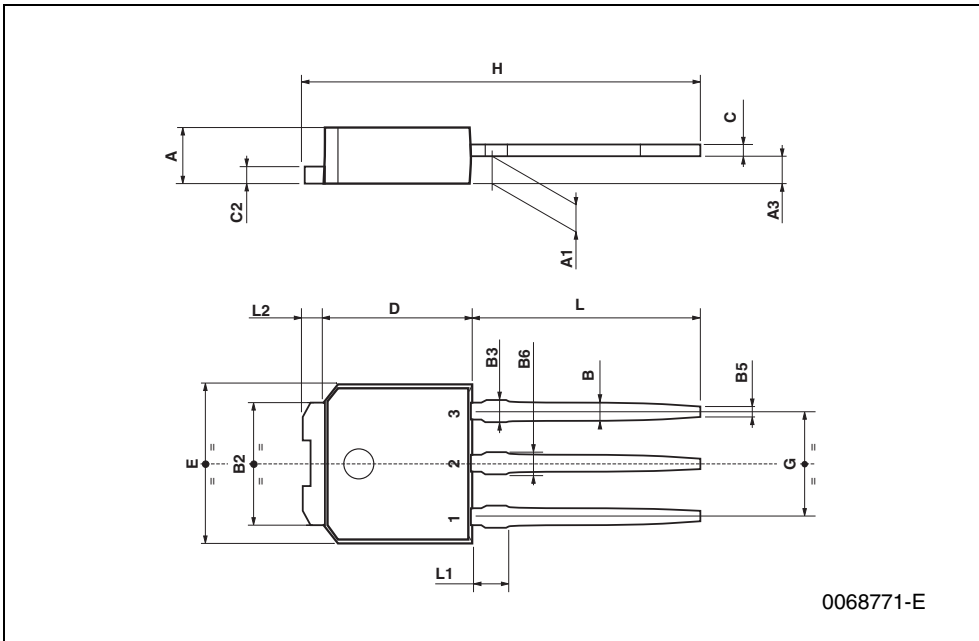
| Parameter | Meaning |
|-------------------|--|
| d | Duty-cycle |
| Q _{gsth} | Post threshold gate charge |
| Q _{gls} | Third quadrant gate charge |
| Pconduction | On state losses |
| Pswitching | On-off transition losses |
| Pdiode | Conduction and reverse recovery diode losses |
| Pgate | Gate drive losses |
| P _{Qoss} | Output capacitance losses |

5 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

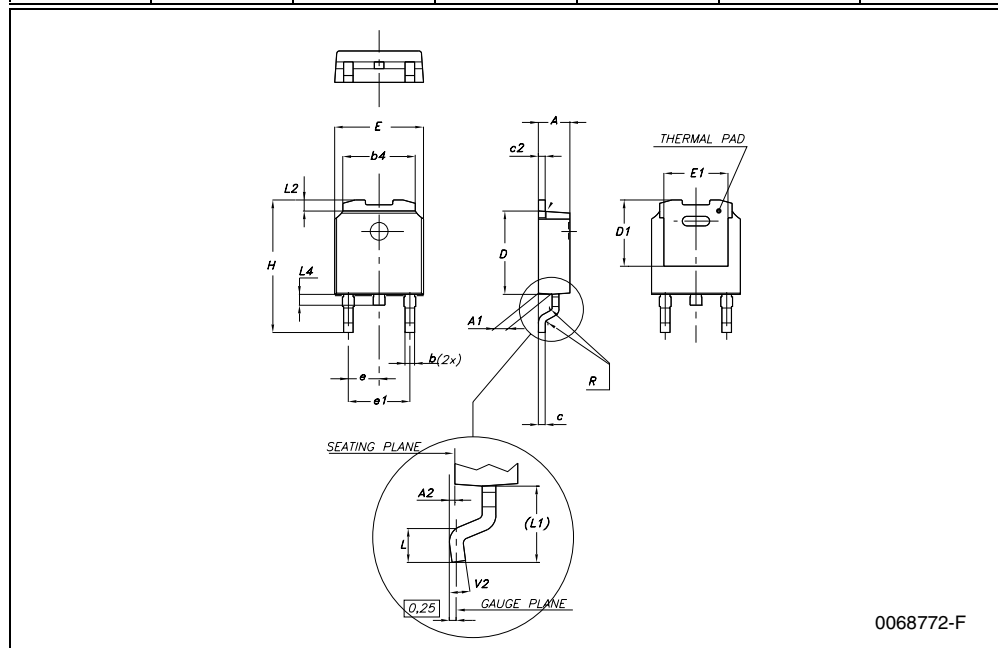
TO-251 (IPAK) MECHANICAL DATA

| DIM. | mm | | | inch | | |
|------|------|------|------|-------|-------|-------|
| | MIN. | TYP. | MAX. | MIN. | TYP. | MAX. |
| A | 2.2 | | 2.4 | 0.086 | | 0.094 |
| A1 | 0.9 | | 1.1 | 0.035 | | 0.043 |
| A3 | 0.7 | | 1.3 | 0.027 | | 0.051 |
| B | 0.64 | | 0.9 | 0.025 | | 0.031 |
| B2 | 5.2 | | 5.4 | 0.204 | | 0.212 |
| B3 | | | 0.85 | | | 0.033 |
| B5 | | 0.3 | | | 0.012 | |
| B6 | | | 0.95 | | | 0.037 |
| C | 0.45 | | 0.6 | 0.017 | | 0.023 |
| C2 | 0.48 | | 0.6 | 0.019 | | 0.023 |
| D | 6 | | 6.2 | 0.236 | | 0.244 |
| E | 6.4 | | 6.6 | 0.252 | | 0.260 |
| G | 4.4 | | 4.6 | 0.173 | | 0.181 |
| H | 15.9 | | 16.3 | 0.626 | | 0.641 |
| L | 9 | | 9.4 | 0.354 | | 0.370 |
| L1 | 0.8 | | 1.2 | 0.031 | | 0.047 |
| L2 | | 0.8 | 1 | | 0.031 | 0.039 |



DPAK MECHANICAL DATA

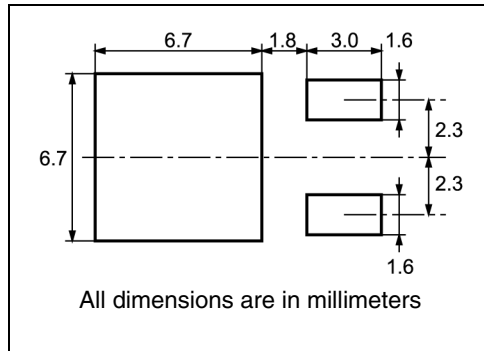
| DIM. | mm. | | | inch | | |
|------|------|------|------|-------|-------|-------|
| | MIN. | TYP. | MAX. | MIN. | TYP. | MAX. |
| A | 2.2 | | 2.4 | 0.086 | | 0.094 |
| A1 | 0.9 | | 1.1 | 0.035 | | 0.043 |
| A2 | 0.03 | | 0.23 | 0.001 | | 0.009 |
| B | 0.64 | | 0.9 | 0.025 | | 0.035 |
| b4 | 5.2 | | 5.4 | 0.204 | | 0.212 |
| C | 0.45 | | 0.6 | 0.017 | | 0.023 |
| C2 | 0.48 | | 0.6 | 0.019 | | 0.023 |
| D | 6 | | 6.2 | 0.236 | | 0.244 |
| D1 | | 5.1 | | | 0.200 | |
| E | 6.4 | | 6.6 | 0.252 | | 0.260 |
| E1 | | 4.7 | | | 0.185 | |
| e | | 2.28 | | | 0.090 | |
| e1 | 4.4 | | 4.6 | 0.173 | | 0.181 |
| H | 9.35 | | 10.1 | 0.368 | | 0.397 |
| L | 1 | | | 0.039 | | |
| (L1) | | 2.8 | | | 0.110 | |
| L2 | | 0.8 | | | 0.031 | |
| L4 | 0.6 | | 1 | 0.023 | | 0.039 |
| R | | 0.2 | | | 0.008 | |
| V2 | 0° | | 8° | 0° | | 8° |



0068772-F

6 Packing mechanical data

DPAK FOOTPRINT



TAPE AND REEL SHIPMENT

40 mm min. Access hole at slot location

Full radius

Tape slot in core for tape start 2.5mm min. width

G measured at hub

REEL MECHANICAL DATA

| DIM. | mm | | inch | |
|------|------|------|-------|--------|
| | MIN. | MAX. | MIN. | MAX. |
| A | | 330 | | 12.992 |
| B | 1.5 | | 0.059 | |
| C | 12.8 | 13.2 | 0.504 | 0.520 |
| D | 20.2 | | 0.795 | |
| G | 16.4 | 18.4 | 0.645 | 0.724 |
| N | 50 | | 1.968 | |
| T | | 22.4 | | 0.881 |

TAPE MECHANICAL DATA

| DIM. | mm | | inch | |
|------|------|------|-------|-------|
| | MIN. | MAX. | MIN. | MAX. |
| A0 | 6.8 | 7 | 0.267 | 0.275 |
| B0 | 10.4 | 10.6 | 0.409 | 0.417 |
| B1 | | 12.1 | | 0.476 |
| D | 1.5 | 1.6 | 0.059 | 0.063 |
| D1 | 1.5 | | 0.059 | |
| E | 1.65 | 1.85 | 0.065 | 0.073 |
| F | 7.4 | 7.6 | 0.291 | 0.299 |
| K0 | 2.55 | 2.75 | 0.100 | 0.108 |
| P0 | 3.9 | 4.1 | 0.153 | 0.161 |
| P1 | 7.9 | 8.1 | 0.311 | 0.319 |
| P2 | 1.9 | 2.1 | 0.075 | 0.082 |
| R | 40 | | 1.574 | |
| W | 15.7 | 16.3 | 0.618 | 0.641 |

TOP COVER TAPE

User Direction of Feed

Center line of cavity

Bending radius R min.

FEED DIRECTION

For machine ref. only including draft and radii concentric around B0

10 pitches cumulative tolerance on tape +/- 0.2 mm

7 Revision history

Table 8. Revision history

| Date | Revision | Changes |
|-------------|-----------------|---------------------------------|
| 21-Jun-2004 | 7 | Preliminary version |
| 11-Jul-2006 | 8 | New template, no content change |

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