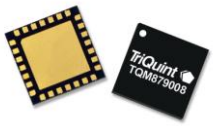
TQM879008

1.5-2.7GHz ½ W Digital Variable Gain Amplifier

Applications

- 3G / 4G Wireless Infrastructure
- CDMA, WCDMA, LTE
- Repeaters

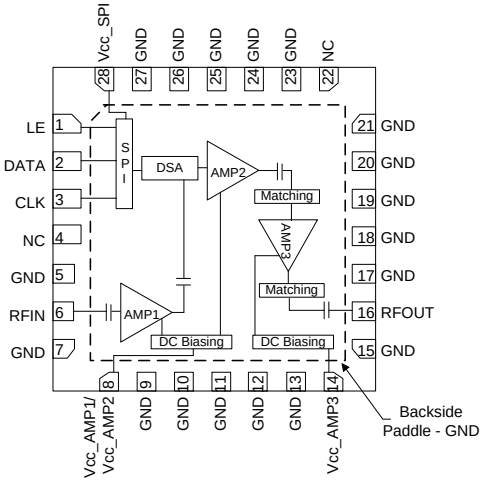


28-pin 6x6mm leadless SMT package

Product Features

- 1.5-2.7 GHz Frequency Range
- 41.1 dB Maximum Gain at 2.5 GHz
- 31.5 dB Gain Range in 0.5 dB Steps
- +47.5 dBm Output IP3
- +27.3 dBm Output P1dB
- Fully Internally Matched Module
- Integrated Blocking Capacitors, Bias Inductors
- 3-wire SPI Control Programming

Functional Block Diagram



General Description

The TQM879008 is a digital variable gain amplifier (DVGA) featuring high linearity over the entire gain control range. This amplifier module integrates two gain blocks, a digital-step attenuator (DSA), and a high linearity ½ W amplifier. The module has the added feature of integrating all matching components, bias chokes and blocking capacitors. The internal 6-bit DSA provides a 31.5 dB gain control range in 0.5 dB steps, and is controlled with a serial periphery interface (SPI™).

The TQM879008 features variable gain from 10 dB to 41.1dB at 2.5 GHz, +47.5 dBm output IP3, and +27.3 dBm P1dB. The module operates from a single +5V supply and is available in a compact 28-pin 6x6 mm leadless SMT package.

The TQM879008 is pin compatible with the TQM829007 (0.7-1.0GHz, 0.25W DVGA) and TQM879006 (1.4-2.7GHz, 0.25W DVGA). This allows one to size the right type of device for specific system level requirements as well as making the DVGA family ideal for applications where a common PCB layout is used for different frequency bands.

Pin Configuration

Pin #	Symbol
1	LE
2	DATA
3	CLK
4, 22	NC
6	RFIN
8	VCC_AMP1/VCC_AMP2
14	VCC_AMP3
16	RFOUT
28	VCC_SPI
All Other Pins	GND

Ordering Information

Part No.	Description
TQM879008	1.5-2.7 GHz Digital Variable Gain Amp
TQM879008-PCB	Fully Assembled Evaluation Board Includes USB control board (EVH)

Standard T/R size = 2500 pieces on a 13” reel.

Specifications

Absolute Maximum Ratings

Parameter	Rating
Storage Temperature	-55 to 150 °C
RF Input Power, CW, 50Ω,T = 25ºC	+23 dBm
Vcc (pins 8, 14, 28)	+5.5 V
Digital Input Voltage	V_{cc}+ 0.5V

Operation of this device outside the parameter ranges given above may cause permanent damage.

Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
Vcc (pins 8, 14, 28)	4.75	5	5.25	V
Case Temperature	-40		85	°C
Junction Temperature, T_J			170	°C

T_J specified for >10^6 hours MTTF

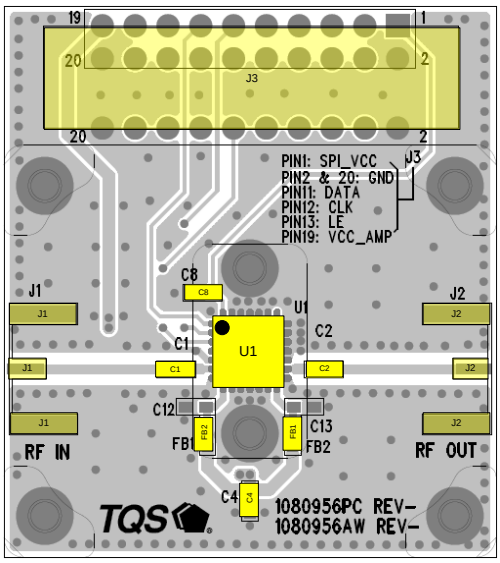
Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

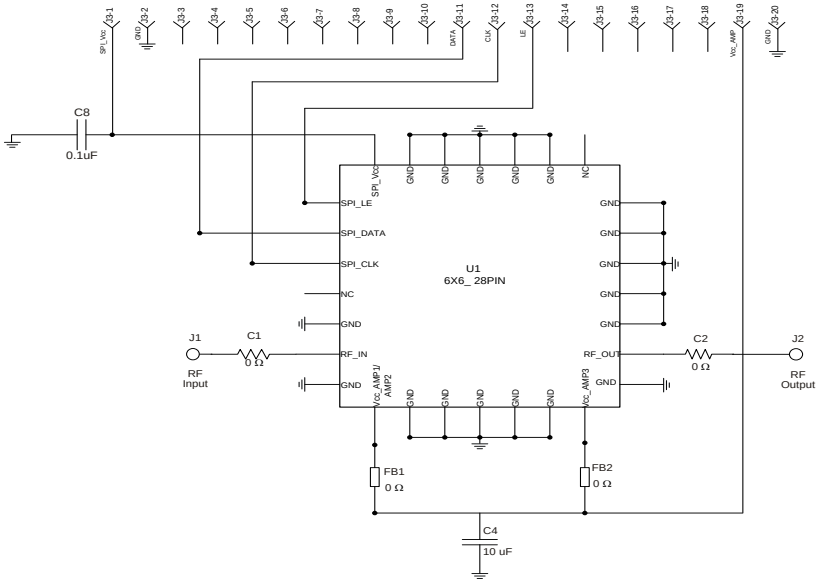
Electrical Specifications

Test conditions unless otherwise noted: 25ºC, +5Vcc, Maximum Gain State.

Parameter	Conditions	Min	Typ	Max	Units
Operational Freq Range		1500		2700	MHz
Test Frequency			2500		MHz
Gain		38	41.1	44	dB
Gain Control Range	0.5 dB Step Size		31.5		dB
Accuracy Error	All States, 3 wire SPI, 6 states	±(0.3+5% of Attenuation setting) Max			dB
Control Interface	3-wire serial interface		6		Bit
Input Return Loss			16		dB
Output Return Loss			14		dB
Noise Figure	Maximum Gain State		3.9		dB
Output P1dB			+27.3		dBm
Output IP3	Pout = +11 dBm/tone, Δf = 1MHz Spacing	+41	+47.5		dBm
I/O Impedance			50		Ohm
Supply Voltage			+5		V
Supply Current		220	285	320	mA
Thermal Resistance, θ_{jc}	Module (junction to case)			20.5	°C/W

Application Circuit (TQM879008-PCB)





Notes:
1. For PCB Board Layout, see page 9 for more information.
2. All Components are of 0603 size unless stated otherwise.
3. For SPI Timing Diagram, see page 6.
4. 0 Ω jumpers may be replaced with copper traces in the target application layout.
5. Different ground pins are used for SPI (digital) and analog supply voltages.
6. The primary RF microstrip characteristic line impedance is 50 Ω.
7. The single power supply is used to provide supply voltage to AMP1, AMP2 and AMP3.

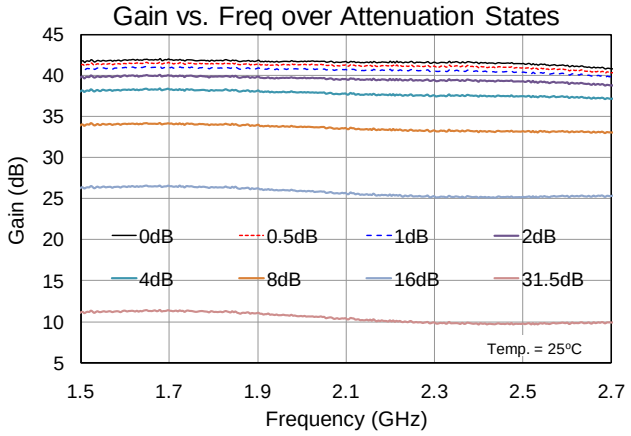
Bill of Material: TQM879008-PCB

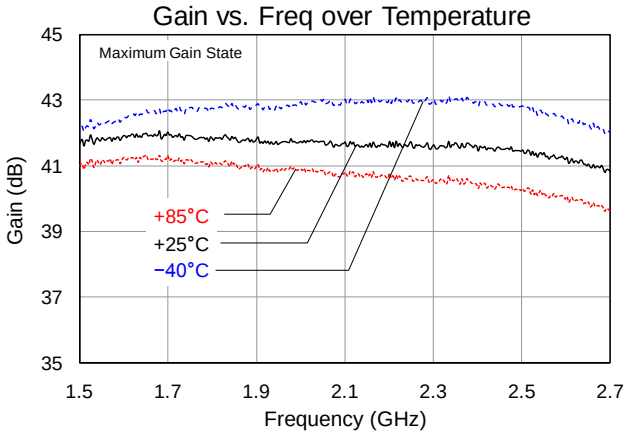
Reference Desg.	Value	Description	Manufacturer	Part Number
U1		1.5 – 2.7 GHz DVGA	TriQuint	TQM879008
C8	0.1 uF	Cap, Chip, 0603, 16V, X7R, 10%	various	
C4	10 uF	Cap, Chip, 0603, 6.3V, X5R, 20%	various	
C1, C2, FB1, FB2	0 Ω	Res, Chip, 0603, 1/16W, 5%	various	

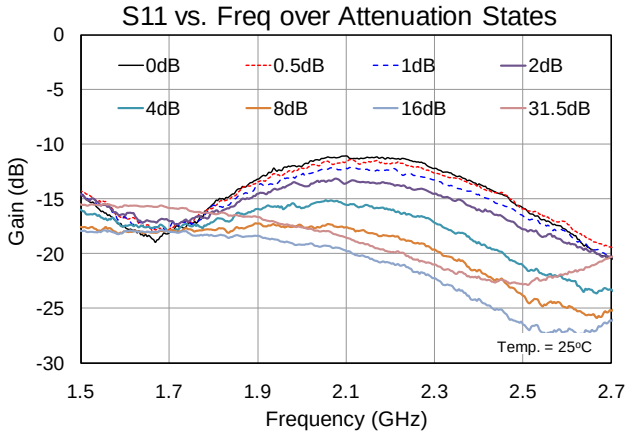
Typical Performance, Maximum Gain State

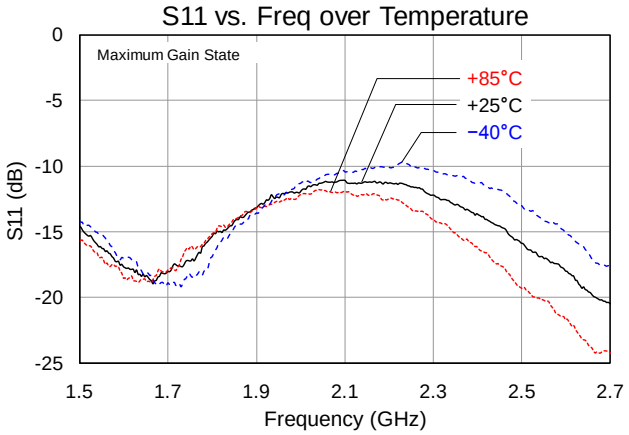
Frequency	GHz	1.5	1.9	2.1	2.3	2.5	2.7
Gain	dB	41.7	41.8	41.7	41.5	41.1	41
Input Return Loss	dB	14.6	13.2	11	12	16	20
Output Return Loss	dB	6.2	9.2	11.7	13	14	12
Output P1dB	dBm	+26.3	+26.7	+27.8	+27.8	+27.3	+27
Output IP3 @ Pout = 11 dBm/tone, Δf = 1 MHz	dBm	+43.7	+40.3	+40.4	+43.5	+48.5	+45
WCDMA channel power at 50dBc ACLR	dBm	17.6	17.8	18.9	18.8	18.5	18
Supply Voltage	V	+5					
Supply Current	mA	285					

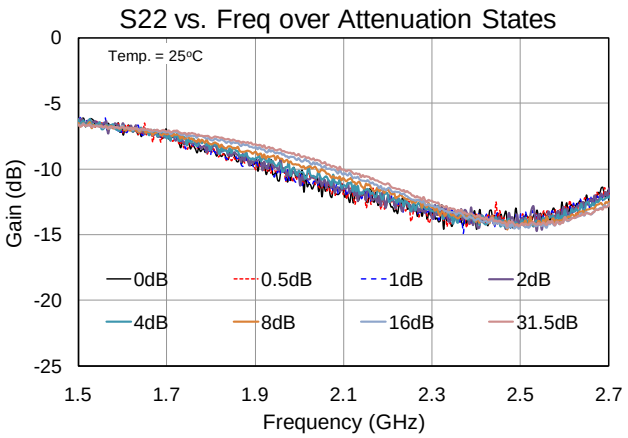
Typical Performance Plots

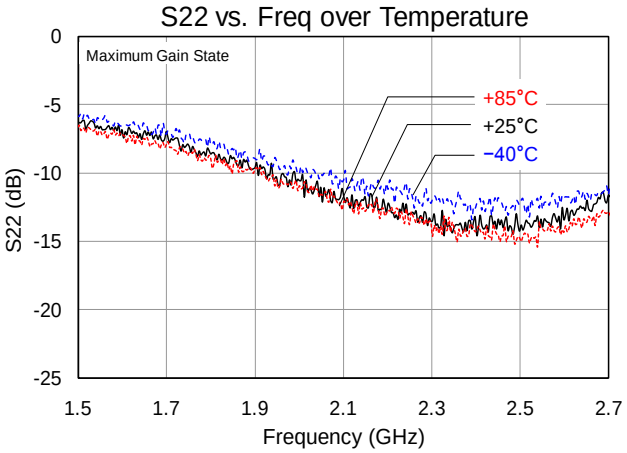




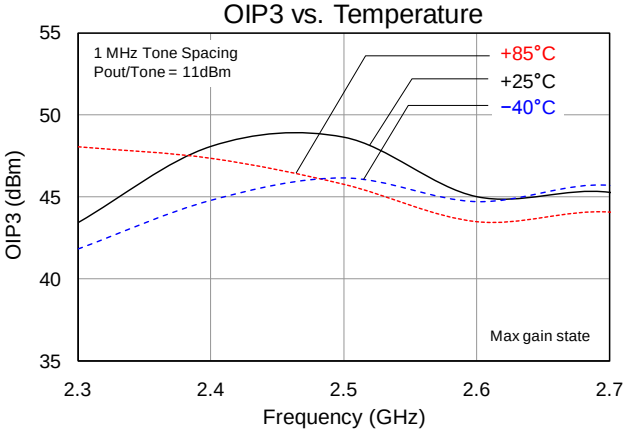




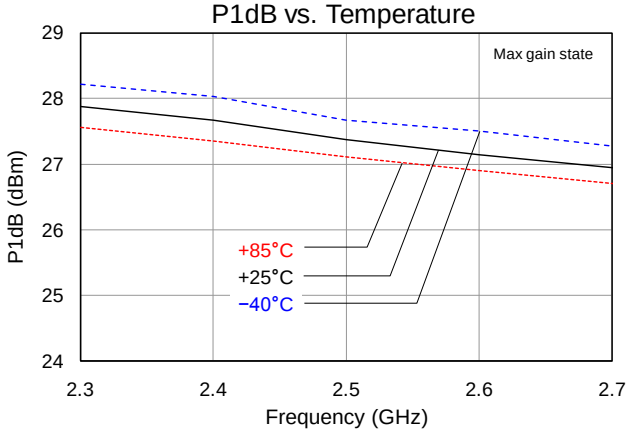




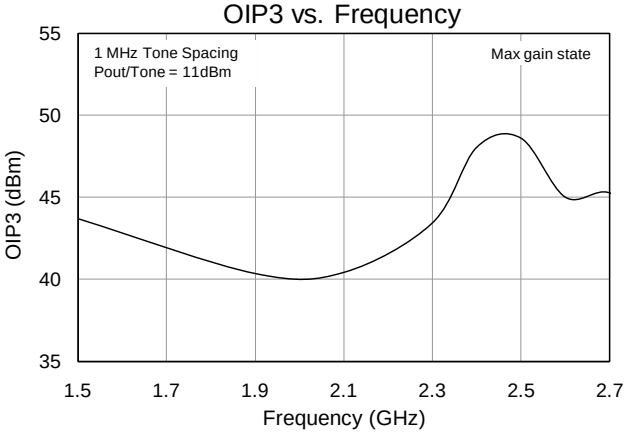
OIP3 vs. Temperature



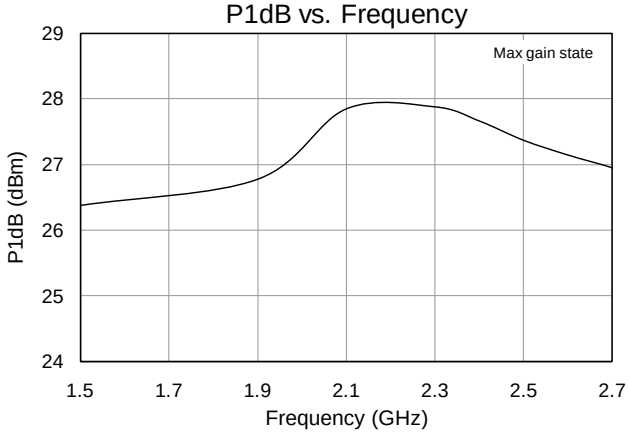
P1dB vs. Temperature



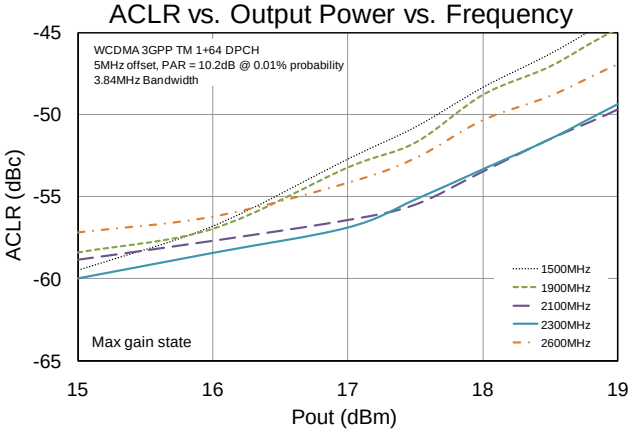
OIP3 vs. Frequency



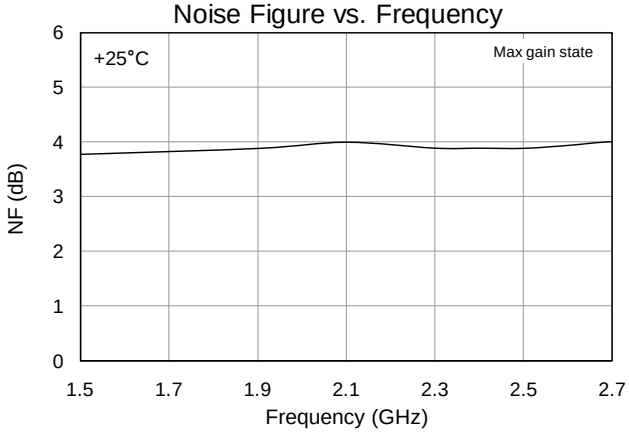
P1dB vs. Frequency



ACLR vs. Output Power vs. Frequency



Noise Figure vs. Frequency



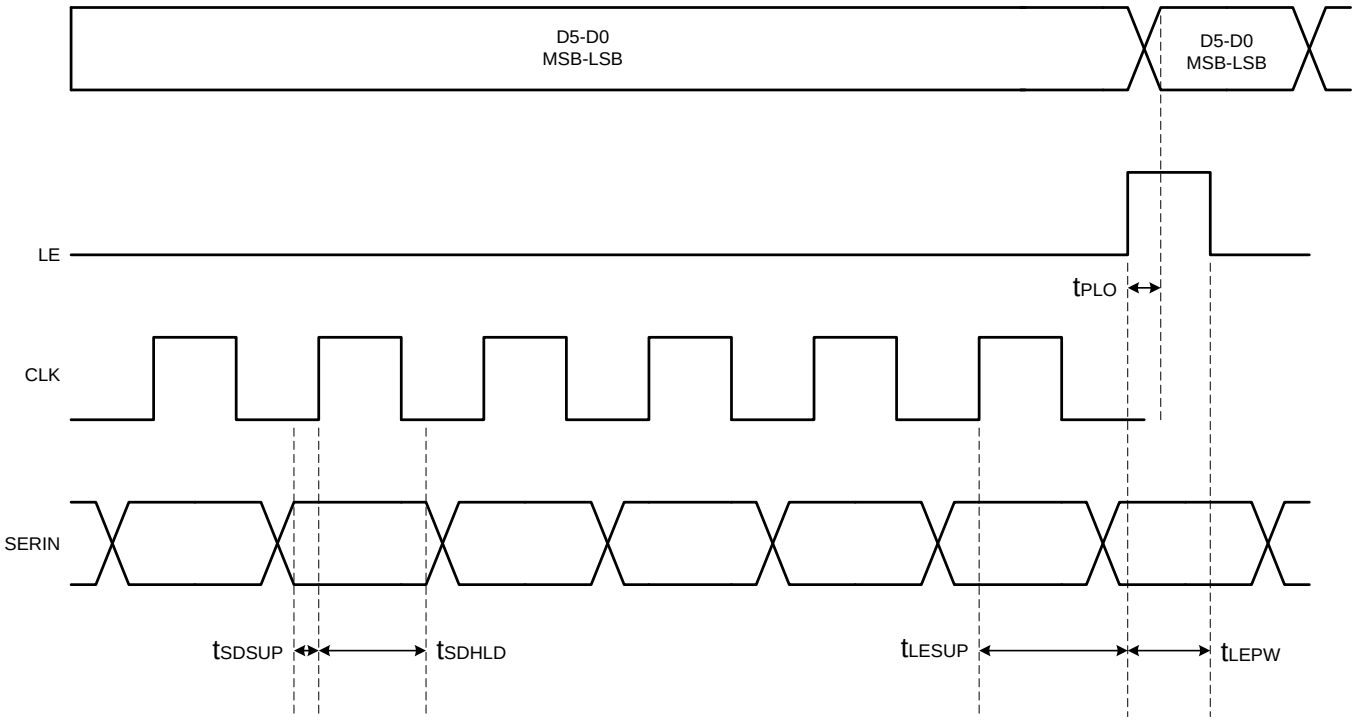
Serial Control Interface

SERIN (MSB in First 6-Bit Word) Control Logic Truth Table

6-Bit Control Word to DSA MSB					LSB	Attenuation State
D5	D4	D3	D2	D1	D0	
1	1	1	1	1	1	Reference : IL
1	1	1	1	1	0	0.5 dB
1	1	1	1	0	1	1 dB
1	1	1	0	1	1	2 dB
1	1	0	1	1	1	4 dB
1	0	1	1	1	1	8 dB
0	1	1	1	1	1	16 dB
0	0	0	0	0	0	31.5 dB
Any combination of the possible 64 states will provide an attenuation of approximately the sum of bits selected						

Serial Control Interface Timing Diagram

CLK is disabled when LE is high



Serial Control Timing Characteristics

Test conditions: 25ºC

Parameter	Condition	Min	Max	Units
Clock Frequency	50% Duty Cycle		10	MHz
LE Setup Time, t_{LESUP}	after last CLK rising edge	10		ns
LE Pulse Width, t_{LEPW}		30		ns
SERIN set-up time, t_{SDSUP}	before CLK rising edge	10		ns
SERIN hold-time, t_{SDHLD}	after CLK rising edge	10		ns
LE Pulse Spacing t_{LE}	LE to LE pulse spacing	630		ns
Propagation Delay t_{PLO}	LE to Parallel output valid		30	ns

Serial Control DC Logic Characteristics

Test conditions: 25ºC

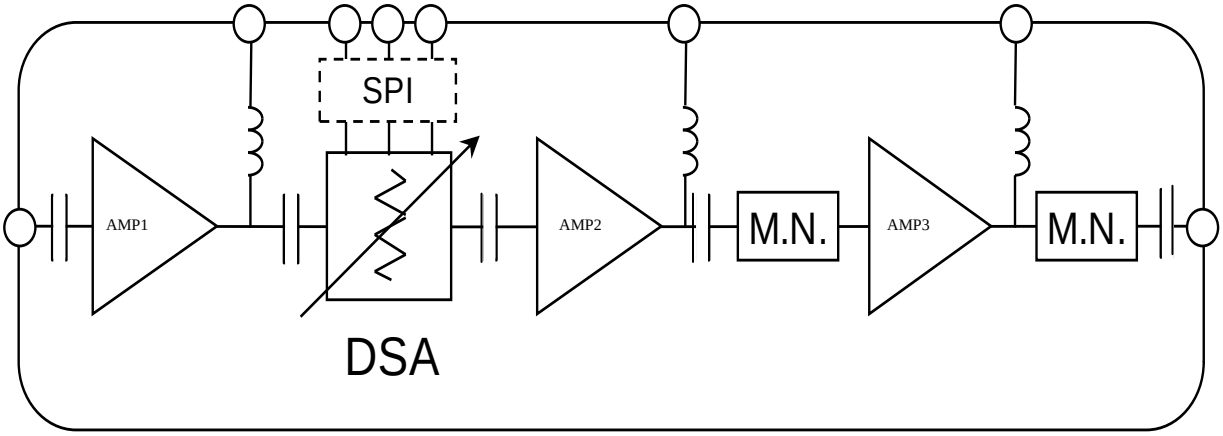
Parameter	Condition	Min	Max	Units
Input Low Voltage, V_{IL}		0	0.8	V
Input High Voltage, V_{IH}		2.1	Vcc	V
Input Current, I_{IH} / I_{IL}	On SERIN, LE and CLK	-10	+10	µA

Detailed Device Description

The TQM879008 is a 50 Ω internally matched digital variable gain amplifier (DVGA) featuring high linearity over the entire gain control range. The amplifier module features the integration of two gain block, a digital-step attenuator (DSA), along with a high linearity ½ W amplifier. The module is unconditionally stable. Internal blocking capacitors and bias structures keep external parts count to a minimum. The DVGA has an operational frequency range from 1.5-2.7 GHz.

For any further technical questions, please email to **sjcapplications.engineering@tqs.com**.

Functional Schematic Diagram



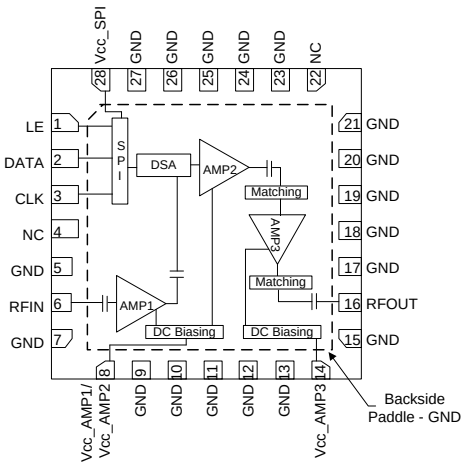
Where M = Matching Network.

Chain Analysis Table

The chain analysis of DVGA module is shown below in the table. This table provides the typical performance of individual stages in the module as well as overall module performance.

	Individual Stage Performance				Overall
Function	**AMP1**	**DSA**	**AMP2**	**AMP3**	**Performance**
Gain (dB)	14	-1.8	14	15	41.1
NF (dB)	3.9	1.8	2.0	4.5	3.9
OIP3 (dBm)	30	55	40	48	47.5
P1dB (dBm)	15	28.5	22	27.4	27.3
Icc (mA)	60	2.0	85	140	285

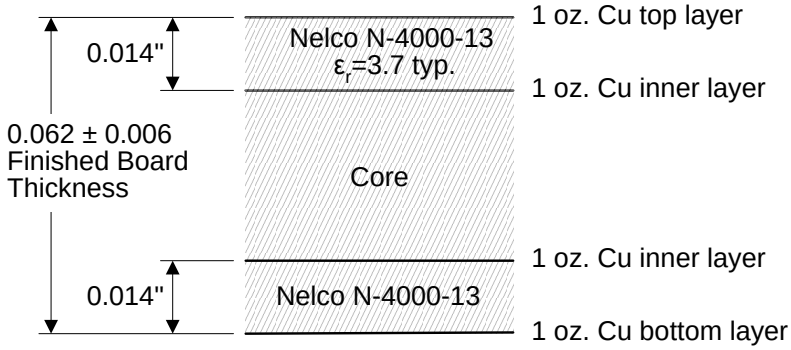
Pin Configuration and Description

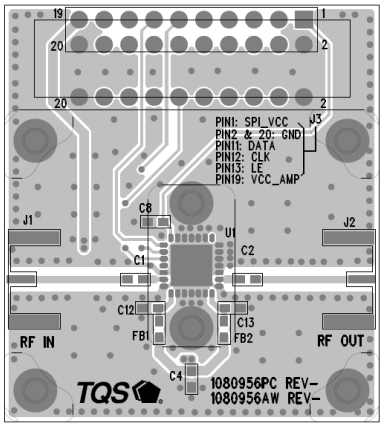


Pin	Symbol	Description
1	LE	Serial Latch Enable Input. When LE is high, latch is clear and content of SPI control the attenuator. When LE is low, data in SPI is latched.
2	DATA	Serial data input. The data and clock pins allow the data to be entered serially into SPI and is independent of Latch state.
3	CLK	Serial clock input.
4, 22	N/C	No connect or open. This pin is not connected in this module
6	RFIN	Input, matched to 50 ohms. Internally DC blocked.
8	VCC_AMP1/ VCC_AMP2	Supply Voltage to AMP1 and AMP2. This pin is connected internally to bypass capacitors followed by inductor inside the module.
14	VCC_AMP3	Supply Voltage to AMP3. This pin is connected internally to bypass capacitors followed by inductor inside the module.
16	RFOUT	Output, matched to 50 ohms. Internally DC blocked.
28	VCC_SPI	Supply voltage for SPI and DSA chip. This pin is connected to bypass capacitor internally.
All other Pins	GND	RF/DC Ground Connection

PC Board Specifications

PCB Material and Stack-up



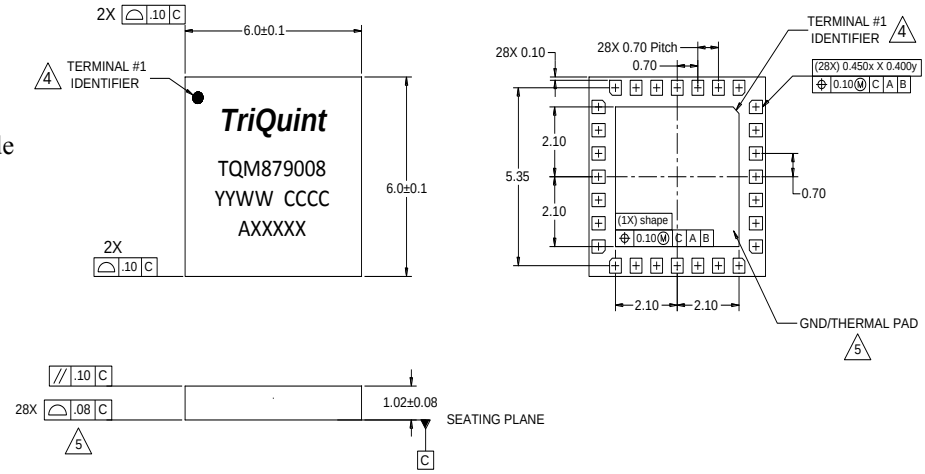


Mechanical Information

Package Information and Dimensions

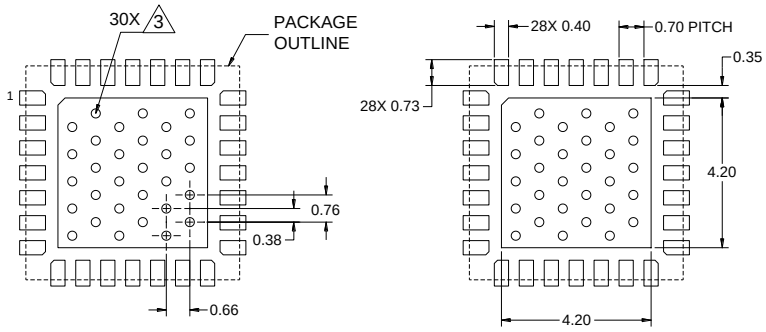
Markings:

Part Number: TQM879008
Lot Code: 'YY' is the year of manufacture
'WW' is the work week
'AaXXXX' is the Assembly code



1. All dimensions are in millimeters. Angles are in degrees.
2. Except where noted, this part outline conforms to JEDEC standard MO-270, Issue B (Variation DAE) for extra thin profile, fine pitch, internal stacking module (ISM).
3. Dimension and tolerance formats conform to ASME Y14.4M-1994.
4. The contact pin numbering convention and pin 1 identifier conform to JESD 95-1 SPP-012.
5. Coplanarity applies to the exposed ground/thermal pad as well as the contact pins.

PCB Mounting Pattern



COMPONENT SIDE

Notes:

1. All dimensions are in millimeters. Angles are in degrees.
2. Use 1 oz. copper minimum for top and bottom layer metal.
3. Vias are required under the backside paddle of this device for proper RF/DC grounding and thermal dissipation. We recommend a 0.35mm (#80/.0135") diameter bit for drilling via holes and a final plated thru diameter of 0.25mm (0.10").
4. Ensure good package backside paddle solder attach for reliable operation and best electrical performance.

Product Compliance Information

ESD Information

Caution! ESD-Sensitive Device

ESD Rating:	Class 1C
Value:	Passes ≥ 1000 V to < 2000 V
Test:	Human Body Model (HBM)
Standard:	JEDEC Standard JESD22-A114

ESD Rating:	Class IV
Value:	Passes ≥ 1000 V
Test:	Charged Device Model (CDM)
Standard:	JEDEC Standard JESD22-C101

MSL Rating

The part is rated Moisture Sensitivity Level 3 at 260°C per JEDEC standard IPC/JEDEC J-STD-020.

Solderability

Compatible with both lead-free (maximum 260 °C reflow temperature) and tin/lead (maximum 245 °C reflow temperature) soldering processes.

This part is compliant with EU 2002/95/EC RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment).

This product also has the following attributes:

- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A ($C_{15}H_{12}Br_40_2$) Free
- PFOS Free
- SVHC Free

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations, and information about TriQuint:

Web: www.triquint.com **Tel:** +1.503.615.9000
Email: info-sales@tqs.com **Fax:** +1.503.615.8902

For technical questions and application information:

Email: sjcapplications.engineering@tqs.com

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