N-Ch and P-Ch 30V Fast Switching MOSFETs

General Description

The UM3304 is the highest performance trench N-ch and P-ch MOSFETs with extreme high cell density , which provide excellent RDSON and gate charge for most of the synchronous buck converter applications .

The UM3304 meet the RoHS and Green Product requirement with full function reliability approved.

Features

- Advanced high cell density Trench technology
- Super Low Gate Charge
- Excellent CdV/dt effect decline
- 100% EAS Guaranteed
- Green Device Available

Product Summery

BVDSS	RDSON	ID
30V	45mΩ	4.6A
-30V	125mΩ	-3A

Applications

- High Frequency Point-of-Load Synchronous Buck Converter for MB/NB/UMPC/VGA
- Networking DC-DC Power System
- CCFL Back-light Inverter

SOP8 Pin Configuration

Absolute Maximum Ratings

Symbol	Parameter	Rating		Units
		N-Ch	P-Ch	
V_{DS}	Drain-Source Voltage	30	-30	V
V_{GS}	Gate-Source Voltage	±20	±20	V
I_D@T_A=25℃	Continuous Drain Current, V_{GS} @ 10V[1]	4.6	-3	A
I_D@T_A=70℃	Continuous Drain Current, V_{GS} @ 10V[1]	3.7	-2.3	A
I_{DM}	Pulsed Drain Current[2]	9.2	-6	A
P_D@T_A=25℃	Total Power Dissipation[4]	1.5	1.5	W
T_{STG}	Storage Temperature Range	-55 to 150	-55 to 150	℃
T_J	Operating Junction Temperature Range	-55 to 150	-55 to 150	℃

Thermal Data

Symbol	Parameter	Typ.	Max.	Unit
$R_{\theta JA}$	Thermal Resistance Junction-Ambient [1]	---	85	℃/W
$R_{\theta JC}$	Thermal Resistance Junction-Case[1]	---	60	℃/W

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N-Channel Electrical Characteristics (T_J=25 ℃, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V , I_D=250uA	30	---	---	V
$\triangle BV_{DSS}/\triangle T_J$	BVDSS Temperature Coefficient	Reference to 25℃ , I_D=1mA	---	0.016	---	V/℃
$R_{DS(ON)}$	Static Drain-Source On-Resistance[2]	V_{GS}=10V , I_D=4A	---	38	45	mΩ
		V_{GS}=4.5V , I_D=2A	---	56	70	
$V_{GS(th)}$	Gate Threshold Voltage	V_{GS}=V_{DS} , I_D =250uA	1.0	1.5	2.5	V
$\triangle V_{GS(th)}$	$V_{GS(th)}$ Temperature Coefficient		---	-3.04	---	mV/℃
I_{DSS}	Drain-Source Leakage Current	V_{DS}=24V , V_{GS}=0V , T_J=25℃	---	---	1	uA
		V_{DS}=24V , V_{GS}=0V , T_J=55℃	---	---	5	
I_{GSS}	Gate-Source Leakage Current	V_{GS}=$\pm$20V , V_{DS}=0V	---	---	$\pm$100	nA
gfs	Forward Transconductance	V_{DS}=5V , I_D=4A	---	8	---	S
R_g	Gate Resistance	V_{DS}=0V , V_{GS}=0V , f=1MHz	---	2.3	4.6	Ω
Q_g	Total Gate Charge (4.5V)	V_{DS}=20V , V_{GS}=4.5V , I_D=4A	---	2.75		nC
Q_{gs}	Gate-Source Charge		---	0.67		
Q_{gd}	Gate-Drain Charge		---	1.52		
$T_{d(on)}$	Turn-On Delay Time	V_{DD}=15V , V_{GS}=10V , R_G=3.3Ω I_D=4A	---	3.6		ns
T_r	Rise Time		---	14.6		
$T_{d(off)}$	Turn-Off Delay Time		---	11.5		
T_f	Fall Time		---	1.9		
C_{iss}	Input Capacitance	V_{DS}=15V , V_{GS}=0V , f=1MHz	---	220		pF
C_{oss}	Output Capacitance		---	38		
C_{rss}	Reverse Transfer Capacitance		---	32		

Diode Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_S	Continuous Source Current[1,4]	V_G=V_D=0V , Force Current	---	---	4.6	A
I_{SM}	Pulsed Source Current[2,4]		---	---	9.2	A
V_{SD}	Diode Forward Voltage[2]	V_{GS}=0V , I_S=1A , T_J=25℃	---	---	1	V

Note :
1.The data tested by surface mounted on a 1 inch[2] FR-4 board with 2OZ copper.
2.The data tested by pulsed , pulse width $\leqq$ 300us , duty cycle $\leqq$ 2%
3.The power dissipation is limited by 150℃ junction temperature
4.The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.

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P-Channel Electrical Characteristics (T_J=25 ℃, unless otherwise noted)

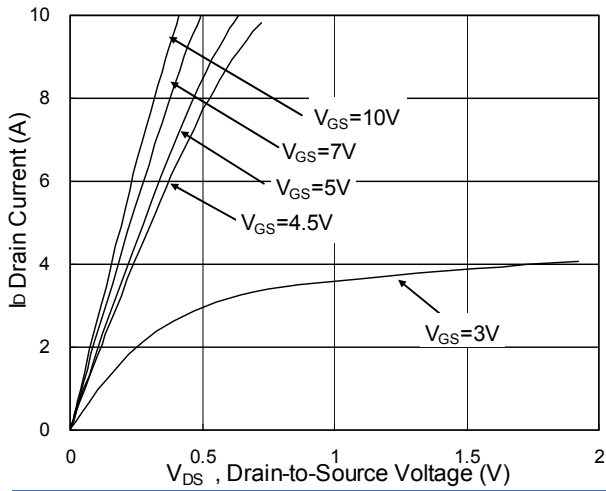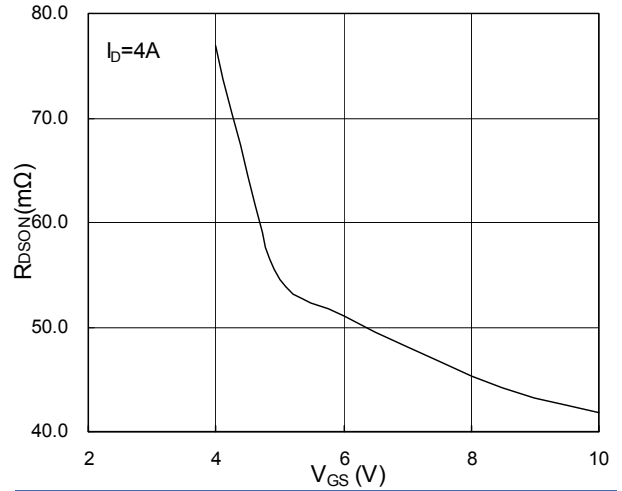| Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V , I_D=-250uA	-30	---	---	V
$\triangle BV_{DSS}/\triangle T_J$	BV_{DSS} Temperature Coefficient	Reference to 25℃ , I_D=-1mA	---	-0.02	---	V/℃
$R_{DS(ON)}$	Static Drain-Source On-Resistance[2]	V_{GS}=-10V , I_D=-3A	---	105	125	mΩ
		V_{GS}=-4.5V , I_D=-1.5A	---	180	215	
$V_{GS(th)}$	Gate Threshold Voltage	V_{GS}=V_{DS} , I_D =-250uA	-1.0	-1.5	-2.5	V
$\triangle V_{GS(th)}$	$V_{GS(th)}$ Temperature Coefficient		---	3.72	---	mV/℃
I_{DSS}	Drain-Source Leakage Current	V_{DS}=-24V , V_{GS}=0V , T_J=25℃	---	---	1	uA
		V_{DS}=-24V , V_{GS}=0V , T_J=55℃	---	---	5	
I_{GSS}	Gate-Source Leakage Current	V_{GS}=±20V , V_{DS}=0V	---	---	±100	nA
gfs	Forward Transconductance	V_{DS}=-5V , I_D=-3A	---	3.8	---	S
R_g	Gate Resistance	V_{DS}=0V , V_{GS}=0V , f=1MHz	---	26	52	Ω
Q_g	Total Gate Charge (-4.5V)	V_{DS}=-20V , V_{GS}=-4.5V , I_D=-1A	---	3.3	---	nC
Q_{gs}	Gate-Source Charge		---	0.88	---	
Q_{gd}	Gate-Drain Charge		---	1.55	---	
$T_{d(on)}$	Turn-On Delay Time	V_{DD}=-15V , V_{GS}=-10V , R_G=3.3Ω, I_D=-1A	---	9.6	---	ns
T_r	Rise Time		---	6.7	---	
$T_{d(off)}$	Turn-Off Delay Time		---	21.5	---	
T_f	Fall Time		---	3.3	---	
C_{iss}	Input Capacitance	V_{DS}=-15V , V_{GS}=0V , f=1MHz	---	203	---	pF
C_{oss}	Output Capacitance		---	42	---	
C_{rss}	Reverse Transfer Capacitance		---	34	---	

Diode Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_S	Continuous Source Current[1,4]	V_G=V_D=0V , Force Current	---	---	-3	A
I_{SM}	Pulsed Source Current[2,4]		---	---	-6	A
V_{SD}	Diode Forward Voltage[2]	V_{GS}=0V , I_S=-1A , T_J=25℃	---	---	-1.2	V

Note :
1.The data tested by surface mounted on a 1 inch[2] FR-4 board with 2OZ copper.
2.The data tested by pulsed , pulse width ≦ 300us , duty cycle ≦ 2%
3The power dissipation is limited by 150℃ junction temperature
4.The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.

N-Channel Typical Characteristics

Fig.1 Typical Output Characteristics

Fig.2 On-Resistance vs. G-S Voltage
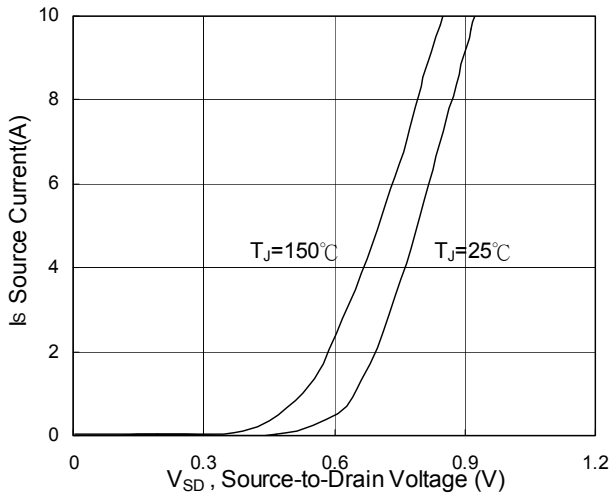
Fig.3 Forward Characteristics of Reverse
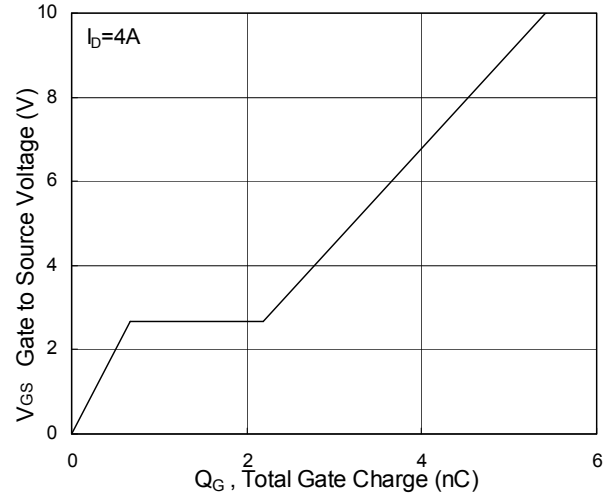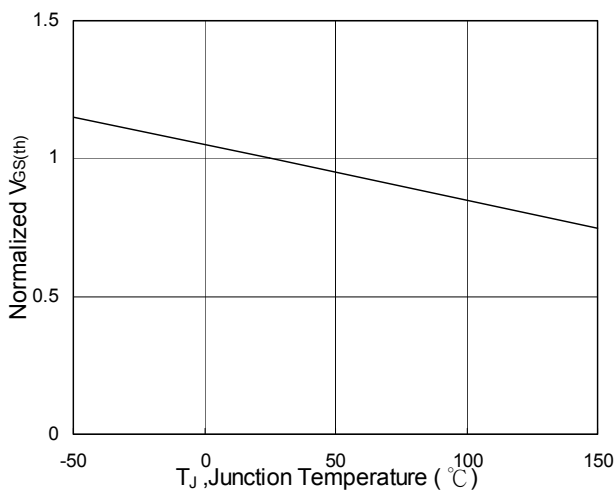
Fig.4 Gate-charge Characteristics

Fig.5 Normalized $V_{GS(th)}$ vs. T_J

Fig.6 Normalized R_{DSON} vs. T_J
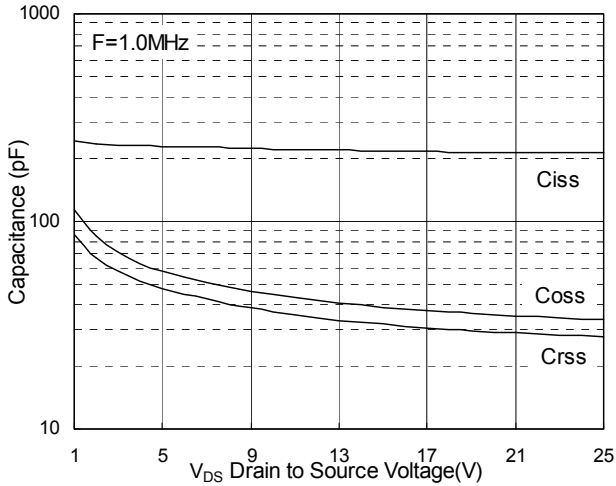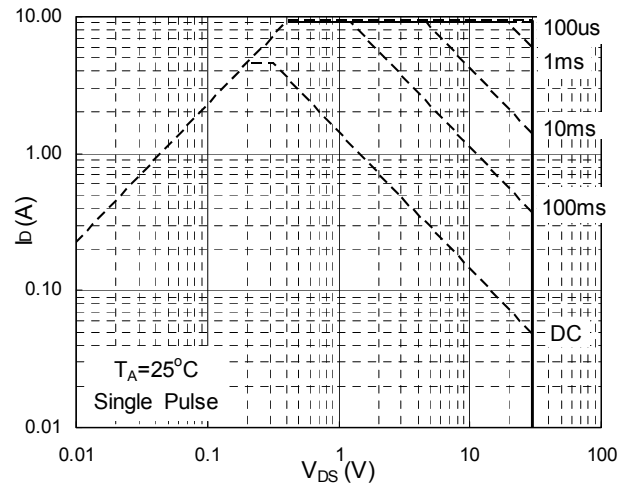
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Fig.7 Capacitance

Fig.8 Safe Operating Area

$D = T_{ON}/T$
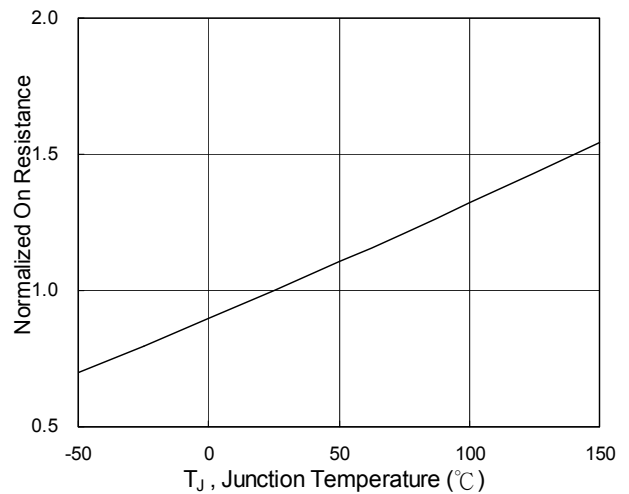
$T_{Jpeak} = T_C + P_{DM} \times R_{\theta JA}$
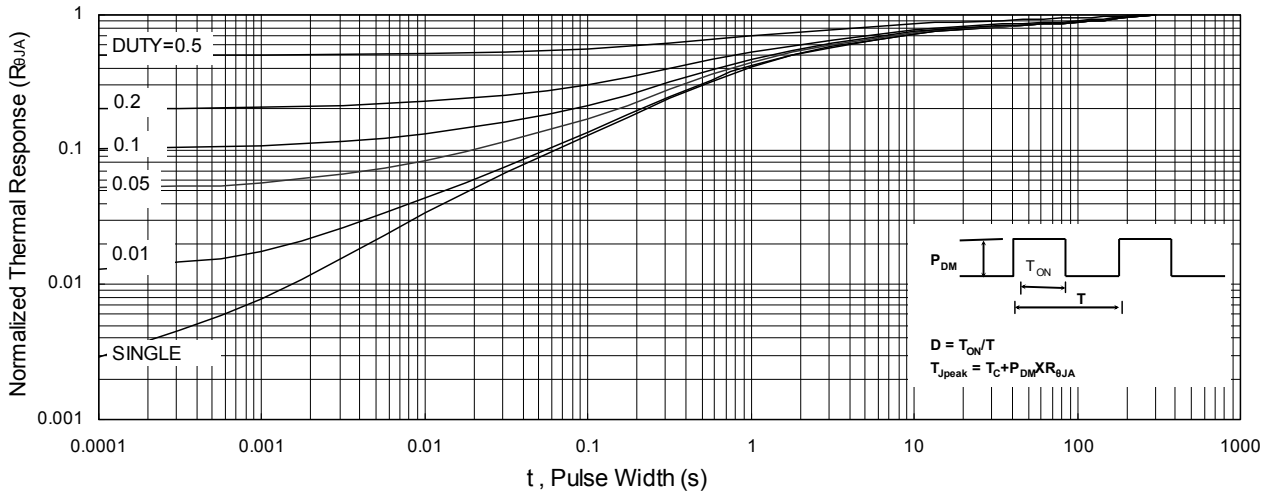
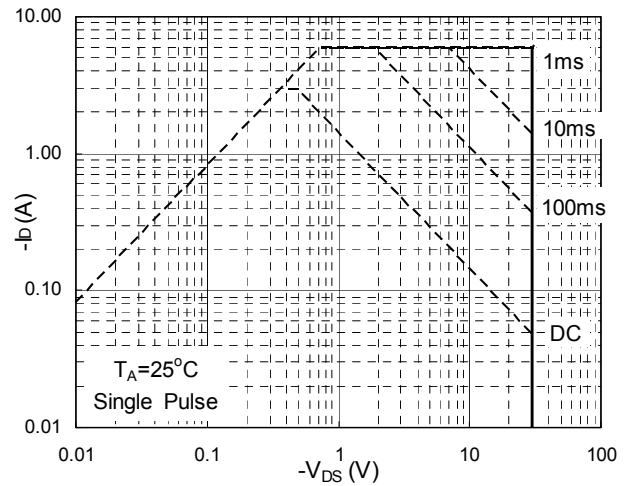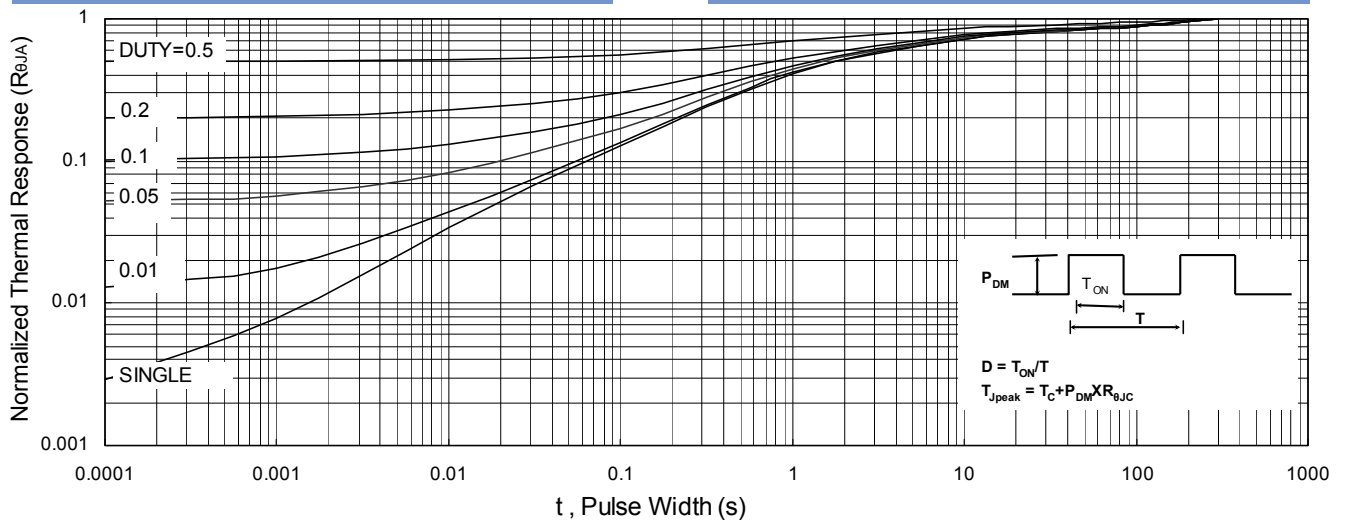**Fig.9 Normalized Maximum Transient Thermal Impedance**
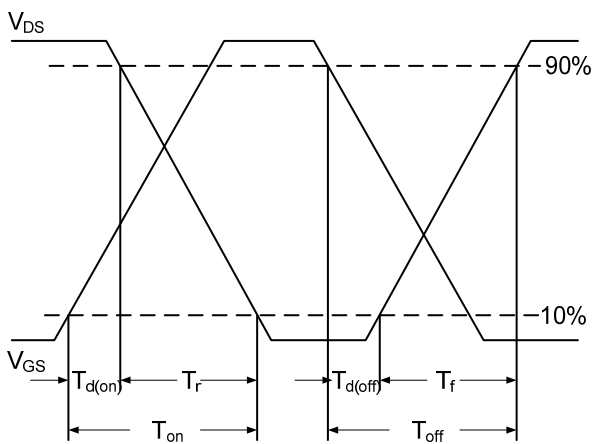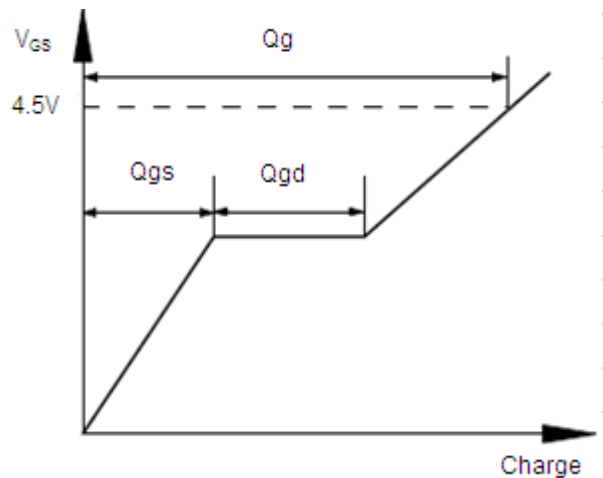
Fig.10 Switching Time Waveform

Fig.11 Gate Charge Waveform

N-Channel Typical Characteristics
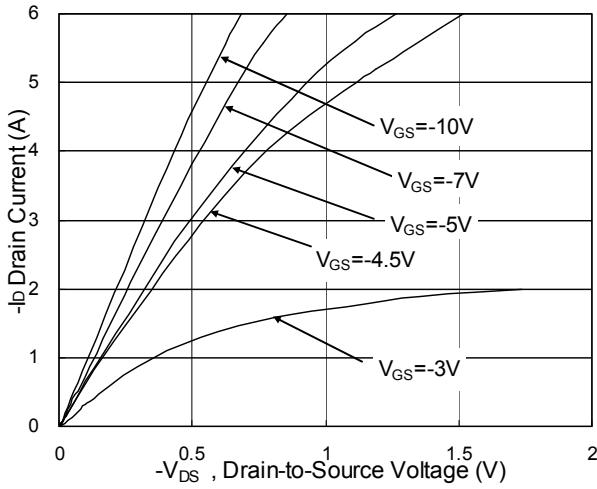
Fig.1 Typical Output Characteristics
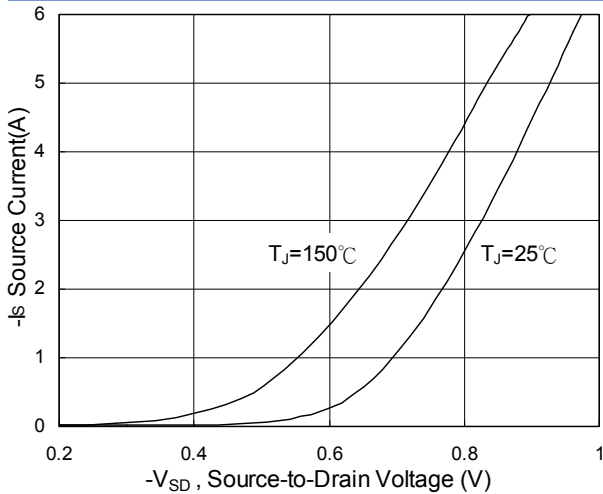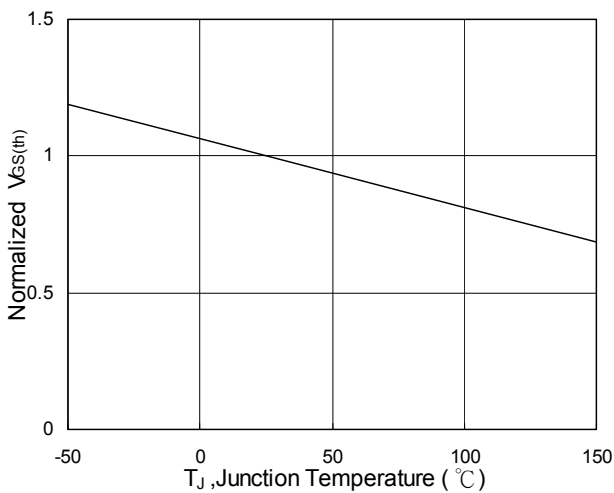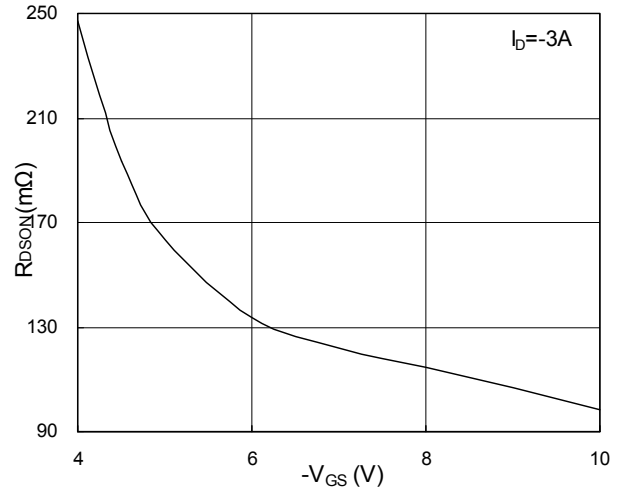
Fig.2 On-Resistance v.s Gate-Source

Fig.3 Forward Characteristics of Reverse

Fig.4 Gate-Charge Characteristics

Fig.5 Normalized $V_{GS(th)}$ v.s T_J

Fig.6 Normalized R_{DSON} v.s T_J

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$D = T_{ON}/T$

$T_{Jpeak} = T_C + P_{DM} X R_{\theta JC}$
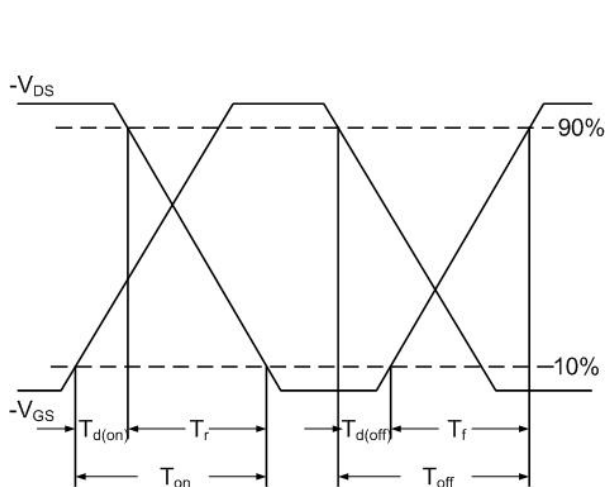
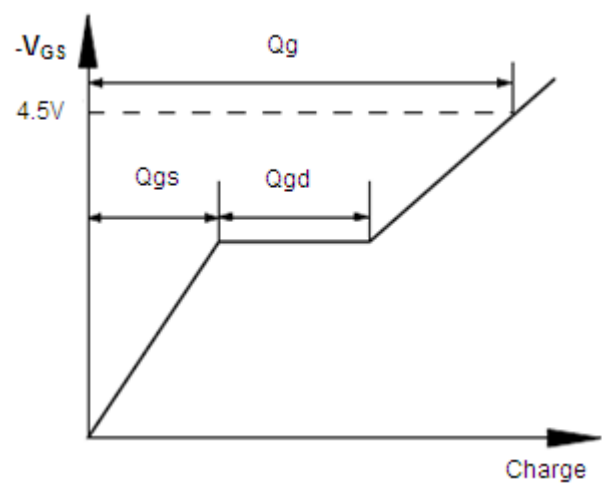**Fig.9 Normalized Maximum Transient Thermal Impedance**

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