Low Charge Injection 16-Channel High Voltage Analog Switch with Bleed Resistors

Features

- ❑ HVCMOS technology for high performance
- ❑ Integrated bleed resistors on the outputs
- ❑ 16 Channels of high voltage analog switch
- ❑ 3.3V input logic level compatible
- ❑ 20MHz data shift clock frequency
- ❑ Very low quiescent power dissipation-10µA
- ❑ Low parasitic capacitance
- ❑ DC to 10MHz analog signal frequency
- ❑ -60dB typical off-isolation at 5MHz
- ❑ CMOS logic circuitry for low power
- ❑ Excellent noise immunity
- ❑ Cascadable serial data register with latches
- ❑ Flexible operating supply voltages

Applications

- ❑ Medical ultrasound imaging
- ❑ NDT metal flaw detection
- ❑ Piezoelectric transducer drivers
- ❑ Optical MEMS modules

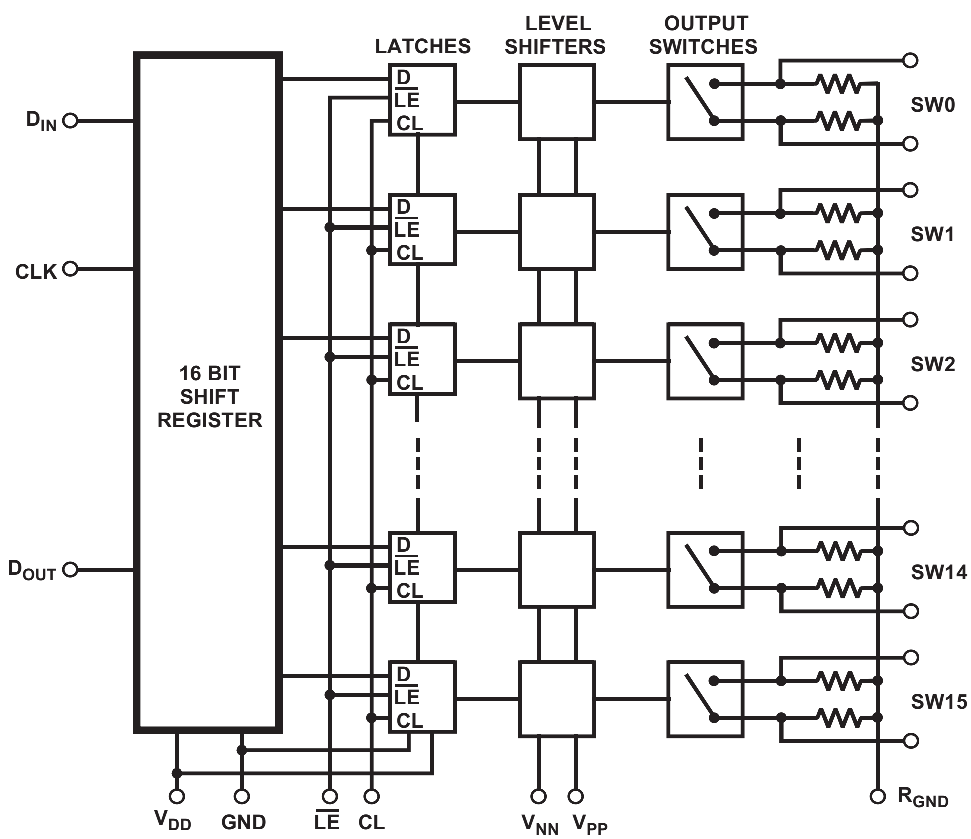
General Description

The Supertex HV2701 is a low charge injection 16-channel high voltage analog switch integrated circuit (IC) with bleed resistors. The device can be used in applications requiring high voltage switching controlled by low voltage control signals, such as medical ultrasound imaging and piezoelectric transducer drivers. The bleed resistors eliminate voltage built up on capacitive loads such as piezoelectric transducers.

Input data is shifted into a 16-bit shift register that can then be retained in a 16-bit latch. To reduce any possible clock feed through noise, the latch enable bar should be left high until all bits are clocked in. Data are clocked in during the rising edge of the clock. Using HVCMOS technology, this device combines high voltage bilateral DMOS switches and low power CMOS logic to provide efficient control of high voltage analog signals.

The device is suitable for various combinations of high voltage supplies, e.g., V_{PP}/V_{NN}: +40V/-160V, +100V/-100V, and +160V/-40V.

HV2701 Block Diagram



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Ordering Information

DEVICE	Package Options
	48-Lead TQFP (1.4mm)
HV2701	HV2701FG-G

-G indicates package is RoHS compliant ('Green')

Absolute Maximum Ratings

V_{DD} Logic supply	-0.5V to +7V
V_{PP}-V_{NN} differential supply	220V
V_{PP} Positive supply	-0.5V to V_{NN}+200V
V_{NN} Negative supply	+0.5V to -200V
Logic input voltage	-0.5V to V_{DD} +0.3V
Analog signal range	V_{NN} to V_{PP}
Peak analog signal current/channel	3.0A
Storage temperature	-65°C to 150°C
Power dissipation	1W

**Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.*

Operation Conditions

Symbol	Parameter	Value
V_{DD}	Logic power supply voltage	3.0V to 5.5V
V_{PP}	Positive high voltage supply	40V to V_{NN} +200V
V_{NN}	Negative high voltage supply	-40V to –160V
V_{IH}	High level input voltage	0.9V_{DD} to V_{DD}
V_{IL}	Low level input voltage	0V to 0.1V_{DD}
V_{SIG}	Analog signal voltage peak-to-peak	V_{NN}+10V to V_{PP}-10V
T_A	Operating free air temperature	0°C to 70°C

Notes:
1 Power up/down sequence is arbitrary except GND must be powered-up first and powered-down last.
2 V_{SIG} must be within V_{NN} and V_{PP} or floating during power up/down transition.
3 Rise and fall times of power supplies V_{DD}, V_{PP}, and V_{NN} should not be less than 1.0msec.

DC Electrical Characteristics

(over recommended operating conditions unless otherwise noted)

Sym	Parameter	0°C Min	0°C Max	+25°C Min	+25°C Typ	+25°C Max	+70°C Min	+70°C Max	Units	Conditions	
R_{ONS}	Small Signal Switch On-Resistance		30		26	38		48	Ω	I_{SIG} = 5mA	V_{PP} = +40V, V_{NN} = -160V
			25		22	27		32		I_{SIG} = 200mA	
			25		22	27		30		I_{SIG} = 5mA	V_{PP} = +100V, V_{NN} = -100V
			18		18	24		27		I_{SIG} = 200mA	
			23		20	25		30		I_{SIG} = 5mA	V_{PP} = +160V, V_{NN} = -40V
			22		16	25		27		I_{SIG} = 200mA	
ΔR_{ONS}	Small Signal Switch On-Resistance Matching		20		5.0	20		20	%	I_{SIG} = 5mA, V_{PP} = +100V, V_{NN} = -100V	
R_{ONL}	Large Signal Switch On-Resistance				15				Ω	V_{SIG}=V_{PP}-10V, I_{SIG}=1A	
R_{INT}	Value of output Bleed Resistor			20	35	50			KΩ	Output Switch to RGND, I_{RINT} = 0.5mA	
I_{SOL}	Switch Off Leakage per Switch*		5.0		1.0	10		15	µA	V_{SIG} = V_{PP}-10V and V_{NN}+10V	
V_{OS}	DC Offset Switch off*		300		100	300		300	mV	No Load	
	DC Offset Switch on*		500		100	500		500	mV		
I_{PPQ}	Quiescent V_{PP} supply current				10	50			µA	All switches off	
I_{NNQ}	Quiescent V_{NN} supply current				-10	-50			µA	All switches off	
I_{PPQ}	Quiescent V_{PP} supply current				10	50			µA	All switches on, I_{SW} = 5mA	
I_{NNQ}	Quiescent V_{NN} supply current				-10	-50			µA	All switches on, I_{SW} = 5mA	
I_{SW}	Switch output peak current		3.0		3.0	2.0		2.0	A	V_{SIG} duty cycle < 0.1%	
f_{SW}	Output switching frequency					50			kHz	Duty cycle = 50%	
I_{PP}	Average V_{PP} supply current		6.5			7.0		8.0	mA	V_{PP} = +40V, V_{NN} = -160V	All output switches are turning On and Off at 50KHz with no load.
			4.0			5.5		5.5		V_{PP} = +100V, V_{NN} = -100V	
			4.0			5.0		5.5		V_{PP} = +160V, V_{NN} = -40V	
I_{NN}	Average V_{NN} supply current		6.5			7.0		8.0	mA	V_{PP} = +40V, V_{NN} = -160V	
			4.0			5.0		5.5		V_{PP} = +100V, V_{NN} = -100V	
			4.0			5.0		5.5		V_{PP} = +160V, V_{NN}=-40V	
I_{DD}	Average V_{DD} supply current		4.0			4.0		4.0	mA	f_{CLK} = 5MHz, V_{DD} = 5.0V	
I_{DDQ}	Quiescent V_{DD} supply current		10			10		10	µA	All logic inputs are static	
I_{SOR}	Data out source current	0.45		0.45	0.70		0.40		mA	V_{OUT} = V_{DD}-0.7V	
I_{SINK}	Data out sink current	0.45		0.45	0.70		0.40		mA	V_{OUT} = 0.7V	
C_{IN}	Logic input capacitance		10			10		10	pF		

** See Test Circuits on page 5*

AC Electrical Characteristics

(over recommended operating conditions, V_{DD}= 5.0V, t_R= t_F ≤ 5ns, 50% duty cycle, C_{LOAD}= 20pF unless otherwise noted)

Sym	Parameter	0°C		+25°C			+70°C		Units	Conditions
		Min	Max	Min	Typ	Max	Min	Max		
t_{SD}	Set Up Time Before LE Rises	25		25			25		ns	
t_{WLE}	Time Width of LE	56			56		56		ns	V_{DD} = 3.0V
		12			12		12			V_{DD} = 5.0V
t_{DO}	Clock Delay Time to Data Out	50	100	50	78	100	50	100	ns	V_{DD} = 3.0V
		15	40	15	30	40	15	40		V_{DD}= 5.0V
t_{WCL}	Time Width of CL	55		55			55		ns	
t_{SU}	Set Up Time Data to Clock	21			21		21		ns	V_{DD}= 3.0V
		7			7		7			V_{DD}= 5.0V
t_H	Hold Time Data from Clock	2		2			2		ns	V_{DD}= 3.0 or 5.0V
f_{CLK}	Clock Frequency		8			8		8	MHz	V_{DD}= 3.0V
			20			20		20		V_{DD}= 5.0V
t_R,t_F	Clock Rise and Fall Times		50			50		50	ns	
T_{ON}	Turn ON Time*		5.0			5.0		5.0	µs	V_{SIG} = V_{PP}-10V, R_{LOAD} = 10KΩ
T_{OFF}	Turn OFF Time*		5.0			5.0		5.0	µs	V_{SIG} = V_{PP}-10V, R_{LOAD} = 10KΩ
dv/dt	Maximum V_{SIG} Slew Rate		20			20		20	v/ns	V_{PP} = +40V, V_{NN} = -160V
			20			20		20		V_{PP} = +100V, V_{NN} = -100V
			20			20		20		V_{PP} = +160V, V_{NN} = -40V
K_O	Off Isolation*	-30		-30	-33		-30		dB	f = 5.0MHz, 1KΩ//15pF load
		-58		-58			-58			f = 5.0MHz, 50Ω load
K_{CR}	Switch Crosstalk*	-60		-60	-70		-60		dB	f = 5.0MHz, 50Ω load
I_{ID}	Output Switch Isolation Diode Current		300			300		300	mA	300ns pulse width, 2.0% duty cycle
$C_{SG(OFF)}$	Off Capacitance SW to GND	5.0	17	5.0	12	17	5.0	17	pF	0V, f = 1.0MHz
$C_{SG(ON)}$	On Capacitance SW to GND	25	50	25	38	50	25	50	pF	0V, f = 1.0MHz
$+V_{SPK}$ $-V_{SPK}$	Output Voltage Spike*					150			mV	V_{PP} = +40V, V_{NN} = -160V, R_{LOAD} = 50ohm
$+V_{SPK}$ $-V_{SPK}$						150				V_{PP} = +100V, V_{NN} = -100V, R_{LOAD} = 50ohm
$+V_{SPK}$ $-V_{SPK}$						150				V_{PP} = +160V, V_{NN} = -40V, R_{LOAD} = 50ohm
QC	Charge Injection*				820				pC	V_{PP}= +40V, V_{NN}= -160V, V_{SIG}= 0V
					600					V_{PP}= +100V, V_{NN}= -100V, V_{SIG}= 0V
					350					V_{PP}= +160V, V_{NN}= -40V, V_{SIG}= 0V

** See Test Circuits on page 5*

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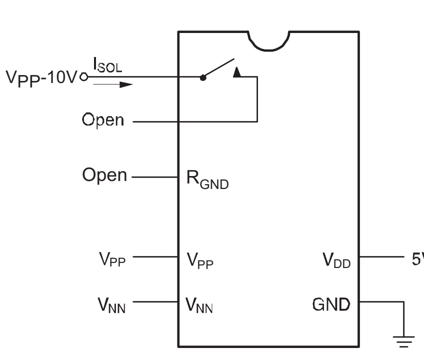
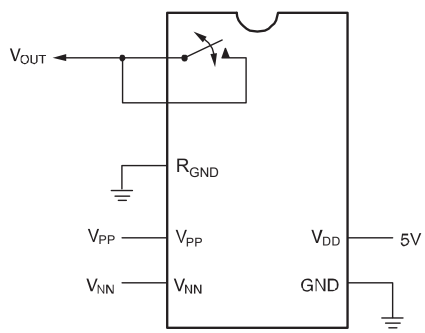
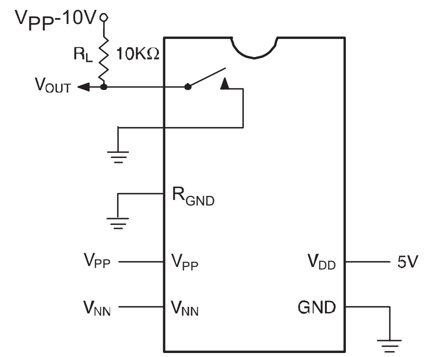
HV2701 Test Circuits



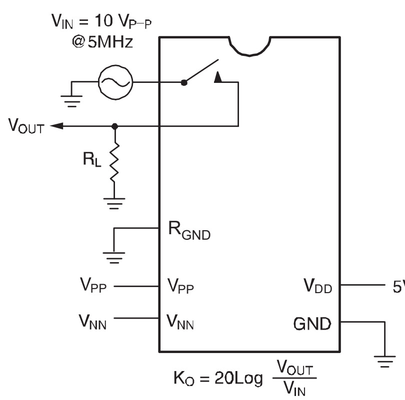
Switch Off Leakage per Switch



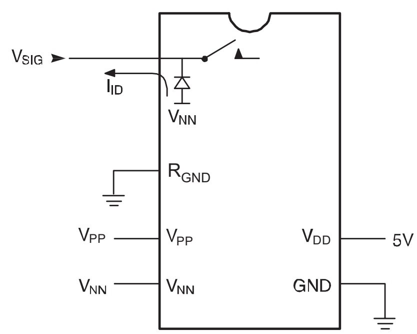
DC Offset Switch ON/OFF



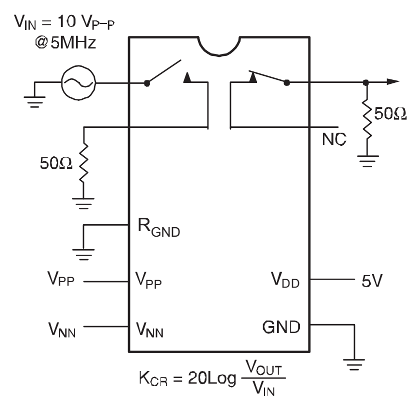
TURN (TON/TOFF) ON/OFF TIME



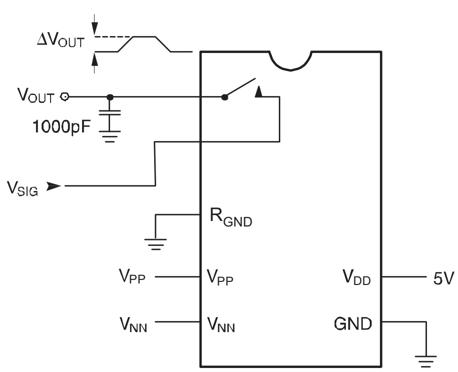
OFF Isolation



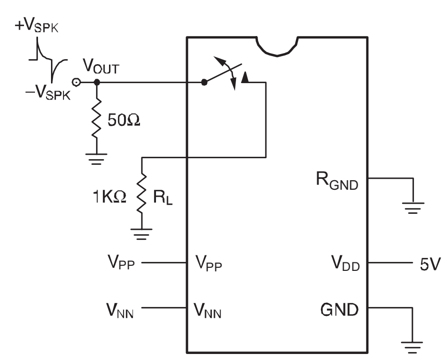
Output Switch Isolation Diode Current



Switch Crosstalk



$Q = 1000pF \times \Delta V_{OUT}$
Charge Injection



Output Voltage Spike

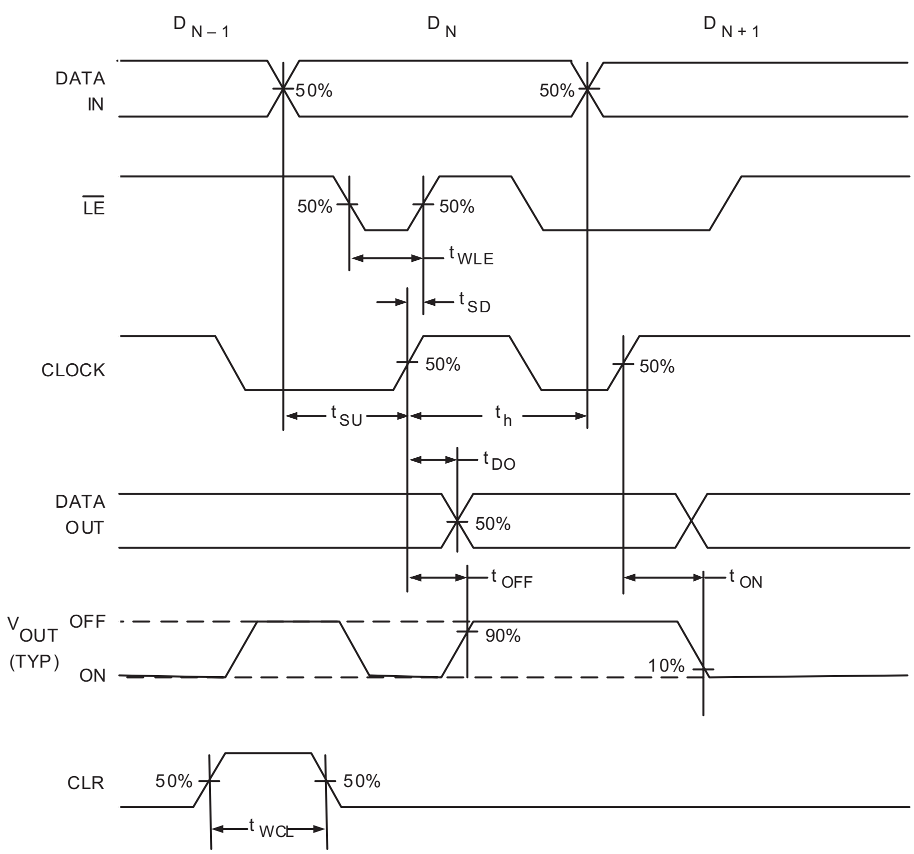
Logic Function Table

INPUT DATA							LATCH ENABLE	CLOCK	OUTPUT SWITCH							
D0	D1	…	D7	D8	…	D15	LE	CL	SW0	SW1	…	SW7	SW8	…	SW15
L							L	L	OFF						
H							L	L	ON						
	L						L	L		OFF					
	H						L	L		ON					
							L	L							
							L	L							
			L				L	L				OFF			
			H				L	L				ON			
		…		L	…		L	L			…		OFF	…	
				H			L	L					ON		
							L	L							
							L	L							
							L	L							
							L	L							
						L	L	L							OFF
						H	L	L							ON
X	X	X	X	X	X	X	H	L	HOLD PREVIOUS STATE						
X	X	X	X	X	X	X	X	H	ALL SWITCHES OFF						

Notes:

1. *Th 16 switches operate independently.*
2. *Serial data is clocked in on the L to H transition of the CLK.*
3. *All 16 switches go to a state retaining their latched condition at the rising edge of LE. When LE is low the shift registers data flow through the latch.*
4. *D_{OUT} is high when data in the register 15 is high.*
5. *Shift registers clocking has no effect on the switch states if LE is high.*
6. *The CL clear input overrides all other inputs.*

Logic Timing Waveforms



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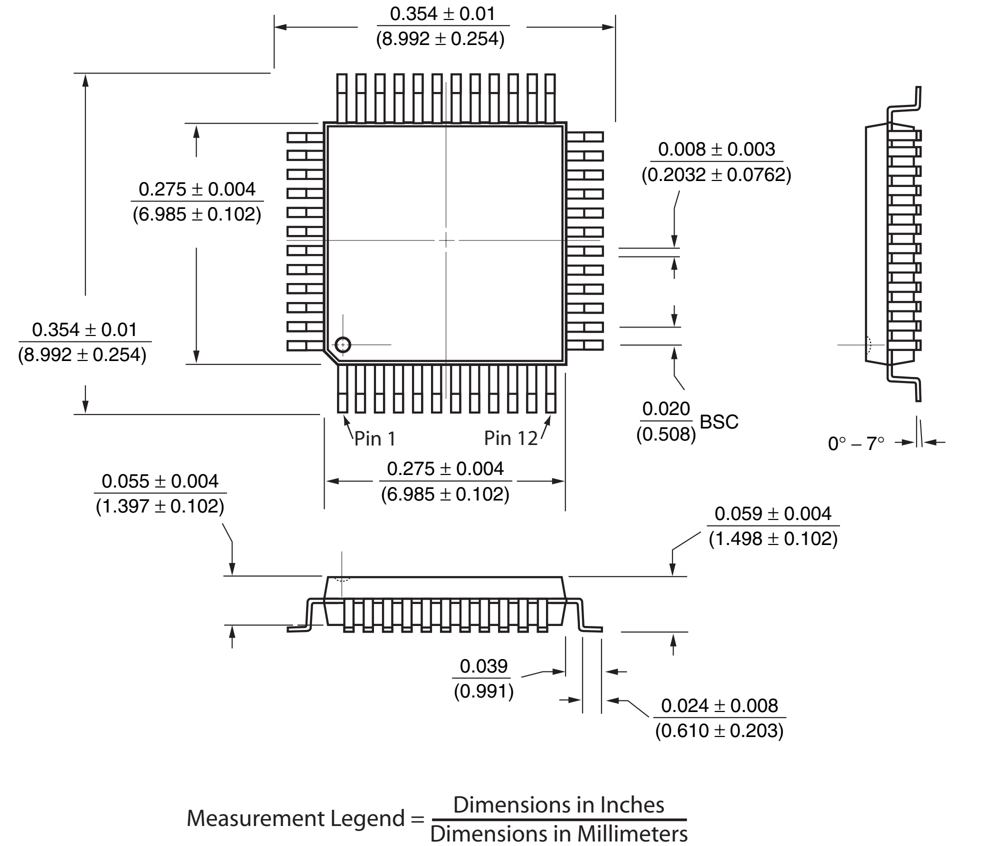
Pin Configuration and Package Outline - 48-Lead TQFP (1.4mm) (FG)

Pin Name	TQFP-48
SW4B	3
SW4A	4
SW3B	5
SW3A	6
SW2B	7
SW2A	8
SW1B	9
SW1A	10
SW0B	11
SW0A	12
V_{NN}	13
V_{PP}	15
GND	17
V_{DD}	18
D_{IN}	19
CLK	20
$\overline{LE}$	21
CLR	22
D_{OUT}	23
RGND	24
SW15B	25
SW15A	26
SW14B	27
SW14A	28
SW13B	29
SW13A	30
SW12B	31
SW12A	32
SW11B	33
SW11A	34
SW10B	37
SW10A	38
SW9B	39
SW9A	40
SW8B	41
SW8A	42
SW7B	43
SW7A	44
SW6B	45
SW6A	46
SW5B	47
SW5A	48
NC	1,2,14,16,35,36

NC = No Internal Connection.



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