FUJITSU MICROELECTRONICS
DATA SHEET

DS07-12618-2E

8-bit Microcontroller

CMOS

F²MC-8FX MB95160 Series

MB95F166D/166D/FV100D-101

DESCRIPTION

The MB95160 series is general-purpose, single-chip microcontrollers. In addition to a compact instruction set, the microcontrollers contain a variety of peripheral functions.

Note : F²MC is the abbreviation of FUJITSU Flexible Microcontroller.

FEATURE

- F²MC-8FX CPU core
  Instruction set optimized for controllers
  - Multiplication and division instructions
  - 16-bit arithmetic operations
  - Bit test branch instruction
  - Bit manipulation instructions etc.
- Clock
  - Main clock
  - Main PLL clock
  - Sub clock
  - Sub PLL clock
- Timer
  - 8/16-bit compound timer × 2 channels
    Can be used to interval timer, PWC timer, PWM timer and input capture.
  - 8/16-bit PPG × 2 channels
  - 16-bit PPG × 1 channel
  - Timebase timer × 1 channel
  - Watch prescaler × 1 channel
- LIN-UART × 1 channel
  - LIN function, clock asynchronous (UART) or clock synchronous (SIO) serial data transfer capable
  - Full duplex double buffer

(Continued)

For the information for microcontroller supports, see the following web site.

http://edevice.fujitsu.com/micom/en-support/

Copyright©2008-2009 FUJITSU MICROELECTRONICS LIMITED All rights reserved
2009.3

(Continued)

- UART/SIO × 1 channel
  Clock asynchronous (UART) or clock synchronous (SIO) serial data transfer capable
  Full duplex double buffer

- I^2C × 1 channel
  Built-in wake-up function
- External interrupt × 8 channels
  Interrupt by edge detection (rising, falling, or both edges can be selected)
  Can be used to recover from low-power consumption (standby) modes.
- 8/10-bit A/D converter × 8 channels
  8-bit or 10-bit resolution can be selected.
- LCD controller (LCDC)
  32 SEG × 4 COM (Max 128 pixels) (Built-in internal division resistance product)
  With blinking function
- Low-power consumption (standby) mode
  Stop mode
  Sleep mode
  Watch mode
  Timebase timer mode
- I/O port
  The number of maximum ports : Max 53
  Port configuration
  - General-purpose I/O ports (N-ch open drain) : 2 ports
  - General-purpose I/O ports (CMOS) : 51 ports
- Programmable input voltage levels of port
  CMOS input level/hysteresis input level
- Flash memory security function (Flash memory device only)
  Protects the content of Flash memory

PRODUCT LINEUP

Parameter \ Part number		MB95F166D	MB95166D
Type		Flash memory product	Mask ROM product
ROM capacity		32 Kbytes	
RAM capacity		1 Kbyte	
Reset output		No	
Option*	Clock system	Dual clock	
	Low voltage detection reset	No	
CPU functions		Number of basic instructions : 136 Instruction bit length : 8 bits Instruction length : 1 to 3 bytes Data bit length : 1, 8, and 16 bits Minimum instruction execution time : 61.5 ns (at machine clock frequency 16.25 MHz) Interrupt processing time : 0.6 µs (at machine clock frequency 16.25 MHz)	
Peripheral functions	Ports (Max 53 ports)	General-purpose I/O port (N-ch open drain) : 2 ports General-purpose I/O port (CMOS) : 51 ports Programmable input voltage levels of port. CMOS input level/hysteresis input level.	
	Timebase timer (1 channel)	Interrupt cycle : 0.5 ms, 2.1 ms, 8.2 ms, 32.8 ms (at main oscillation clock 4 MHz)	
	Watchdog timer	Reset generated cycle At main oscillation clock 10 MHz : Min 105 ms At sub oscillation clock 32.768 kHz (for dual clock product) : Min 250 ms	
	Wild register	Capable of replacing 3 bytes of ROM data	
	I^2C (1 channel)	Master/slave sending and receiving Bus error function and arbitration function Detecting transmitting direction function Start condition repeated generation and detection functions Built-in wake-up function	
	UART/SIO (1 channel)	Data transfer capable in UART/SIO Full duplex double buffer, variable data length (5/6/7/8-bit), built-in baud rate generator NRZ type transfer format, error detected function LSB-first or MSB-first can be selected. Clock synchronous (SIO) or clock asynchronous (UART) serial data transfer capable	
	LIN-UART (1 channel)	Dedicated reload timer allowing a wide range of communication speeds to be set. Full duplex double buffer. Capable of serial data transfer synchronous or asynchronous to clock signal. LIN functions available as the LIN master or LIN slave.	

(Continued)

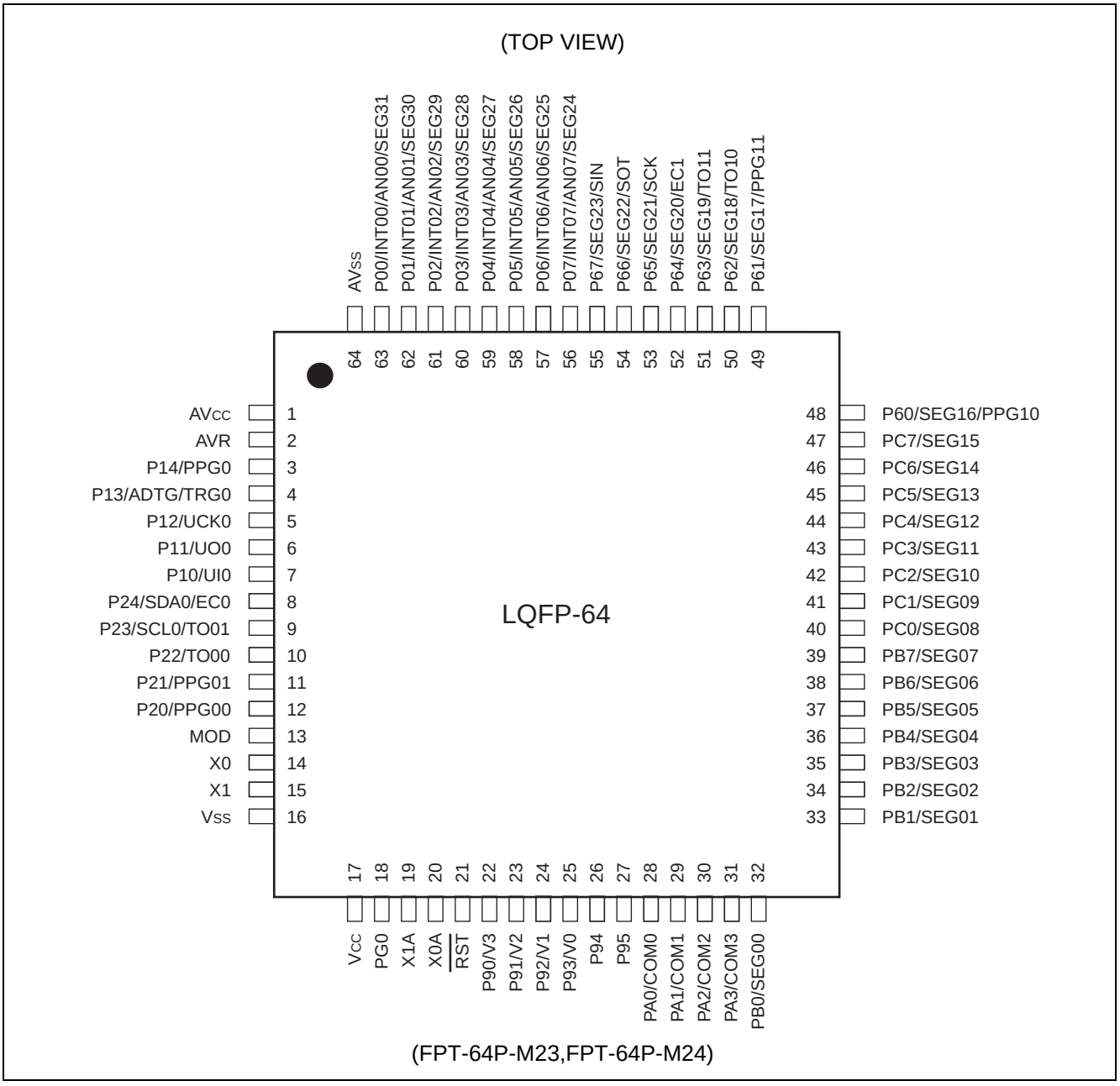
(Continued)

Parameter \ Part number		MB95F166D	MB95166D
Peripheral functions	8/10-bit A/D converter (8 channels)	8-bit or 10-bit resolution can be selected.	
	LCD controller (LCDC)	COM output : 4 (Max) SEG output : 32 (Max) LCD drive power supply (bias) pin : 4 32 SEG × 4 COM : 128 pixels can be displayed. (Built-in internal division resistance product) Duty LCD mode Operable in LCD standby mode Built-in internal division resistance With blinking function	
	8/16-bit compound timer (2 channels)	Each channel of the timer can be used as 8-bit timer × 2 channels or 16-bit timer × 1 channel . Built-in timer function, PWC function, PWM function, capture function, and square wave form output Count clock : 7 internal clocks and external clock can be selected.	
	16-bit PPG (1 channel)	PWM mode or one-shot mode can be selected. Counter operating clock : Eight selectable clock sources Support for external trigger start	
	8/16-bit PPG (2 channels)	Each channel of the PPG can be used as “8-bit PPG × 2 channels” or “16-bit PPG × 1 channel”. Counter operating clock : Eight selectable clock sources	
	Watch counter	Count clock : Four selectable clock sources (125 ms, 250 ms, 500 ms, or 1 s) Counter value can be set from 0 to 63. (Capable of counting for 1 minute when selecting clock source 1 second and setting counter value to 60)	
	Watch prescaler (1 channel)	4 selectable interval times (125 ms, 250 ms, 500 ms, or 1 s)	
	External interrupt (8 channels)	Interrupt by edge detection (rising, falling, or both edges can be selected.) Can be used to recover from standby modes.	
Flash memory		Supports automatic programming, Embedded Algorithm Write/Erase/Erase-Suspend/Resume commands A flag indicating completion of the algorithm Number of write/erase cycles (Min) : 10000 times Data retention time : 20 years Erase can be performed on each block Block protection with external programming voltage Flash Security Feature for protecting the content of the Flash	
Standby mode		Sleep, stop, watch, and timebase timer	

* : For details of option, refer to MASK OPTION .

Note : Part number of the evaluation product in MB95160 series is MB95FV100D-101 (internal division resistance included) . When using it, the MCU board (MB2146-301A) is required.

PIN ASSIGNMENT



PIN DESCRIPTION

Pin no.	Pin name	I/O circuit type*	Function
1	AV_{CC}	—	A/D converter power supply pin.
2	AVR	—	A/D converter reference input pin.
3	P14/PPG0	H	General-purpose I/O port. The pin is shared with 16-bit PPG ch.0 output.
4	P13/TRG0/ ADTG		General-purpose I/O port. The pin is shared with 16-bit PPG ch.0 trigger input (TRG0) and A/D trigger input (ADTG) .
5	P12/UCK0		General-purpose I/O port. The pin is shared with UART/SIO ch.0 clock I/O.
6	P11/UO0		General-purpose I/O port. The pin is shared with UART/SIO ch.0 data output.
7	P10/UI0	G	General-purpose I/O port. The pin is shared with UART/SIO ch.0 data input.
8	P24/EC0/ SDA0	I	General-purpose I/O port. The pin is shared with 8/16-bit compound timer ch.0 clock input (EC0) and I^2C ch.0 data I/O (SDA0) .
9	P23/TO01/ SCL0		General-purpose I/O port. The pin is shared with 8/16-bit compound timer ch.0 output (TO01) and I^2C ch.0 clock I/O (SCL0) .
10	P22/TO00	H	General-purpose I/O port. The pin is shared with 8/16-bit compound timer ch.0 output.
11	P21/PPG01		General-purpose I/O port. The pin is shared with 8/16-bit PPG ch.0 output.
12	P20/PPG00		General-purpose I/O port. The pin is shared with 8/16-bit PPG ch.0 output.
13	MOD	B	Operating mode designation pin.
14	X0	A	Main clock oscillation pins.
15	X1		
16	V_{SS}	—	Power supply pin (GND).
17	V_{CC}	—	Power supply pin.
18	PG0	H	General-purpose I/O port.
19	X1A	A	Sub clock oscillation pins (32 kHz).
20	X0A		
21	$\overline{RST}$	B	Reset pin.
22	P90/V3	R	General-purpose I/O ports. The pins are shared with power supply pin for LCDC drive.
23	P91/V2		
24	P92/V1		
25	P93/V0		

(Continued)

Pin no.	Pin name	I/O circuit type*	Function
26	P94	S	General-purpose I/O ports.
27	P95		
28	PA0/COM0	M	General-purpose I/O ports. The pins are shared with LCDC COM output (COM0 to COM3).
29	PA1/COM1		
30	PA2/COM2		
31	PA3/COM3		
32	PB0/SEG00	M	General-purpose I/O ports. The pins are shared with LCDC SEG output (SEG00 to SEG07).
33	PB1/SEG01		
34	PB2/SEG02		
35	PB3/SEG03		
36	PB4/SEG04		
37	PB5/SEG05		
38	PB6/SEG06		
39	PB7/SEG07		
40	PC0/SEG08	M	General-purpose I/O ports. The pins are shared with LCDC SEG output (SEG08 to SEG15).
41	PC1/SEG09		
42	PC2/SEG10		
43	PC3/SEG11		
44	PC4/SEG12		
45	PC5/SEG13		
46	PC6/SEG14		
47	PC7/SEG15		
48	P60/SEG16/ PPG10	M	General-purpose I/O ports. The pins are shared with LCDC SEG output (SEG16, SEG17) and 8/16-bit PPG ch.1 output (PPG10, PPG11) .
49	P61/SEG17/ PPG11		
50	P62/SEG18/ TO10		General-purpose I/O port. The pin is shared with LCDC SEG output (SEG18) and 8/16-bit compound timer ch.1 output (TO10) .

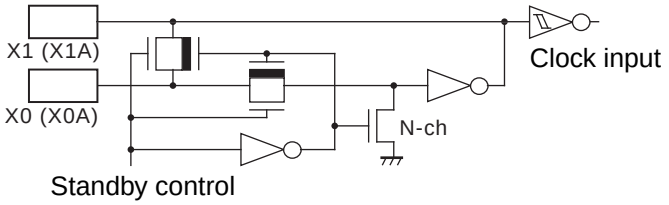
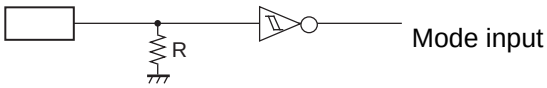
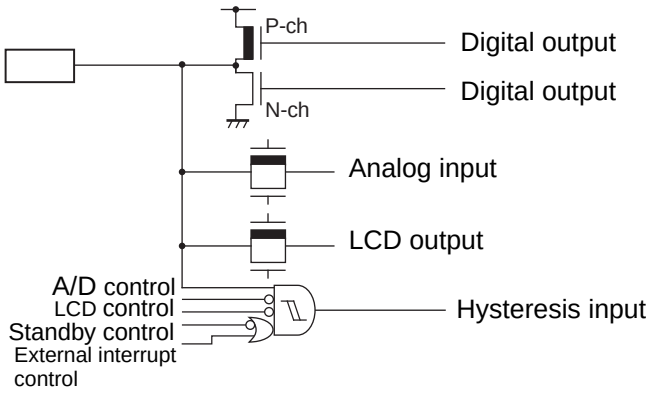
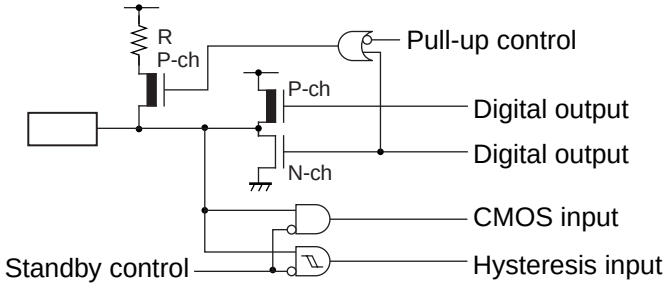
(Continued)

(Continued)

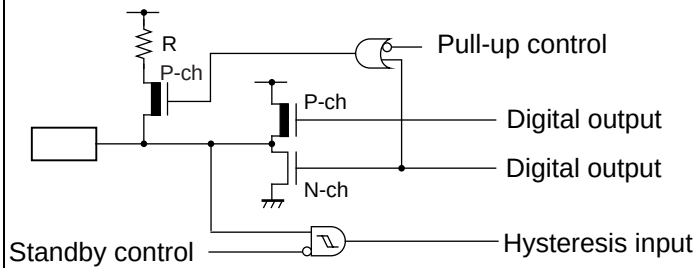
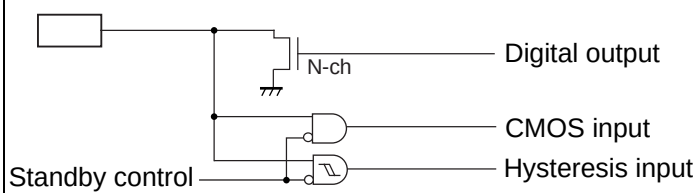
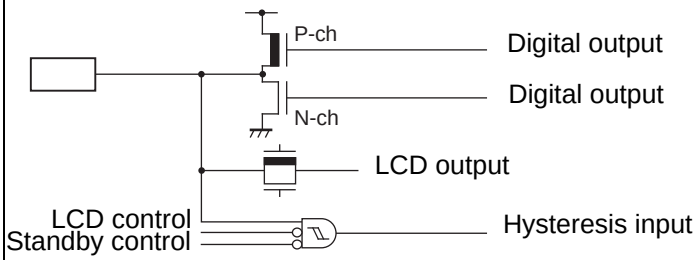
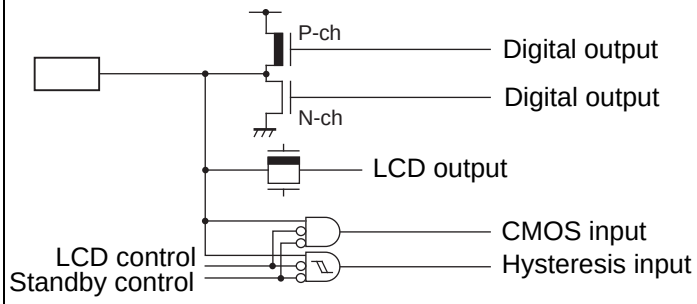
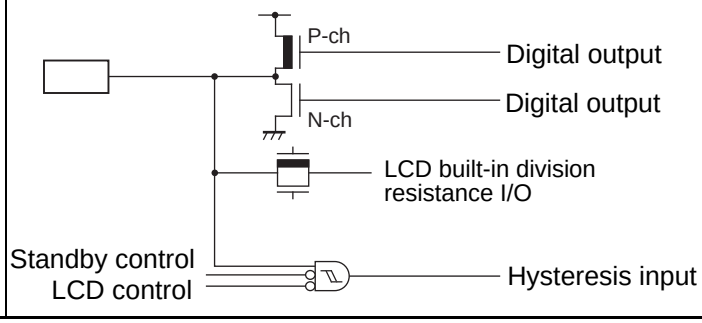
Pin no.	Pin name	I/O circuit type*	Function
51	P63/SEG19/ TO11	M	General-purpose I/O port. The pin is shared with LCDC SEG output (SEG19) and 8/16-bit compound timer ch.1 output (TO11) .
52	P64/SEG20/ EC1		General-purpose I/O port. The pin is shared with LCDC SEG output (SEG20) and 8/16-bit compound timer ch.1 clock input (EC1) .
53	P65/SEG21/ SCK		General-purpose I/O port. The pin is shared with LCDC SEG output (SEG21) and LIN-UART clock I/O (SCK) .
54	P66/SEG22/ SOT		General-purpose I/O port. The pin is shared with LCDC SEG output (SEG22) and LIN-UART data output (SOT) .
55	P67/SEG23/ SIN	N	General-purpose I/O port. The pin is shared with LCDC SEG output (SEG23) and LIN-UART data input (SIN) .
56	P07/INT07/ AN07/SEG24	F	General-purpose I/O port. The pins are shared with external interrupt input (INT00 to INT07) , A/D analog input (AN00 to AN07) and LCDC SEG output (SEG24 to SEG31) .
57	P06/INT06/ AN06/SEG25		
58	P05/INT05/ AN05/SEG26		
59	P04/INT04/ AN04/SEG27		
60	P03/INT03/ AN03/SEG28		
61	P02/INT02/ AN02/SEG29		
62	P01/INT01/ AN01/SEG30		
63	P00/INT00/ AN00/SEG31		
64	AV_{SS}	—	Power supply pin (GND) of A/D converter

* : For the I/O circuit type, refer to I/O CIRCUIT TYPE .

I/O CIRCUIT TYPE

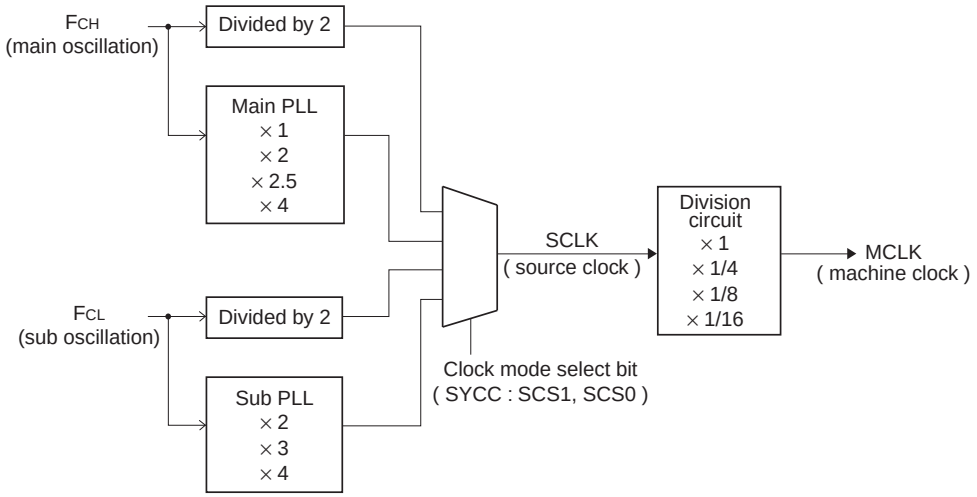
Type	Circuit	Remarks
A		Oscillation circuit High-speed side Feedback resistance : approx. 1 MΩ Low-speed side - Feedback resistance : approx. 24 MΩ (Evaluation product : approx. 10 MΩ) - Dumping resistance : approx.144 kΩ (Evaluation product : without dumping resistance)
B		Only for input Hysteresis input only for Mask ROM product Pull-down resistor only for MODE pin of Mask ROM product
B		Hysteresis input
F		CMOS output LCD output Hysteresis input Analog input
G		CMOS output CMOS input Hysteresis input With pull-up control

(Continued)

Type	Circuit	Remarks
H		CMOS output Hysteresis input With pull-up control
I		N-ch open drain output CMOS input Hysteresis input
M		CMOS output LCD output Hysteresis input
N		CMOS output LCD output CMOS input Hysteresis input
R		CMOS output LCD power supply Hysteresis input

(Continued)

• Outline of clock generation block



HANDLING DEVICES

- Preventing Latch-up

  Care must be taken to ensure that maximum voltage ratings are not exceeded when they are used.
  Latch-up may occur on CMOS ICs if voltage higher than V_{CC} or lower than V_{SS} is applied to input and output pins other than medium- and high-withstand voltage pins or if higher than the rating voltage is applied between V_{CC} pin and V_{SS} pin.
  When latch-up occurs, power supply current increases rapidly and might thermally damage elements.

- Stable Supply Voltage

  Supply voltage should be stabilized.
  A sudden change in power-supply voltage may cause a malfunction even within the guaranteed operating range of the Vcc power-supply voltage.
  For stabilization, in principle, keep the variation in Vcc ripple (p-p value) in a commercial frequency range (50/60 Hz) not to exceed 10% of the standard Vcc value and suppress the voltage variation so that the transient variation rate does not exceed 0.1 V/ms during a momentary change such as when the power supply is switched.

- Precautions for Use of External Clock

  Even when an external clock is used, oscillation stabilization wait time is required for power-on reset, wake-up from sub clock mode or stop mode.

- Serial Communication

  There is a possibility to receive wrong data due to the noise or other causes on the serial communication.
  Therefore, design a printed circuit board so as to avoid noise.
  Retransmit the data if an error occurs because of applying the checksum to the last data in consideration of receiving wrong data due to the noise.

PIN CONNECTION

- Treatment of Unused Pin

  Leaving unused input pins unconnected can cause abnormal operation or latch-up, leaving to permanent damage. Unused input pins should always be pulled up or down through resistance of at least 2 kΩ. Any unused input/output pins may be set to output mode and left open, or set to input mode and treated the same as unused input pins. If there is unused output pin, make it to open.

- Power Supply Pins

  In products with multiple V_{CC} or V_{SS} pins, the pins of the same potential are internally connected in the device to avoid abnormal operations including latch-up. However, you must connect the pins to external power supply and a ground line to lower the electro-magnetic emission level, to prevent abnormal operation of strobe signals caused by the rise in the ground level, and to conform to the total output current rating.
  Moreover, connect the current supply source with the V_{CC} and V_{SS} pins of this device at the low impedance.

  It is also advisable to connect a ceramic bypass capacitor of approximately 0.1 µF between V_{CC} and V_{SS} pins near this device.

- Mode Pin (MOD)

  Connect the MOD pin directly to V_{CC} or V_{SS}.

  To prevent the device unintentionally entering test mode due to noise, lay out the printed circuit board so as to minimize the distance from the MOD pin to V_{CC} or V_{SS} and to provide a low-impedance connection.

- Analog Power Supply

  Always set the same potential to AV_{CC} and V_{CC} pins. When $V_{CC} > AV_{CC}$, the current may flow through the AN00 to AN07 pins.

- Treatment of Power Supply Pins on A/D Converter

  Connect to be $AV_{CC} = V_{CC}$ and $AV_{SS} = AVR = V_{SS}$ even if the A/D converter is not in use.

  Noise riding on the AV_{CC} pin may cause accuracy degradation. So, connect approx. 0.1 μF ceramic capacitor as a bypass capacitor between AV_{CC} and AV_{SS} pins in the vicinity of this device.

PROGRAMMING FLASH MEMORY MICROCONTROLLERS USING PARALLEL PROGRAMMER

- **Supported Parallel Programmers and Adapters**

The following table lists supported parallel programmers and adapters.

Package	Applicable adapter model	Parallel programmers
FPT-64P-M23	TEF110-95F168HPMC	AF9708 (Ver 02.35G or more) AF9709/B (Ver 02.35G or more) AF9723+AF9834 (Ver 02.08E or more)
FPT-64P-M24	TEF110-95F168HPMC1	

Note : For information on applicable adapter models and parallel programmers, contact the following:
Flash Support Group, Inc. TEL: +81-53-428-8380

- **Sector Configuration**

The individual sectors of Flash memory correspond to addresses used for CPU access and programming by the parallel programmer as follows:

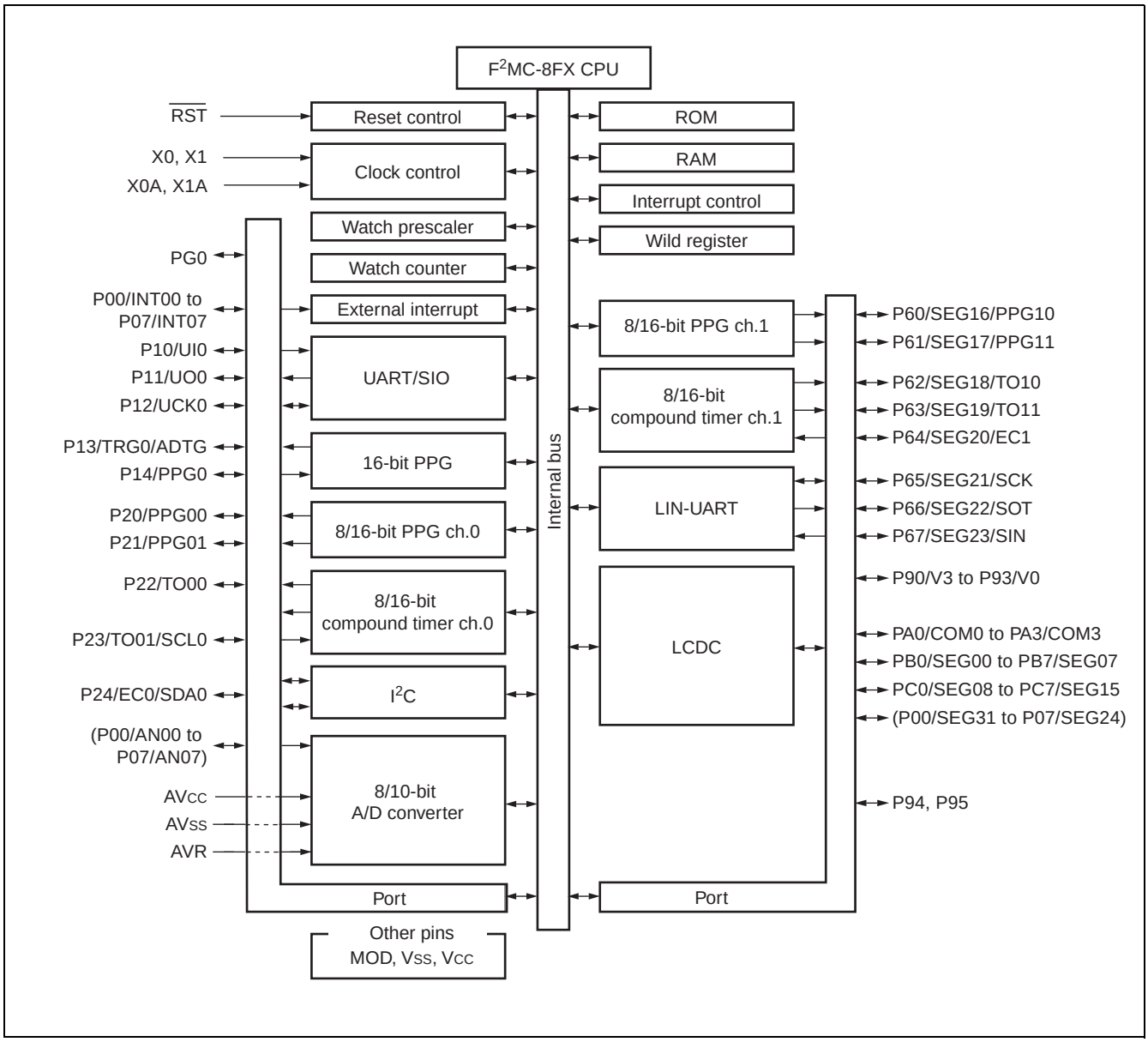
Flash memory	CPU address	Programmer address*
32 Kbytes	8000_H	18000_H
	$FFFF_H$	$1FFFF_H$

*: Programmer addresses are corresponding to CPU addresses, used when the parallel programmer programs data into Flash memory.
These programmer addresses are used for the parallel programmer to program or erase data in Flash memory.

- **Programming Method**

1) Set the type code of the parallel programmer to 17222 .
2) Load program data to programmer addresses 18000_H to $1FFFF_H$.
3) Programmed by parallel programmer

BLOCK DIAGRAM

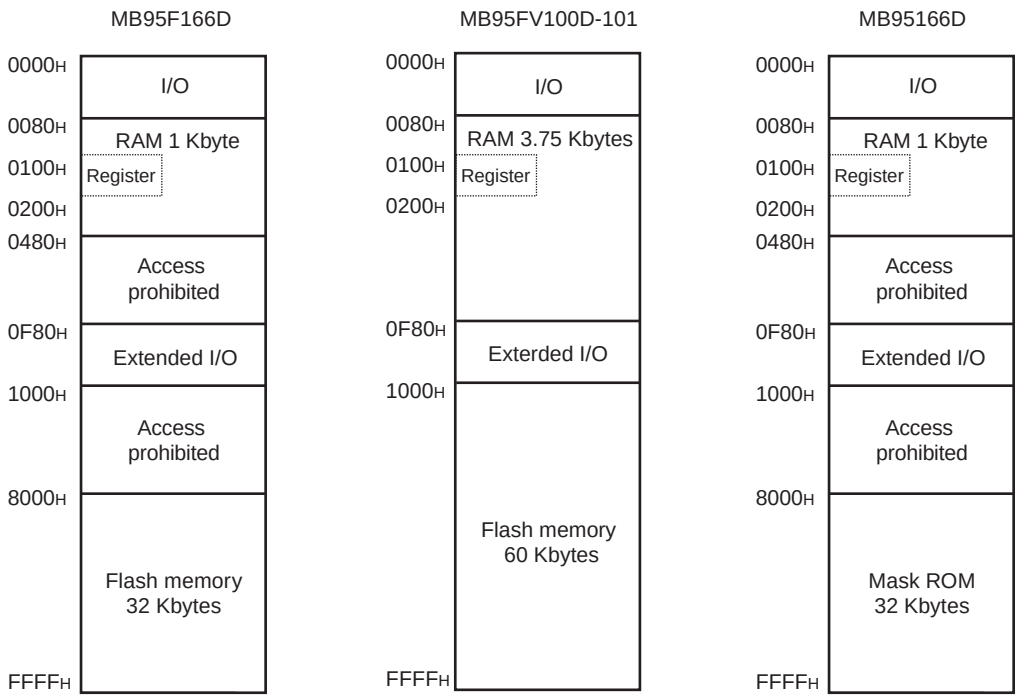


CPU CORE

1. Memory space

Memory space of the MB95160 series is 64 Kbytes and consists of I/O area, data area, and program area. The memory space includes special-purpose areas such as the general-purpose registers and vector table.

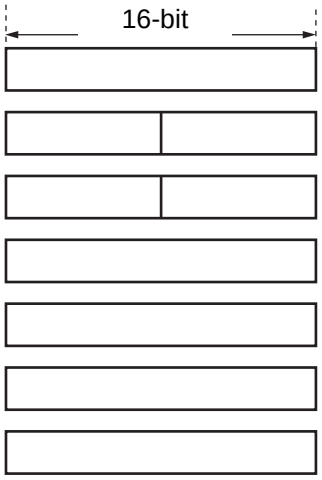
Memory Map



2. Register

The MB95160 series has two types of registers; dedicated registers in the CPU and general-purpose registers in the memory. The dedicated registers are as follows:

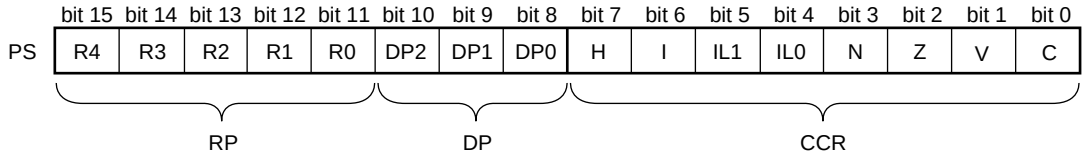
Program counter (PC)	:	A 16-bit register to indicate locations where instructions are stored.
Accumulator (A)	:	A 16-bit register for temporary storage of arithmetic operations. In the case of an 8-bit data processing instruction, the lower 1 byte is used.
Temporary accumulator (T)	:	A 16-bit register which performs arithmetic operations with the accumulator. In the case of an 8-bit data processing instruction, the lower 1 byte is used.
Index register (IX)	:	A 16-bit register for index modification.
Extra pointer (EP)	:	A 16-bit pointer to point to a memory address.
Stack pointer (SP)	:	A 16-bit register to indicate a stack area.
Program status (PS)	:	A 16-bit register for storing a register bank pointer, a direct bank pointer, and a condition code register.



	Initial Value
: Program counter	FFFD$_H$
: Accumulator	0000$_H$
: Temporary accumulator	0000$_H$
: Index register	0000$_H$
: Extra pointer	0000$_H$
: Stack pointer	0000$_H$
: Program status	0030$_H$

The PS can further be divided into higher 8 bits for use as a register bank pointer (RP) and a direct bank pointer (DP) and the lower 8 bits for use as a condition code register (CCR) .

- Structure of the Program Status

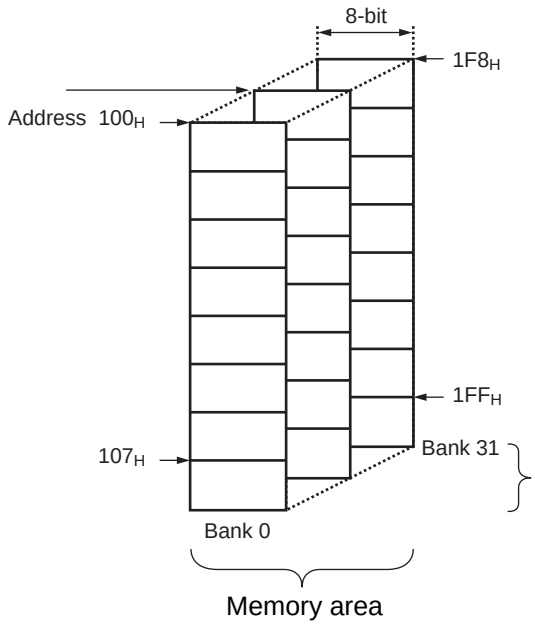


The following general-purpose registers are provided:

General-purpose registers: 8-bit data storage registers

The general-purpose registers are 8 bits and located in the register banks on the memory. 1-bank contains 8-register. Up to a total of 32 banks can be used on the MB95160 series. The bank currently in use is specified by the register bank pointer (RP), and the lower 3 bits of OP code indicates the general-purpose register 0 (R0) to general-purpose register 7 (R7).

Register Bank Configuration



32 banks (RAM area)
The number of banks is limited by the usable RAM capacitance.

Address	Register abbreviation	Register name	R/W	Initial value
002A$_H$	PDRG	Port G data register	R/W	00000000$_B$
002B$_H$	DDRG	Port G direction register	R/W	00000000$_B$
002C$_H$	—	(Disabled)	—	—
002D$_H$	PUL1	Port 1 pull-up register	R/W	00000000$_B$
002E$_H$	PUL2	Port 2 pull-up register	R/W	00000000$_B$
002F$_H$ to 0034$_H$	—	(Disabled)	—	—
0035$_H$	PULG	Port G pull-up control register	R/W	00000000$_B$
0036$_H$	T01CR1	8/16-bit compound timer 01 control status register 1 ch.0	R/W	00000000$_B$
0037$_H$	T00CR1	8/16-bit compound timer 00 control status register 1 ch.0	R/W	00000000$_B$
0038$_H$	T11CR1	8/16-bit compound timer 11 control status register 1 ch.1	R/W	00000000$_B$
0039$_H$	T10CR1	8/16-bit compound timer 10 control status register 1 ch.1	R/W	00000000$_B$
003A$_H$	PC01	8/16-bit PPG1 control register ch.0	R/W	00000000$_B$
003B$_H$	PC00	8/16-bit PPG0 control register ch.0	R/W	00000000$_B$
003C$_H$	PC11	8/16-bit PPG1 control register ch.1	R/W	00000000$_B$
003D$_H$	PC10	8/16-bit PPG0 control register ch.1	R/W	00000000$_B$
003E$_H$ to 0041$_H$	—	(Disabled)	—	—
0042$_H$	PCNTH0	16-bit PPG status control register (upper byte) ch.0	R/W	00000000$_B$
0043$_H$	PCNTL0	16-bit PPG status control register (lower byte) ch.0	R/W	00000000$_B$
0044$_H$ to 0047$_H$	—	(Disabled)	—	—
0048$_H$	EIC00	External interrupt circuit control register ch.0/ch.1	R/W	00000000$_B$
0049$_H$	EIC10	External interrupt circuit control register ch.2/ch.3	R/W	00000000$_B$
004A$_H$	EIC20	External interrupt circuit control register ch.4/ch.5	R/W	00000000$_B$
004B$_H$	EIC30	External interrupt circuit control register ch.6/ch.7	R/W	00000000$_B$
004C$_H$ to 004F$_H$	—	(Disabled)	—	—
0050$_H$	SCR	LIN-UART serial control register	R/W	00000000$_B$
0051$_H$	SMR	LIN-UART serial mode register	R/W	00000000$_B$
0052$_H$	SSR	LIN-UART serial status register	R/W	00001000$_B$
0053$_H$	RDR/TDR	LIN-UART reception/transmission data register	R/W	00000000$_B$
0054$_H$	ESCR	LIN-UART extended status control register	R/W	00000100$_B$

(Continued)

Address	Register abbreviation	Register name	R/W	Initial value
0055H	ECCR	LIN-UART extended communication control register	R/W	000000XXB
0056H	SMC10	UART/SIO serial mode control register 1 ch.0	R/W	00000000B
0057H	SMC20	UART/SIO serial mode control register 2 ch.0	R/W	00100000B
0058H	SSR0	UART/SIO serial status register ch.0	R/W	00000001B
0059H	TDR0	UART/SIO serial output data register ch. 0	R/W	00000000B
005AH	RDR0	UART/SIO serial input data register ch.0	R	00000000B
005BH to 005FH	—	(Disabled)	—	—
0060H	IBCR00	I²C bus control register 0 ch.0	R/W	00000000B
0061H	IBCR10	I²C bus control register 1 ch.0	R/W	00000000B
0062H	IBSR0	I²C bus status register ch.0	R	00000000B
0063H	IDDR0	I²C data register ch.0	R/W	00000000B
0064H	IAAR0	I²C address register ch.0	R/W	00000000B
0065H	ICCR0	I²C clock control register ch.0	R/W	00000000B
0066H to 006BH	—	(Disabled)	—	—
006CH	ADC1	8/10-bit A/D converter control register 1	R/W	00000000B
006DH	ADC2	8/10-bit A/D converter control register 2	R/W	00000000B
006EH	ADDH	8/10-bit A/D converter data register (upper byte)	R/W	00000000B
006FH	ADDL	8/10-bit A/D converter data register (lower byte)	R/W	00000000B
0070H	WCSR	Watch counter status register	R/W	00000000B
0071H	—	(Disabled)	—	—
0072H	FSR*	Flash memory status register	R/W	000X0000B
0073H	—	(Disabled)	—	—
0074H	—	(Disabled)	—	—
0075H	—	(Disabled)	—	—
0076H	WREN	Wild register address compare enable register	R/W	00000000B
0077H	WROR	Wild register data test setting register	R/W	00000000B
0078H	—	Register bank pointer (RP) , Mirror of direct bank pointer (DP)	—	—
0079H	ILR0	Interrupt level setting register 0	R/W	11111111B
007AH	ILR1	Interrupt level setting register 1	R/W	11111111B
007BH	ILR2	Interrupt level setting register 2	R/W	11111111B
007CH	ILR3	Interrupt level setting register 3	R/W	11111111B

(Continued)

Address	Register abbreviation	Register name	R/W	Initial value
007D$_H$	ILR4	Interrupt level setting register 4	R/W	11111111$_B$
007E$_H$	ILR5	Interrupt level setting register 5	R/W	11111111$_B$
007F$_H$	—	(Disabled)	—	—
0F80$_H$	WRARH0	Wild register address setting register (upper byte) ch.0	R/W	00000000$_B$
0F81$_H$	WRARL0	Wild register address setting register (lower byte) ch.0	R/W	00000000$_B$
0F82$_H$	WRDR0	Wild register data setting register ch.0	R/W	00000000$_B$
0F83$_H$	WRARH1	Wild register address setting register (upper byte) ch.1	R/W	00000000$_B$
0F84$_H$	WRARL1	Wild register address setting register (lower byte) ch.1	R/W	00000000$_B$
0F85$_H$	WRDR1	Wild register data setting register ch.1	R/W	00000000$_B$
0F86$_H$	WRARH2	Wild register address setting register (upper byte) ch.2	R/W	00000000$_B$
0F87$_H$	WRARL2	Wild register address setting register (lower byte) ch.2	R/W	00000000$_B$
0F88$_H$	WRDR2	Wild register data setting register ch.2	R/W	00000000$_B$
0F89$_H$ to 0F91$_H$	—	(Disabled)	—	—
0F92$_H$	T01CR0	8/16-bit compound timer 01 control status register 0 ch.0	R/W	00000000$_B$
0F93$_H$	T00CR0	8/16-bit compound timer 00 control status register 0 ch.0	R/W	00000000$_B$
0F94$_H$	T01DR	8/16-bit compound timer 01 data register ch.0	R/W	00000000$_B$
0F95$_H$	T00DR	8/16-bit compound timer 00 data register ch.0	R/W	00000000$_B$
0F96$_H$	TMCR0	8/16-bit compound timer 00/01 timer mode control register ch.0	R/W	00000000$_B$
0F97$_H$	T11CR0	8/16-bit compound timer 11 control status register 0 ch.1	R/W	00000000$_B$
0F98$_H$	T10CR0	8/16-bit compound timer 10 control status register 0 ch.1	R/W	00000000$_B$
0F99$_H$	T11DR	8/16-bit compound timer 11 data register ch.1	R/W	00000000$_B$
0F9A$_H$	T10DR	8/16-bit compound timer 10 data register ch.1	R/W	00000000$_B$
0F9B$_H$	TMCR1	8/16-bit compound timer 10/11 timer mode control register ch.1	R/W	00000000$_B$
0F9C$_H$	PPS01	8/16-bit PPG1 cycle setting buffer register ch.0	R/W	11111111$_B$
0F9D$_H$	PPS00	8/16-bit PPG0 cycle setting buffer register ch.0	R/W	11111111$_B$
0F9E$_H$	PDS01	8/16-bit PPG1 duty setting buffer register ch.0	R/W	11111111$_B$
0F9F$_H$	PDS00	8/16-bit PPG0 duty setting buffer register ch.0	R/W	11111111$_B$
0FA0$_H$	PPS11	8/16-bit PPG1 cycle setting buffer register ch.1	R/W	11111111$_B$
0FA1$_H$	PPS10	8/16-bit PPG0 cycle setting buffer register ch.1	R/W	11111111$_B$
0FA2$_H$	PDS11	8/16-bit PPG1 duty setting buffer register ch.1	R/W	11111111$_B$
0FA3$_H$	PDS10	8/16-bit PPG0 duty setting buffer register ch.1	R/W	11111111$_B$
0FA4$_H$	PPGS	8/16-bit PPG start register	R/W	00000000$_B$

(Continued)

Address	Register abbreviation	Register name	R/W	Initial value
0FA5H	REVC	8/16-bit PPG output inversion register	R/W	00000000B
0FA6H to 0FA9H	—	(Disabled)	—	—
0FAAH	PDCRH0	16-bit PPG down counter register (upper byte) ch.0	R	00000000B
0FABH	PDCRL0	16-bit PPG down counter register (lower byte) ch.0	R	00000000B
0FACH	PCSRH0	16-bit PPG cycle setting buffer register (upper byte) ch.0	R/W	11111111B
0FADH	PCSRL0	16-bit PPG cycle setting buffer register (lower byte) ch.0	R/W	11111111B
0FAEH	PDUTH0	16-bit PPG duty setting buffer register (upper byte) ch.0	R/W	11111111B
0FAFH	PDUTL0	16-bit PPG duty setting buffer register (lower byte) ch.0	R/W	11111111B
0FB0H to 0FBBH	—	(Disabled)	—	—
0FBCH	BGR1	LIN-UART baud rate generator register 1	R/W	00000000B
0FBDH	BGR0	LIN-UART baud rate generator register 0	R/W	00000000B
0FBEH	PSSR0	UART/SIO dedicated baud rate generator prescaler selecting register ch.0	R/W	00000000B
0FBFH	BRSR0	UART/SIO dedicated baud rate generator setting register ch.0	R/W	00000000B
0FC0H to 0FC2H	—	(Disabled)	—	—
0FC3H	AIDRL	A/D input disable register (lower byte)	R/W	00000000B
0FC4H	LCDCC	LCDC control register	R/W	00010000B
0FC5H	LCDCE1	LCDC enable register 1	R/W	00110000B
0FC6H	LCDCE2	LCDC enable register 2	R/W	00000000B
0FC7H	LCDCE3	LCDC enable register 3	R/W	00000000B
0FC8H	LCDCE4	LCDC enable register 4	R/W	00000000B
0FC9H	LCDCE5	LCDC enable register 5	R/W	00000000B
0FCAH	—	(Disabled)	—	—
0FCBH	LCDCB1	LCDC blinking setting register 1	R/W	00000000B
0FCCH	LCDCB2	LCDC blinking setting register 2	R/W	00000000B
0FCDH to 0FDCH	LCDRAM	LCDC display RAM	R/W	00000000B
0FDDH to 0FE2H	—	(Disabled)	—	—
0FE3H	WCDR	Watch counter data register	R/W	00111111B

(Continued)

INTERRUPT SOURCE TABLE

Interrupt source	Interrupt request number	Vector table address		Bit name of interrupt level setting register	Same level priority order (at simultaneous occurrence)
		Upper	Lower		
External interrupt ch.0	IRQ0	FFFA$_H$	FFFB$_H$	L00 [1 : 0]	High
External interrupt ch.4					
External interrupt ch.1	IRQ1	FFF8$_H$	FFF9$_H$	L01 [1 : 0]	
External interrupt ch.5					
External interrupt ch.2	IRQ2	FFF6$_H$	FFF7$_H$	L02 [1 : 0]	
External interrupt ch.6					
External interrupt ch.3	IRQ3	FFF4$_H$	FFF5$_H$	L03 [1 : 0]	
External interrupt ch.7					
UART/SIO ch.0	IRQ4	FFF2$_H$	FFF3$_H$	L04 [1 : 0]	
8/16-bit compound timer ch.0 (Lower)	IRQ5	FFF0$_H$	FFF1$_H$	L05 [1 : 0]	
8/16-bit compound timer ch.0 (Upper)	IRQ6	FFEE$_H$	FFEF$_H$	L06 [1 : 0]	
LIN-UART (reception)	IRQ7	FFEC$_H$	FFED$_H$	L07 [1 : 0]	
LIN-UART (transmission)	IRQ8	FFEA$_H$	FFEB$_H$	L08 [1 : 0]	
8/16-bit PPG ch.1 (Lower)	IRQ9	FFE8$_H$	FFE9$_H$	L09 [1 : 0]	
8/16-bit PPG ch.1 (Upper)	IRQ10	FFE6$_H$	FFE7$_H$	L10 [1 : 0]	
(Unused)	IRQ11	FFE4$_H$	FFE5$_H$	L11 [1 : 0]	
8/16-bit PPG ch.0 (Upper)	IRQ12	FFE2$_H$	FFE3$_H$	L12 [1 : 0]	
8/16-bit PPG ch.0 (Lower)	IRQ13	FFE0$_H$	FFE1$_H$	L13 [1 : 0]	
8/16-bit compound timer ch.1 (Upper)	IRQ14	FFDE$_H$	FFDF$_H$	L14 [1 : 0]	
16-bit PPG ch.0	IRQ15	FFDC$_H$	FFDD$_H$	L15 [1 : 0]	
I^2C ch.0	IRQ16	FFDA$_H$	FFDB$_H$	L16 [1 : 0]	
(Unused)	IRQ17	FFD8$_H$	FFD9$_H$	L17 [1 : 0]	
8/10-bit A/D converter	IRQ18	FFD6$_H$	FFD7$_H$	L18 [1 : 0]	
Timebase timer	IRQ19	FFD4$_H$	FFD5$_H$	L19 [1 : 0]	
Watch prescaler/Watch counter	IRQ20	FFD2$_H$	FFD3$_H$	L20 [1 : 0]	
(Unused)	IRQ21	FFD0$_H$	FFD1$_H$	L21 [1 : 0]	
8/16-bit compound timer ch.1 (Lower)	IRQ22	FFCE$_H$	FFCF$_H$	L22 [1 : 0]	
Flash memory	IRQ23	FFCC$_H$	FFCD$_H$	L23 [1 : 0]	Low

ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage*1	V_{CC}, AV_{CC}	Vss – 0.3	Vss + 4.0	V	*2
	AVR	Vss – 0.3	Vss + 4.0		*2
Power supply voltage for LCD	V0 to V3	V_{SS} – 0.3	V_{SS} + 4.0	V	*3
Input voltage*1	V_I	Vss – 0.3	Vss + 6.0	V	P23, P24*4
		Vss – 0.3	Vss + 4.0	V	Other than P23, P24*4
Output voltage*1	V_O	Vss – 0.3	Vss + 4.0	V	*4
Maximum clamp current	I_{CLAMP}	– 2.0	+ 2.0	mA	Applicable to pins*5
Total maximum clamp current	$\Sigma\lvert I_{CLAMP}\rvert$	—	20	mA	Applicable to pins*5
L level maximum output current	I_{OL}	—	15	mA	Applicable to pins*5
L level average current	I_{OLAV}	—	4	mA	Applicable to pins*5 Average output current = operating current × operating ratio (1 pin)
L level total maximum output current	ΣI_{OL}	—	100	mA	
L level total average output current	ΣI_{OLAV}	—	50	mA	Total average output current = operating current × operating ratio (Total of pins)
H level maximum output current	I_{OH}	—	– 15	mA	Applicable to pins*5
H level average current	I_{OHAV}	—	– 4	mA	Applicable to pins*5 Average output current = operating current × operating ratio (1 pin)
H level total maximum output current	ΣI_{OH}	—	– 100	mA	
H level total average output current	ΣI_{OHAV}	—	– 50	mA	Total average output current = operating current × operating ratio (Total of pins)
Power consumption	Pd	—	320	mW	
Operating temperature	T_A	– 40	+ 85	°C	
Storage temperature	Tstg	– 55	+ 150	°C	

*1 : The parameter is based on V_{SS} = 0.0 V.

*2 : Apply equal potential to AV_{CC} and V_{CC}. AVR should not exceed AV_{CC} + 0.3 V.

(Continued)

(Continued)

*3 : V0 to V3 should not exceed V_{CC} + 0.3 V.

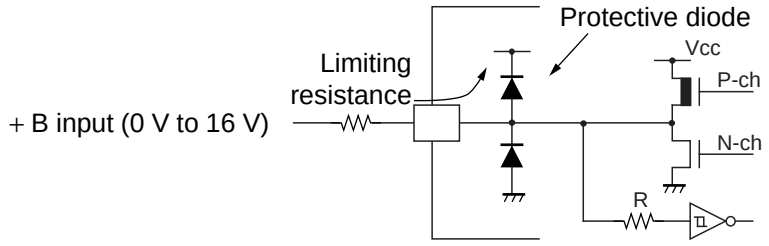
*4 : V_I and Vo should not exceed V_{CC} + 0.3 V. V_I must not exceed the rating voltage. However, if the maximum current to/from an input is limited by some means with external components, the I_{CLAMP} rating supersedes the V_I rating.

*5 : Applicable to pins :

P00 to P07, P10 to P14, P20 to P22,P60 to P67, P90 to P95, PA0 to PA3, PB0 to PB7, PC0 to PC7

- Use within recommended operating conditions.
- Use at DC voltage (current).
- +B signal is an input signal that exceeds V_{CC} voltage. The + B signal should always be applied a limiting resistance placed between the + B signal and the microcontroller.
- The value of the limiting resistance should be set so that when the + B signal is applied the input current to the microcontroller pin does not exceed rated values, either instantaneously or for prolonged periods.
- Note that when the microcontroller drive current is low, such as in the power saving modes, the +B input potential may pass through the protective diode and increase the potential at the V_{CC} pin, and this affects other devices.
- Note that if the + B signal is inputted when the microcontroller power supply is off (not fixed at 0 V), the power supply is provided from the pins, so that incomplete operation may result.
- Note that if the + B input is applied during power-on, the power supply is provided from the pins and the resulting power supply voltage may not be sufficient to operate the power-on reset.
- Care must be taken not to leave the + B input pin open.
- Note that analog system input/output pins other than the A/D input pins (LCD drive pins, etc.) cannot accept + B signal input.
- Sample recommended circuits :

• Input/Output Equivalent circuits



WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

3. DC Characteristics

(Vcc = 3.3 V, Vss = 0.0 V, T_A = − 40 °C to + 85 °C)

Parameter	Sym-bol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
H level input voltage	V_{IH1}	P10, P67	—	0.7 V_{CC}	—	V_{CC} + 0.3	V	When selecting CMOS input level
	V_{IH2}	P23, P24	—	0.7 V_{CC}	—	V_{SS} + 6.0	V	
	V_{IHS1}	P00 to P07, P10 to P14, P20 to P22, P60 to P67, P90 to P95, PA0 to PA3, PB0 to PB7, PC0 to PC7	—	0.8 V_{CC}	—	V_{CC} + 0.3	V	Hysteresis input
	V_{IHS2}	P23, P24	—	0.8 V_{CC}	—	V_{SS} + 5.5	V	
	V_{IHM}	$\overline{RST}$, MOD	—	0.7 V_{CC}	—	V_{CC} + 0.3	V	CMOS input (Flash Memory product)
				0.8 V_{CC}	—	V_{CC} + 0.3	V	Hysteresis input (Mask ROM product)
L level input voltage	V_{IL}	P10,P23, P24,P67	—	V_{SS} − 0.3	—	0.3 V_{CC}	V	When selecting CMOS input level
	V_{ILS}	P00 to P07, P10 to P14, P20 to P24, P60 to P67, P90 to P95, PA0 to PA3, PB0 to PB7, PC0 to PC7	—	V_{SS} − 0.3	—	0.2 V_{CC}	V	Hysteresis input
	V_{ILM}	$\overline{RST}$, MOD	—	V_{SS} − 0.3	—	0.2 V_{CC}	V	Hysteresis input (Mask ROM product)
				V_{SS} − 0.3	—	0.3 V_{CC}	V	CMOS input (Flash Memory product)
H level output voltage	V_{OH}	Output pins other than P23, P24	I_{OH} = 4.0 mA	2.4	—	—	V	
L level output voltage	V_{OL}	Output pins other than $\overline{RST}$	I_{OL} = 4.0 mA	—	—	0.4	V	
Input leakage current (Hi-Z output leakage current)	I_{LI}	Ports other than P23, P24	0.0 V < V_I < V_{CC}	− 5	—	+ 5	µA	When the pull-up prohibition setting

(Continued)

(Vcc = 3.3 V,Vss = 0.0 V, T_A = − 40 °C to + 85 °C)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Open-drain output leakage current	I_{LIOD}	P23, P24	0.0 V < V_I < V_{SS} + 5.5 V	—	—	5	µA	
Pull-up resistor	R_{PULL}	P10 to P14, P20 to P22	V_I = 0.0 V	25	50	100	kΩ	When the pull-up permission setting
Pull-down resistor	R_{MOD}	MOD	V_I = Vcc	25	50	100	kΩ	Mask ROM product
Input capacitance	C_{IN}	Other than AV_{CC}, AV_{SS}, AVR, V_{CC}, V_{SS}	f = 1 MHz	—	5	15	pF	
Power supply current*	I_{CC}	V_{CC} (External clock operation)	F_{CH} = 20 MHz F_{MP} = 10 MHz Main clock mode (divided by 2)	—	11.0	14.0	mA	MB95F166D At other than Flash memory writing and erasing
				—	30.0	35.0	mA	MB95F166D At Flash memory writing and erasing
				—	7.3	10.0	mA	MB95166D
			F_{CH} = 32 MHz F_{MP} = 16 MHz Main clock mode (divided by 2)	—	17.6	22.4	mA	MB95F166D At other than Flash memory writing and erasing
				—	38.1	44.9	mA	MB95F166D At Flash memory writing and erasing
				—	11.7	16.0	mA	MB95166D
	I_{CCS}		F_{CH} = 20 MHz F_{MP} = 10 MHz Main Sleep mode (divided by 2)	—	4.5	6.0	mA	
			F_{CH} = 32 MHz F_{MP} = 16 MHz Main Sleep mode (divided by 2)	—	7.2	9.6	mA	
	I_{CCL}		F_{CL} = 32 kHz F_{MPL} = 16 kHz Sub clock mode (divided by 2)	—	25	35	µA	
	I_{CCLS}		F_{CL} = 32 kHz F_{MPL} = 16 kHz Sub sleep mode (divided by 2)	—	7	15	µA	

(Continued)

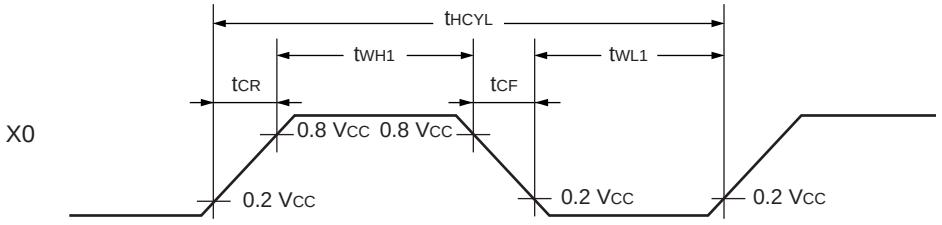
4. AC Characteristics

(1) Clock Timing

(Vcc = 3.3 V, Vss = 0.0 V, T_A = − 40 °C to + 85 °C)

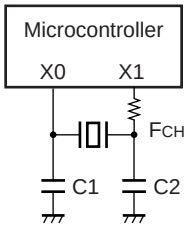
Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Clock frequency	F_{CH}	X0, X1	—	1.00	—	16.25	MHz	When using main oscillation circuit
				1.00	—	32.50	MHz	When using external clock
				3.00	—	10.00	MHz	Main PLL multiplied by 1
				3.00	—	8.13	MHz	Main PLL multiplied by 2
				3.00	—	6.50	MHz	Main PLL multiplied by 2.5
				3.00	—	4.06	MHz	Main PLL multiplied by 4
	F_{CL}	X0A, X1A		—	32.768	—	kHz	When using sub oscillation circuit
				—	32.768	—	kHz	When using sub PLL
Clock cycle time	t_{HCYL}	X0, X1		61.5	—	1000	ns	When using oscillation circuit
				30.8	—	1000	ns	When using external clock
	t_{LCYL}	X0A, X1A		—	30.5	—	µs	When using sub clock, When using external clock
Input clock pulse width	t_{WH1} t_{WL1}	X0		61.5	—	—	ns	When using external clock Duty ratio is about 30% to 70%.
	t_{WH2} t_{WL2}	X0A		—	15.2	—	µs	
Input clock rise time and fall time	t_{CR} t_{CF}	X0, X0A		—	—	5	ns	When using external clock

- Input wave form at external clock use (main clock)

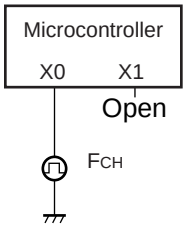


- Figure of Main Clock Input Port External Connection

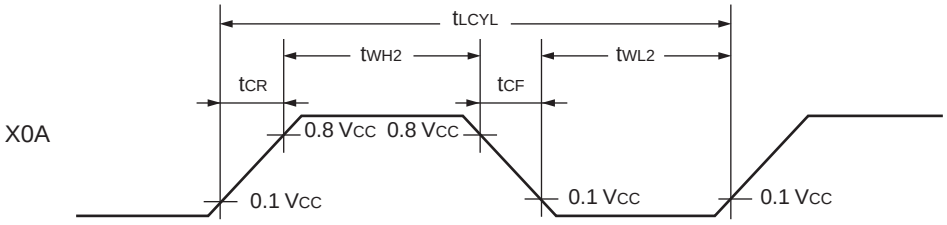
When using a crystal or ceramic oscillator



When using external clock

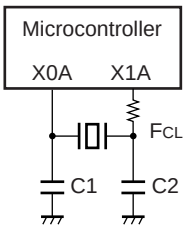


- Input wave form at external clock use (sub clock)

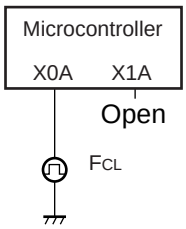


- Figure of Sub clock Input Port External Connection

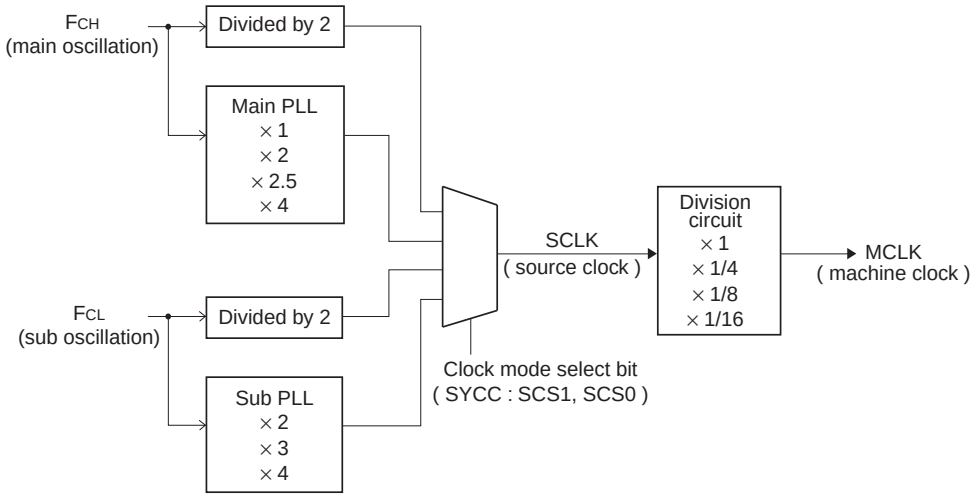
When using a crystal or ceramic oscillator



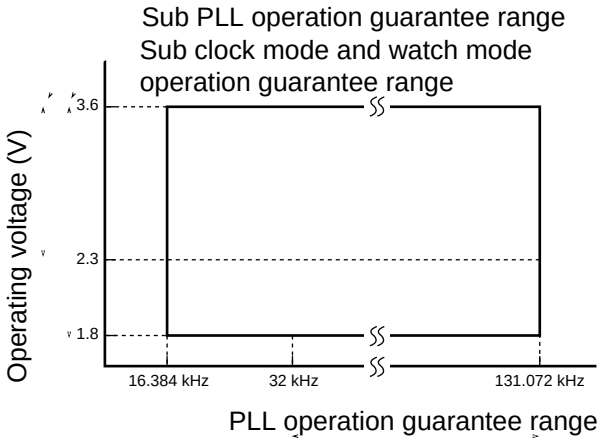
When using external clock

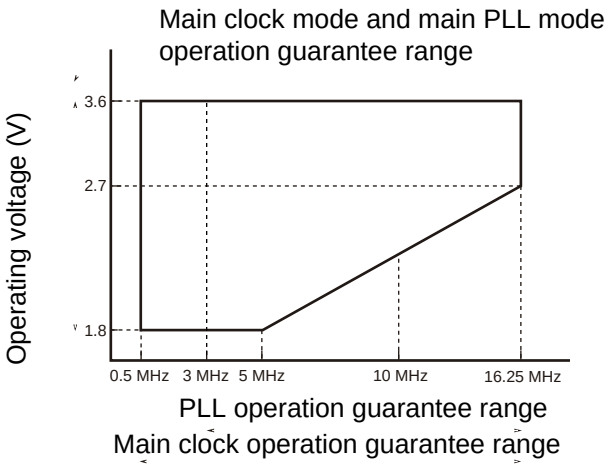


• Outline of clock generation block

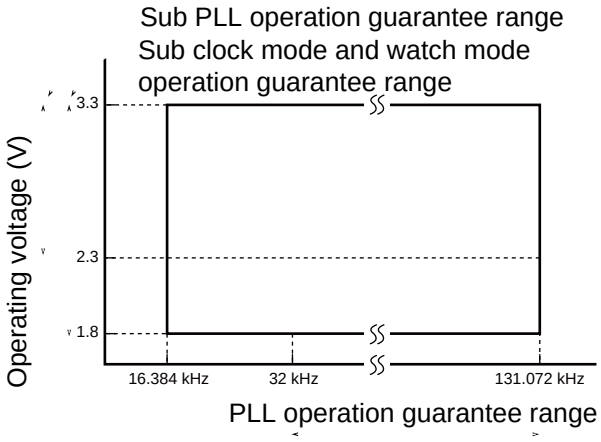


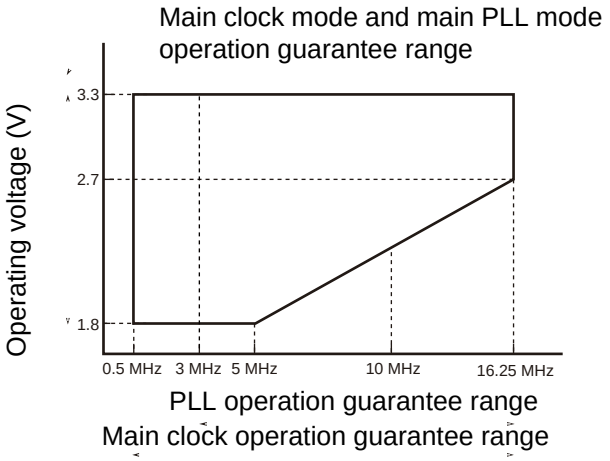
- Operating voltage - Operating frequency (When T_A = – 10 °C to + 85 °C)
  - MB95166D



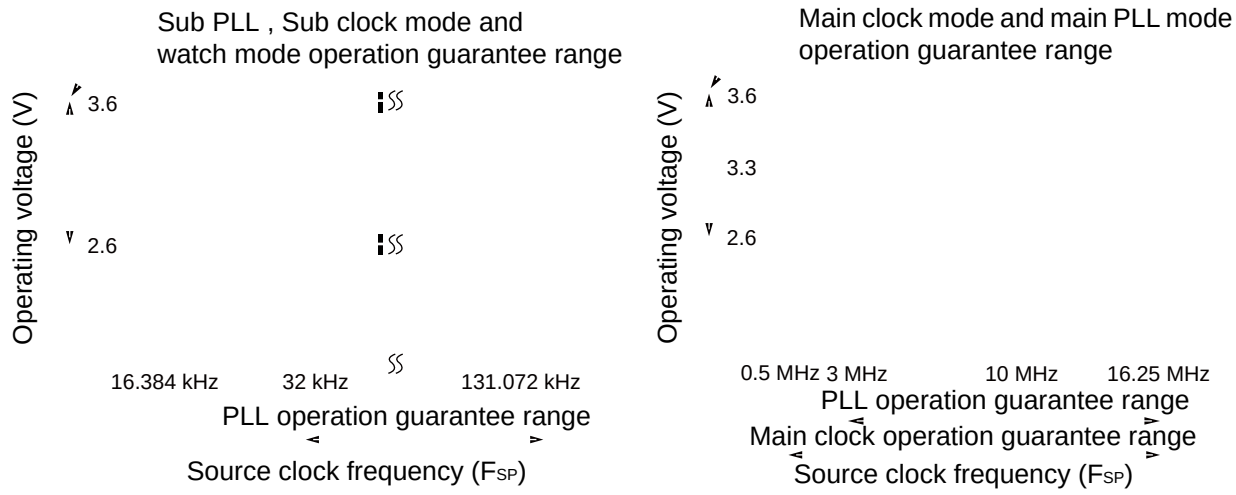


  - MB95F166D

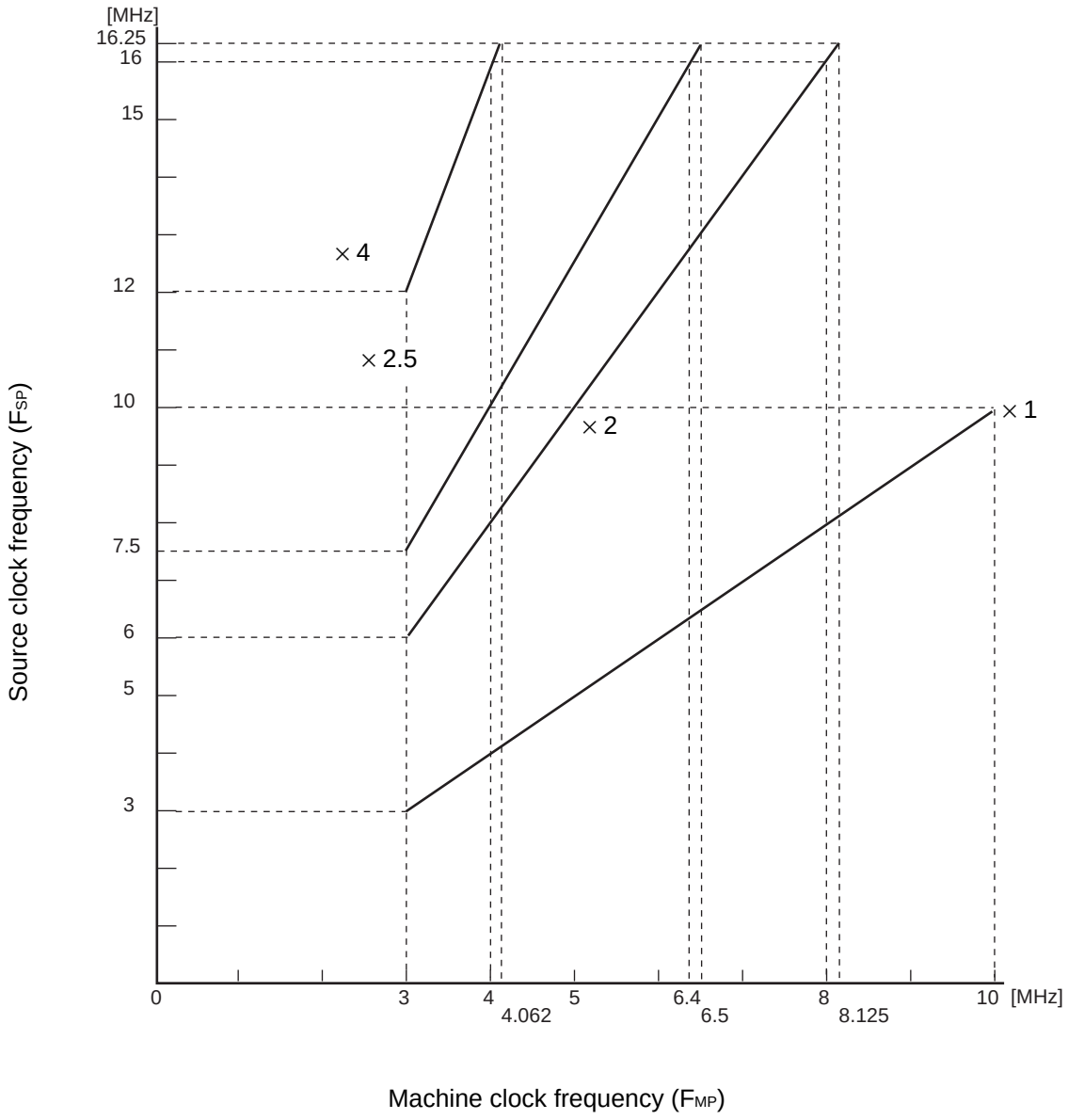




- Operating voltage - Operating frequency (When T_A = + 5 °C to + 35 °C)
  - MB95FV100D-101



• Main PLL operation frequency



(3) External Reset

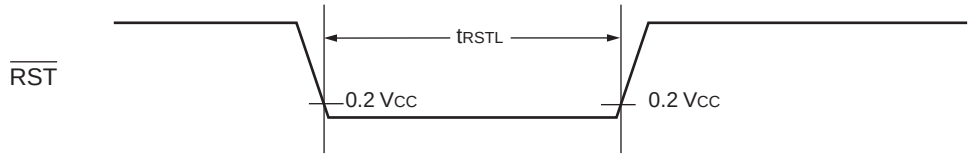
(Vcc = 3.3 V, Vss = 0.0 V, T_A = − 40 °C to + 85 °C)

Parameter	Symbol	Pin name	Condi-tions	Value		Unit	Remarks
				Min	Max		
$\overline{RST}$ L level pulse width	t_{RSTL}	$\overline{RST}$	—	2 t_{MCLK}*1	—	ns	At normal operating
				Oscillation time of oscillator*2 + 100	—	µs	At stop mode, sub clock mode, sub sleep mode, and watch mode

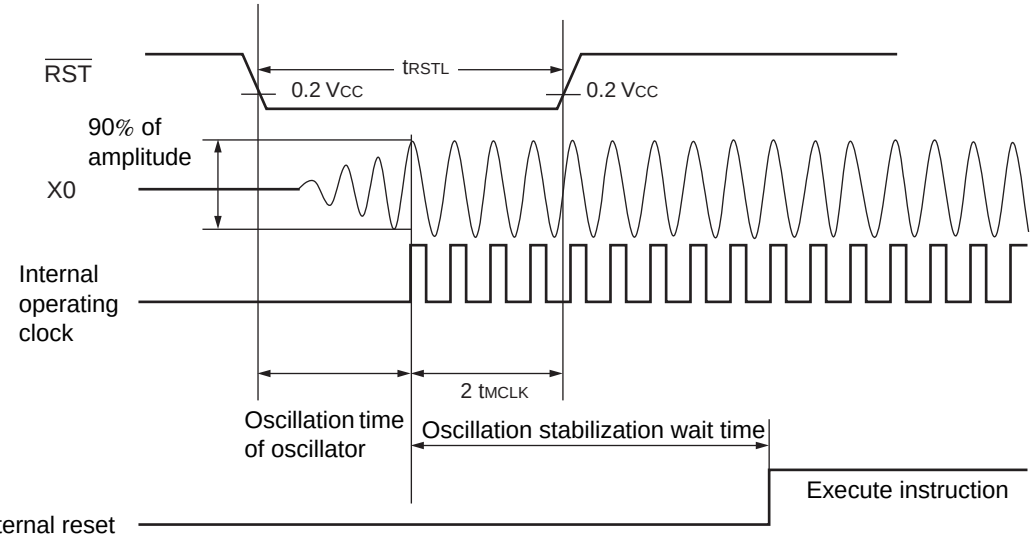
*1 : Refer to (2) Source Clock/Machine Clock for t_{MCLK}.

*2 : Oscillation time of oscillator is the time that the amplitude reaches 90 %. In the crystal oscillator, the oscillation time is between several ms and tens of ms. In ceramic oscillators, the oscillation time is between hundreds of µs and several ms. In the external clock, the oscillation time is 0 ms.

• At normal operating



• At stop mode, sub clock mode, sub sleep mode, watch mode, and power-on

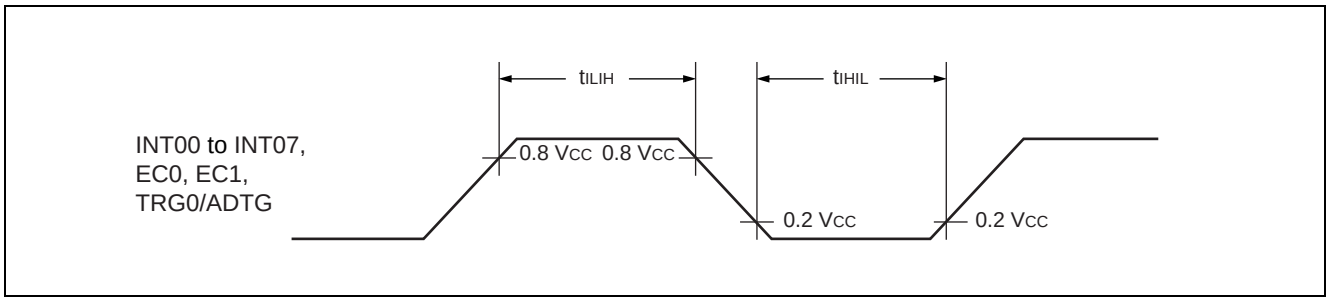


(5) Peripheral Input Timing

(Vcc = 3.3 V, Vss = 0.0 V, T_A = − 40 °C to + 85 °C)

Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
Peripheral input H pulse width	t_{ILIH}	INT00 to INT07, EC0, EC1, TRG0/ADTG	—	2 t_{MCLK}*	—	ns
Peripheral input L pulse width	t_{IHIL}			2 t_{MCLK}*	—	ns

* : Refer to (2) Source Clock/Machine Clock for t_{MCLK}.



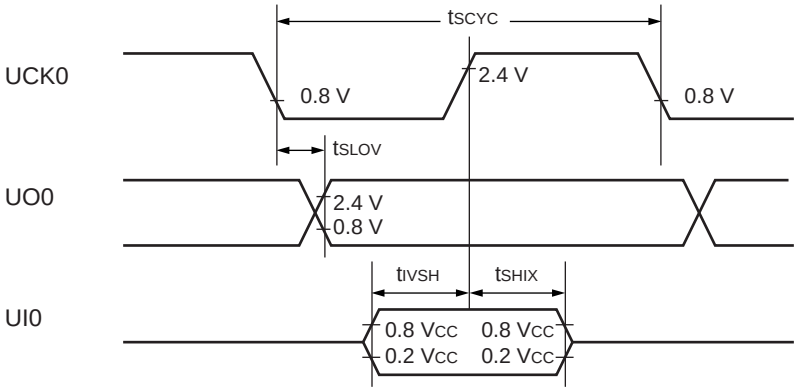
(6) UART/SIO, Serial I/O Timing

(Vcc = 3.3 V, Vss = 0.0 V, T_A = − 40 °C to + 85 °C)

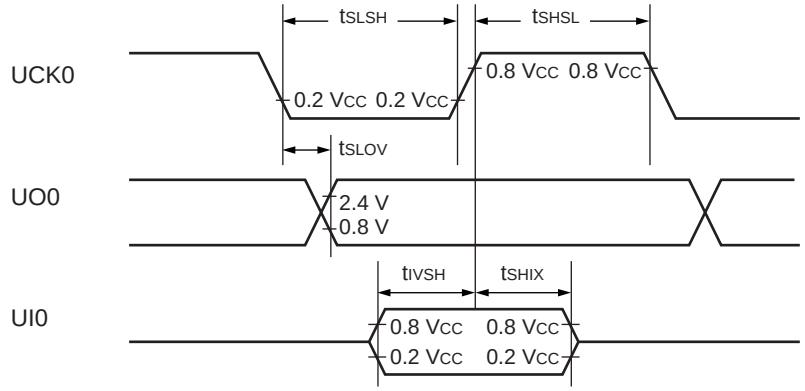
Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	UCK0	Internal clock operation output pin : C_L = 80 pF + 1TTL.	4 t_{MCLK}*	—	ns
UCK ↓ → UO time	t_{SLOV}	UCK0, UO0		− 190	+ 190	ns
Valid UI → UCK ↑	t_{IVSH}	UCK0, UI0		2 t_{MCLK}*	—	ns
UCK ↑ → valid UI hold time	t_{SHIX}	UCK0, UI0		2 t_{MCLK}*	—	ns
Serial clock H pulse width	t_{SHSL}	UCK0	External clock operation output pin : C_L = 80 pF + 1TTL.	4 t_{MCLK}*	—	ns
Serial clock L pulse width	t_{SLSH}	UCK0		4 t_{MCLK}*	—	ns
UCK ↓ → UO time	t_{SLOV}	UCK0, UO0		—	190	ns
Valid UI → UCK ↑	t_{IVSH}	UCK0, UI0		2 t_{MCLK}*	—	ns
UCK ↑ → valid UI hold time	t_{SHIX}	UCK0, UI0		2 t_{MCLK}*	—	ns

* : Refer to (2) Source Clock/Machine Clock for t_{MCLK}.

Internal shift clock mode



External shift clock mode



(7) LIN-UART Timing

Sampling at the rising edge of sampling clock*1 and prohibited serial clock delay*2
(ESCR register : SCES bit = 0, ECCR register : SCDE bit = 0)

(Vcc = 3.3 V, Vss = 0.0 V, T_A = –40 °C to + 85 °C)

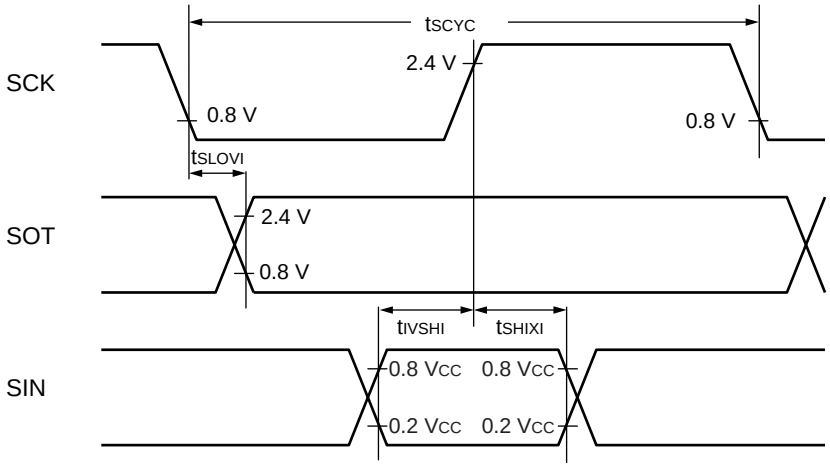
Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCK	Internal clock operation output pin : C_L = 80 pF + 1 TTL.	5 t_{MCLK}*3	—	ns
SCK ↓ → SOT delay time	t_{SLOVI}	SCK, SOT		–95	+ 95	ns
Valid SIN → SCK ↑	t_{IVSHI}	SCK, SIN		t_{MCLK}*3 + 190	—	ns
SCK ↑ → valid SIN hold time	t_{SHIXI}	SCK, SIN		0	—	ns
Serial clock L pulse width	t_{SLSH}	SCK	External clock operation output pin : C_L = 80 pF + 1 TTL.	3 t_{MCLK}*3 – t_R	—	ns
Serial clock H pulse width	t_{SHSL}	SCK		t_{MCLK}*3 + 95	—	ns
SCK ↓ → SOT delay time	t_{SLOVE}	SCK, SOT		—	2 t_{MCLK}*3 + 95	ns
Valid SIN → SCK ↑	t_{IVSHE}	SCK, SIN		190	—	ns
SCK ↑ → valid SIN hold time	t_{SHIXE}	SCK, SIN		t_{MCLK}*3 + 95	—	ns
SCK fall time	t_F	SCK		—	10	ns
SCK rise time	t_R	SCK		—	10	ns

*1 : Provide switch function whether sampling of reception data is performed at rising edge or falling edge of the serial clock.

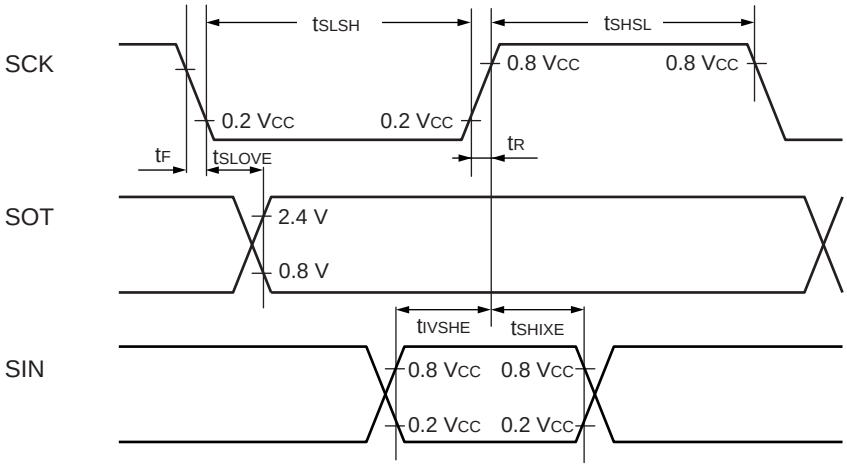
*2 : Serial clock delay function is used to delay half clock for the output signal of serial clock.

*3 : Refer to (2) Source Clock/Machine Clock for t_{MCLK}.

Internal shift clock mode



External shift clock mode



Sampling at the falling edge of sampling clock*1 and prohibited serial clock delay*2
(ESCR register : SCES bit = 1, ECCR register : SCDE bit = 0)

(V_{CC} = 3.3 V, V_{SS} = 0.0 V, T_A = –40 °C to + 85 °C)

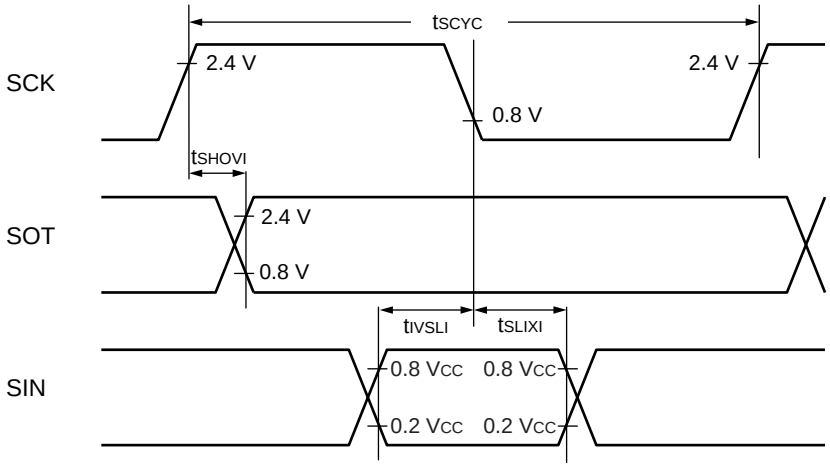
Parameter	Sym-bol	Pin name	Conditions	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCK	Internal clock operation output pin : C_L = 80 pF + 1 TTL.	5 t_{MCLK}*3	—	ns
SCK ↑ → SOT delay time	t_{SHOVI}	SCK, SOT		–95	+ 95	ns
Valid SIN → SCK ↓	t_{IVSLI}	SCK, SIN		t_{MCLK}*3 + 190	—	ns
SCK ↓ → valid SIN hold time	t_{SLIXI}	SCK, SIN		0	—	ns
Serial clock H pulse width	t_{SHSL}	SCK	External clock operation output pin : C_L = 80 pF + 1 TTL.	3 t_{MCLK}*3 – t_R	—	ns
Serial clock L pulse width	t_{SLSH}	SCK		t_{MCLK}*3 + 95	—	ns
SCK ↑ → SOT delay time	t_{SHOVE}	SCK, SOT		—	2 t_{MCLK}*3 + 95	ns
Valid SIN → SCK ↓	t_{IVSLE}	SCK, SIN		190	—	ns
SCK ↓ → valid SIN hold time	t_{SLIXE}	SCK, SIN		t_{MCLK}*3 + 95	—	ns
SCK fall time	t_F	SCK		—	10	ns
SCK rise time	t_R	SCK		—	10	ns

*1 : Provide switch function whether sampling of reception data is performed at rising edge or falling edge of the serial clock.

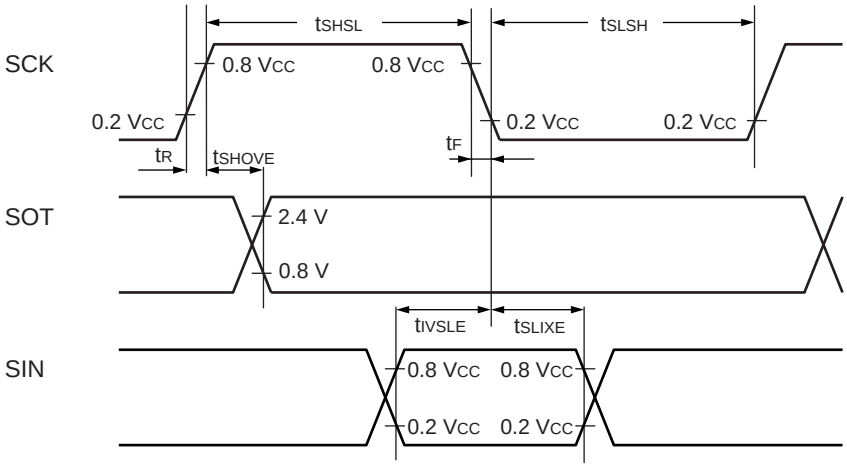
*2 : Serial clock delay function is used to delay half clock for the output signal of serial clock.

*3 : Refer to (2) Source Clock/Machine Clock for t_{MCLK}.

Internal shift clock mode



External shift clock mode



Sampling at the rising edge of sampling clock*1 and enabled serial clock delay*2
(ESCR register : SCES bit = 0, ECCR register : SCDE bit = 1)

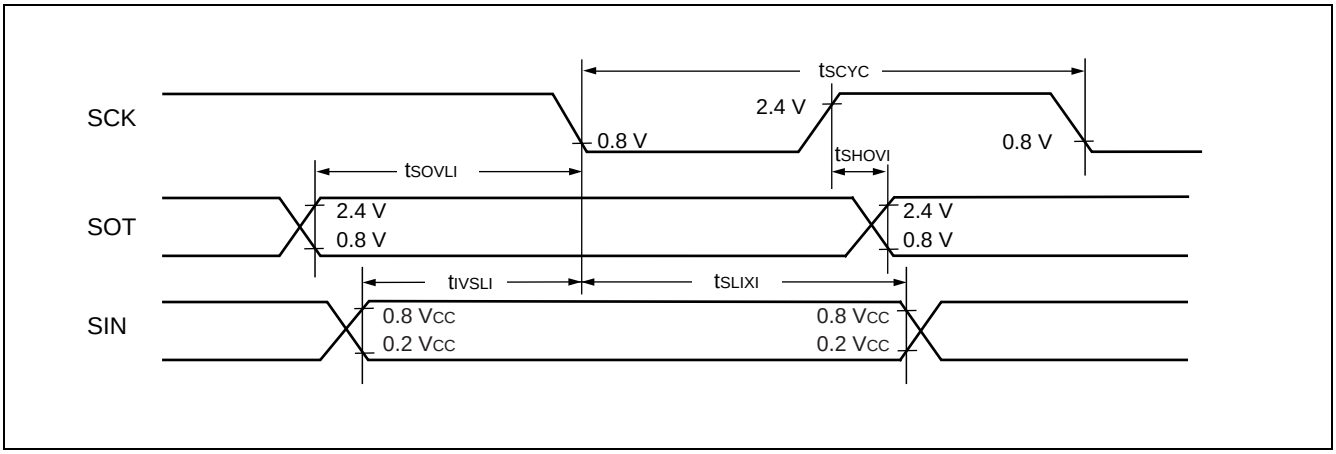
(V_{CC} = 3.3 V, V_{SS} = 0.0 V, T_A = –40 °C to + 85 °C)

Parameter	Sym-bol	Pin name	Conditions	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCK	Internal clock operation output pin : C_L = 80 pF + 1 TTL.	5 t_{MCLK}*3	—	ns
SCK ↑ → SOT delay time	t_{SHOVI}	SCK, SOT		–95	+ 95	ns
Valid SIN → SCK ↓	t_{IVSLI}	SCK, SIN		t_{MCLK}*3 + 190	—	ns
SCK ↓ → valid SIN hold time	t_{SLIXI}	SCK, SIN		0	—	ns
SOT → SCK ↓ delay time	t_{SOVLI}	SCK, SOT		—	4 t_{MCLK}*3	ns

*1 : Provide switch function whether sampling of reception data is performed at rising edge or falling edge of the serial clock.

*2 : Serial clock delay function is used to delay half clock for the output signal of serial clock.

*3 : Refer to (2) Source Clock/Machine Clock for t_{MCLK}.



Sampling at the falling edge of sampling clock*1 and enabled serial clock delay*2
(ESCR register : SCES bit = 1, ECCR register : SCDE bit = 1)

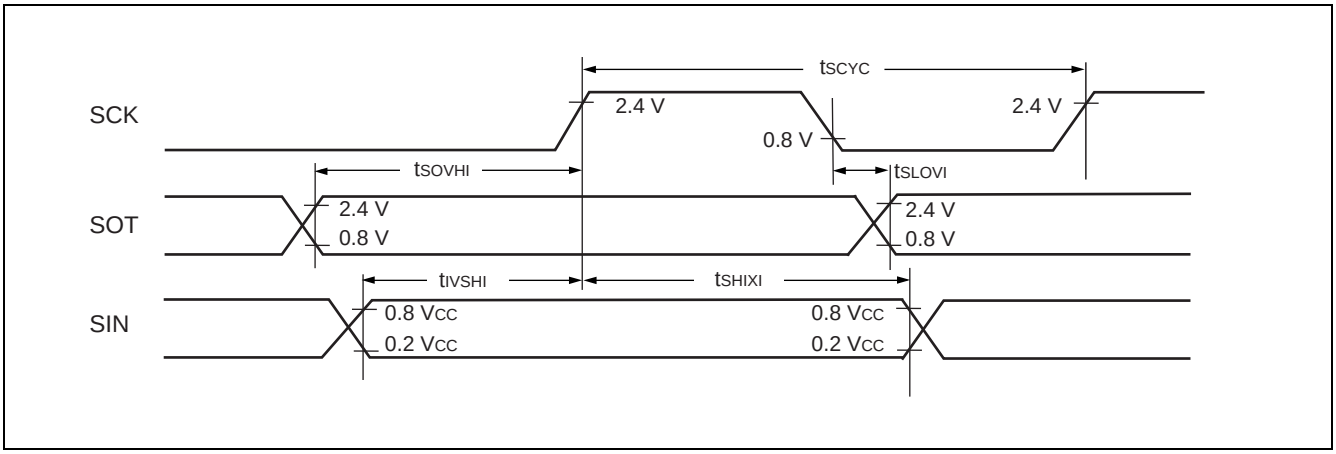
(V_{CC} = 3.3 V, V_{SS} = 0.0 V, T_A = –40 °C to + 85 °C)

Parameter	Sym-bol	Pin name	Conditions	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCK	Internal clock operation output pin : C_L = 80 pF + 1 TTL.	5 t_{MCLK}*3	—	ns
SCK ↓ → SOT delay time	t_{SLOVI}	SCK, SOT		–95	+ 95	ns
Valid SIN → SCK ↑	t_{IVSHI}	SCK, SIN		t_{MCLK}*3 + 190	—	ns
SCK ↑ → valid SIN hold time	t_{SHIXI}	SCK, SIN		0	—	ns
SOT → SCK ↑ delay time	t_{SOVHI}	SCK, SOT		—	4 t_{MCLK}*3	ns

*1 : Provide switch function whether sampling of reception data is performed at rising edge or falling edge of the serial clock.

*2 : Serial clock delay function is used to delay half clock for the output signal of serial clock.

*3 : Refer to (2) Source Clock/Machine Clock for t_{MCLK}.



(8) I²C Timing

(V_{CC} = 3.3 V ± 10%, AV_{SS} = V_{SS} = 0.0 V, T_A = − 40 °C to + 85 °C)

Parameter	Symbol	Pin name	Conditions	Value				Unit
				Standard-mode		Fast-mode		
				Min	Max	Min	Max	
SCL clock frequency	f_{SCL}	SCL0	R = 1.7 kΩ, C = 50 pF*1	0	100	0	400	kHz
(Repeat) Start condition hold time SDA ↓ → SCL ↓	$t_{HD;STA}$	SCL0 SDA0		4.0	—	0.6	—	µs
SCL clock L width	t_{LOW}	SCL0		4.7	—	1.3	—	µs
SCL clock H width	t_{HIGH}	SCL0		4.0	—	0.6	—	µs
(Repeat) Start condition setup time SCL ↑ → SDA ↓	$t_{SU;STA}$	SCL0 SDA0		4.7	—	0.6	—	µs
Data hold time SCL ↓ → SDA ↓ ↑	$t_{HD;DAT}$	SCL0 SDA0		0	3.45*2	0	0.9*3	µs
Data setup time SDA ↓ ↑ → SCL ↑	$t_{SU;DAT}$	SCL0 SDA0		0.25*4	—	0.1*4	—	µs
Stop condition setup time SCL ↑ → SDA ↑	$t_{SU;STO}$	SCL0 SDA0		4.0	—	0.6	—	µs
Bus free time between stop condition and start condition	t_{BUF}	SCL0 SDA0		4.7	—	1.3	—	µs

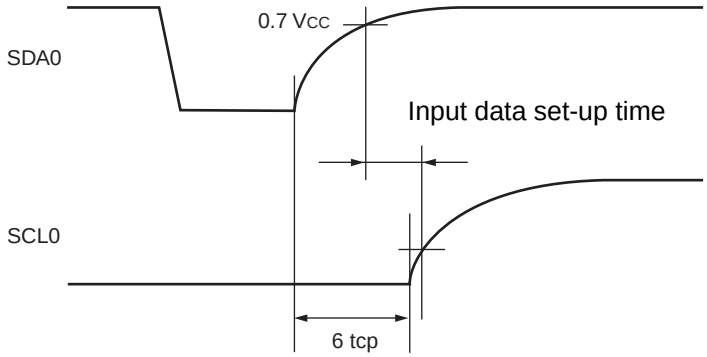
*1 : R, C : Pull-up resistor and load capacitor of the SCL and SDA lines.

*2 : The maximum $t_{HD;DAT}$ have only to be met if the device dose not stretch the L width (t_{LOW}) of the SCL signal.

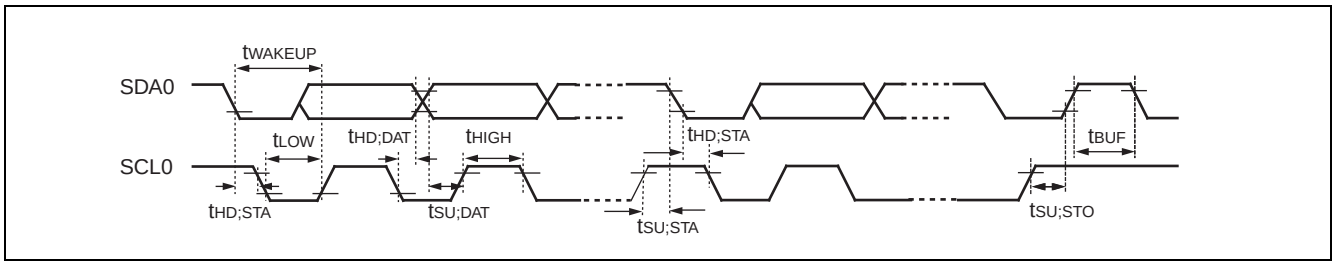
*3 : A fast-mode I²C-bus device can be used in a standard-mode I²C-bus system, but the requirement $t_{SU;DAT} \geq$ 250 ns must then be met.

*4 : Refer to • Note of SDA and SCL set-up time .

• Note of SDA and SCL set-up time



Note : The rating of the input data set-up time in the device connected to the bus cannot be satisfied depending on the load capacitance or pull-up resistor.
Be sure to adjust the pull-up resistor of SDA and SCL if the rating of the input data set-up time cannot be satisfied.


tWAKEUP
SDA0
SCL0
tLOW
tHD;DAT
tHIGH
tHD;STA
tBUF
tHD;STA
tSU;DAT
tSU;STA
tSU;STO

(V_{CC} = 3.3 V ± 10%, AV_{SS} = V_{SS} = 0.0 V, T_A = − 40 °C to + 85 °C)

Parameter	Symbol	Pin name	Conditions	Value*2		Unit	Remarks
				Min	Max		
SCL clock L width	t_{LOW}	SCL0	R = 1.7 kΩ, C = 50 pF*1	(2 + nm / 2) t_{MCLK} – 20	—	ns	Master mode
SCL clock H width	t_{HIGH}	SCL0		(nm / 2) t_{MCLK} – 20	(nm / 2) t_{MCLK} + 20	ns	Master mode
Start condition hold time	$t_{HD;STA}$	SCL0 SDA0		(–1 + nm / 2) t_{MCLK} – 20	(–1 + nm) t_{MCLK} + 20	ns	Master mode Maximum value is applied when m, n = 1, 8. Otherwise, the minimum value is applied.
Stop condition setup time	$t_{SU;STO}$	SCL0 SDA0		(1 + nm / 2) t_{MCLK} – 20	(1 + nm / 2) t_{MCLK} + 20	ns	Master mode
Start condition setup time	$t_{SU;STA}$	SCL0 SDA0		(1 + nm / 2) t_{MCLK} – 20	(1 + nm / 2) t_{MCLK} + 20	ns	Master mode
Bus free time between stop condition and start condition	t_{BUF}	SCL0 SDA0		(2 nm + 4) t_{MCLK} – 20	—	ns	
Data hold time	$t_{HD;DAT}$	SCL0 SDA0		3 t_{MCLK} – 20	—	ns	Master mode
Data setup time	$t_{SU;DAT}$	SCL0 SDA0		(–2 + nm / 2) t_{MCLK} – 20	(–1 + nm / 2) t_{MCLK} + 20	ns	Master mode When assuming that L of SCL is not extended, the minimum value is applied to first bit of continuous data. Otherwise, the maximum value is applied.
Setup time between clearing interrupt and SCL rising	$t_{SU;INT}$	SCL0		(nm / 2) t_{MCLK} – 20	(1 + nm / 2) t_{MCLK} + 20	ns	Minimum value is applied to interrupt at 9th SCL↓. Maximum value is applied to interrupt at 8th SCL↓.
SCL clock L width	t_{LOW}	SCL0		4 t_{MCLK} – 20	—	ns	At reception
SCL clock H width	t_{HIGH}	SCL0		4 t_{MCLK} – 20	—	ns	At reception
Start condition detection	$t_{HD;STA}$	SCL0 SDA0		2 t_{MCLK} – 20	—	ns	Undetected when 1 t_{MCLK} is used at reception

(Continued)

(Continued)

(V_{CC} = 3.3 V ± 10%, AV_{SS} = V_{SS} = 0.0 V, T_A = − 40 °C to + 85 °C)

Parameter	Symbol	Pin name	Conditions	Value*2		Unit	Remarks
				Min	Max		
Stop condition detection	$t_{SU;STO}$	SCL0 SDA0	R = 1.7 kΩ, C = 50 pF*1	2 t_{MCLK} – 20	—	ns	Undetected when 1 t_{MCLK} is used at reception
Restart condition detection condition	$t_{SU;STA}$	SCL0 SDA0		2 t_{MCLK} – 20	—	ns	Undetected when 1 t_{MCLK} is used at reception
Bus free time	t_{BUF}	SCL0 SDA0		2 t_{MCLK} – 20	—	ns	At reception
Data hold time	$t_{HD;DAT}$	SCL0 SDA0		2 t_{MCLK} – 20	—	ns	At slave transmission mode
Data setup time	$t_{SU;DAT}$	SCL0 SDA0		t_{LOW} – 3 t_{MCLK} – 20	—	ns	At slave transmission mode
Data hold time	$t_{HD;DAT}$	SCL0 SDA0		0	—	ns	At reception
Data setup time	$t_{SU;DAT}$	SCL0 SDA0		t_{MCLK} – 20	—	ns	At reception
SDA ↓ → SCL ↑ (at wakeup function)	t_{WAKEUP}	SCL0 SDA0		Oscillation stabilization wait time + 2 t_{MCLK} – 20	—	ns	

*1 : R, C : Pull-up resistor and load capacitor of the SCL and SDA lines.

*2 :
- Refer to (2) Source Clock/Machine Clock for t_{MCLK}.
- m is CS4 bit and CS3 bit (bit 4 and bit 3) of I²C clock control register (ICCR) .
- n is CS2 bit to CS0 bit (bit 2 to bit 0) of I²C clock control register (ICCR) .
- Actual timing of I²C is determined by m and n values set by the machine clock (t_{MCLK}) and CS4 to CS0 of ICCR0 register.
- Standard-mode :
  m and n can be set at the range : 0.9 MHz < t_{MCLK} (machine clock) < 10 MHz.
  Setting of m and n determines the machine clock that can be used below.
  (m, n) = (1, 8) : 0.9 MHz < t_{MCLK} ≤ 1 MHz
  (m, n) = (1, 22) , (5, 4) , (6, 4) , (7, 4) , (8, 4) : 0.9 MHz < t_{MCLK} ≤ 2 MHz
  (m, n) = (1, 38) , (5, 8) , (6, 8) , (7, 8) , (8, 8) : 0.9 MHz < t_{MCLK} ≤ 4 MHz
  (m, n) = (1, 98) : 0.9 MHz < t_{MCLK} ≤ 10 MHz
- Fast-mode :
  m and n can be set at the range : 3.3 MHz < t_{MCLK} (machine clock) < 10 MHz.
  Setting of m and n determines the machine clock that can be used below.
  (m, n) = (1, 8) : 3.3 MHz < t_{MCLK} ≤ 4 MHz
  (m, n) = (1, 22) , (5, 4) : 3.3 MHz < t_{MCLK} ≤ 8 MHz
  (m, n) = (6, 4) : 3.3 MHz < t_{MCLK} ≤ 10 MHz

5. A/D Converter

(1) A/D Converter Electrical Characteristics

(AV_{CC} = V_{CC} = 1.8 V to 3.3 V, AV_{SS} = V_{SS} = 0.0 V, T_A = − 40 °C to + 85 °C)

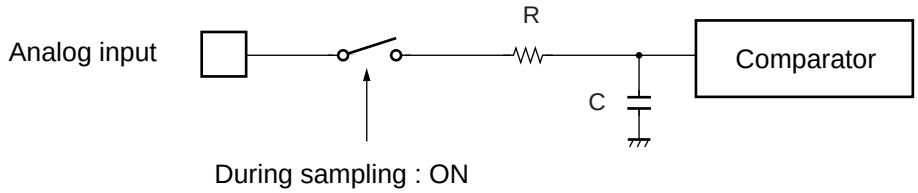
Parameter	Symbol	Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	—	—	—	—	10	bit	
Total error			− 3.0	—	+ 3.0	LSB	
Linearity error			− 2.5	—	+ 2.5	LSB	
Differential linear error			− 1.9	—	+ 1.9	LSB	
Zero transition voltage	V_{OT}		AV_{SS} − 1.5 LSB	AV_{SS} + 0.5 LSB	AV_{SS} + 2.5 LSB	V	2.7 V ≤ AV_{CC} ≤ 3.3 V
			AV_{SS} − 0.5 LSB	AV_{SS} + 1.5 LSB	AV_{SS} + 3.5 LSB	V	1.8 V ≤ AV_{CC} < 2.7 V
Full-scale transition voltage	V_{FST}		AVR − 3.5 LSB	AVR − 1.5 LSB	AVR + 0.5 LSB	V	2.7 V ≤ AV_{CC} ≤ 3.3 V
			AVR − 2.5 LSB	AVR − 0.5 LSB	AVR + 1.5 LSB	V	1.8 V ≤ AV_{CC} < 2.7 V
Compare time	—		0.6	—	140	µs	2.7 V ≤ AVcc ≤ 3.3 V
			20	—	140	µs	1.8 V ≤ AVcc < 2.7 V
Sampling time	—	—	0.4	—	∞	µs	2.7 V ≤ AVcc ≤ 3.3 V, At external impedance < 1.8 kΩ
			30	—	∞	µs	1.8 V ≤ AVcc < 2.7 V, At external impedance < 14.8 kΩ
Analog input current	I_{AIN}		−0.3	—	+0.3	µA	
Analog input voltage	V_{AIN}		AV_{SS}	—	AVR	V	
Reference voltage	—		AV_{SS} + 1.8	—	AV_{CC}	V	AVR pin
Reference voltage supply current	I_R		—	400	600	µA	AVR pin, During A/D operation
	I_{RH}		—	—	5	µA	AVR pin, At stop mode

(2) Notes on Using A/D Converter

- **About the external impedance of analog input and its sampling time**

A/D converter with sample and hold circuit. If the external impedance is too high to keep sufficient sampling time, the analog voltage charged to the internal sample and hold capacitor is insufficient, adversely affecting A/D conversion precision. Therefore, to satisfy the A/D conversion precision standard, consider the relationship between the external impedance and minimum sampling time and either adjust the register value and operating frequency or decrease the external impedance so that the sampling time is longer than the minimum value. Also, if the sampling time cannot be sufficient, connect a capacitor of about 0.1 µF to the analog input pin.

- Analog input equivalent circuit

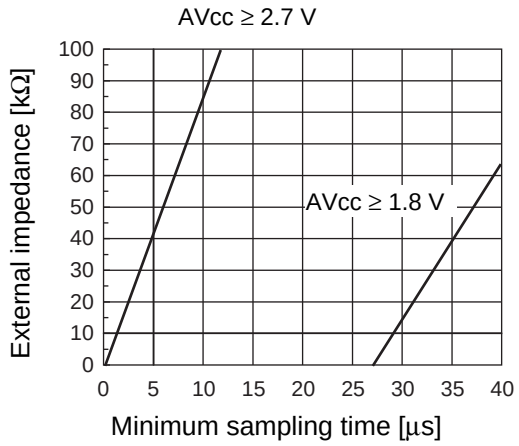


	R	C
2.7 V ≤ V_{CC} ≤ 3.6 V	1.7 kΩ (Max)	14.5 pF (Max)
1.8 V ≤ V_{CC} < 2.7 V	84 kΩ (Max)	25.2 pF (Max)

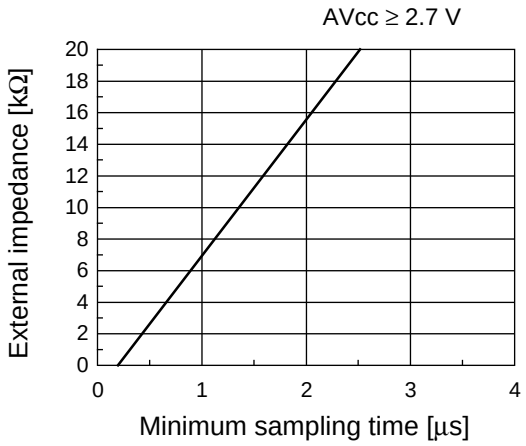
Note : The values are reference values.

- The relationship between external impedance and minimum sampling time

(External impedance = 0 kΩ to 100 kΩ)



(External impedance = 0 kΩ to 20 kΩ)



- **About errors**

As |V_{CC} – V_{SS}| becomes smaller, values of relative errors grow larger.

(3) Definition of A/D Converter Terms

Resolution

The analog quantity to be monitored by the A/D converter.

When the number of bits is 10, analog voltage can be divided into $2^{10} = 1024$.

Linearity error (unit : LSB)

The deviation between the value along a straight line connecting the zero transition point (00 0000 0000 ⟷ 00 0000 0001) of a device and the full-scale transition point (11 1111 1111 ⟷ 11 1111 1110) compared with the actual conversion values obtained.

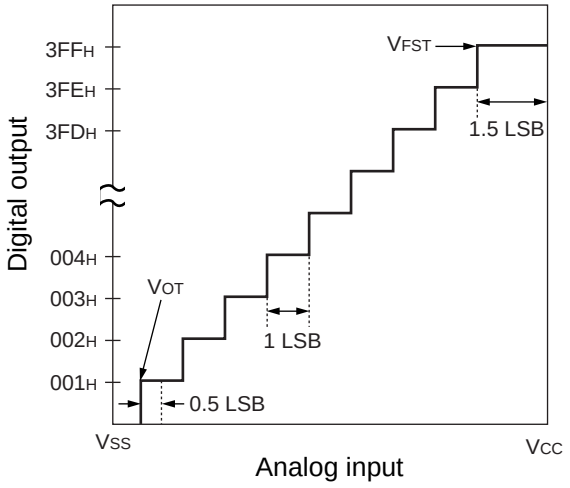
Differential linear error (Unit : LSB)

Deviation of input voltage, which is required for changing output code by 1 LSB, from an ideal value.

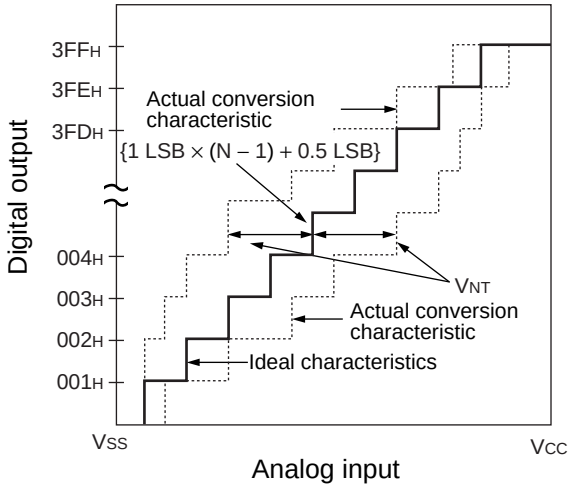
Total error (unit: LSB)

Difference between actual and theoretical values, caused by a zero transition error, full-scale transition error, linearity error, quantum error, and noise.

Ideal I/O characteristics



Total error



$$1\ \text{LSB} = \frac{V_{CC} - V_{SS}}{1024}\ \text{(V)}$$

$$\text{Total error of digital output N} = \frac{V_{NT} - \{1\ \text{LSB} \times (N - 1) + 0.5\ \text{LSB}\}}{1\ \text{LSB}}\ \text{[LSB]}$$

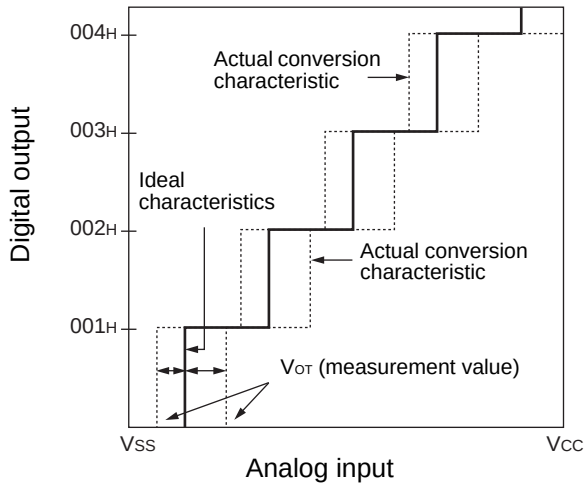
N : A/D converter digital output value

V_{NT} : A voltage at which digital output transits from $(N - 1)_H$ to N_H

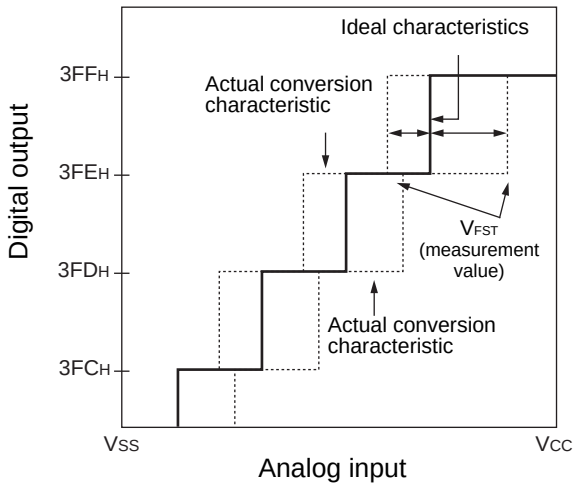
(Continued)

(Continued)

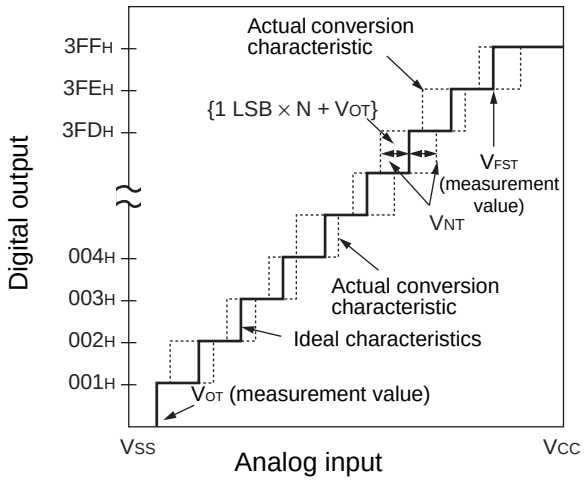
Zero transition error



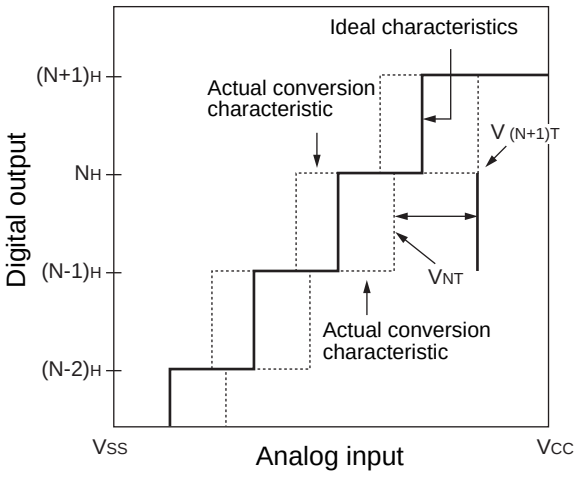
Full-scale transition error



Linearity error



Differential linear error



$$\text{Linearity error in digital output N} = \frac{V_{NT} - \{1\ \text{LSB} \times N + V_{OT}\}}{1\ \text{LSB}}$$

$$\text{Differential linear error in digital output N} = \frac{V_{(N+1)T} - V_{NT}}{1\ \text{LSB}} - 1$$

N : A/D converter digital output value
V_{NT} : A voltage at which digital output transits from $(N - 1)_H$ to N_H
V_{OT} (Ideal value) = V_{SS} + 0.5 LSB [V]
V_{FST} (Ideal value) = V_{CC} – 1.5 LSB [V]

6. Flash Memory Program/Erase Characteristics

Parameter	Value			Unit	Remarks
	Min	Typ	Max		
Chip erase time	—	1*1	15*2	s	Excludes 00_H programming prior erasure.
Byte programming time	—	32	3600*2	µs	Excludes system-level overhead.
Erase/program cycle	10000	—	—	cycle	
Power supply voltage at erase/ program	2.7	—	3.3	V	
Flash memory data retention time	20*3	—	—	year	Average T_A = +85 °C

*1 : T_A = + 25 °C, V_{CC} = 3.0 V, 10000 cycles

*2 : T_A = + 85 °C, V_{CC} = 2.7 V, 10000 cycles

*3 : This value comes from the technology qualification (using Arrhenius equation to translate high temperature measurements into normalized value at +85 °C) .

MASK OPTION

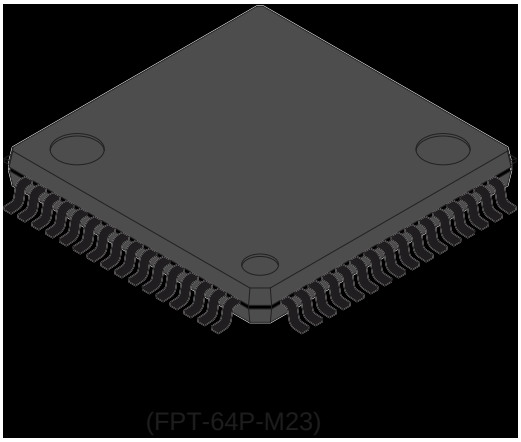
No.	Part number	MB95F166D	MB95FV100D-101	MB95166D
	Specifying procedure	Setting disabled	Setting disabled	Specifying when ordering MASK
1	Clock mode select • Single-system clock mode • Dual-system clock mode	Dual-system clock mode	Changing by the switch on MCU board	Dual-system clock mode
2	Low voltage detection reset* • With low voltage detection reset • Without low voltage detection reset	No	No	No
3	Clock supervisor* • With clock supervisor • Without clock supervisor	No	No	No
4	Selection of oscillation stabilization wait time • Selectable the initial value of main clock oscillation stabilization wait time	Fixed to oscillation stabilization wait time of $(2^{14} - 2) / F_{CH}$	Fixed to oscillation stabilization wait time of $(2^{14} - 2) / F_{CH}$	Selectable: 1 : $(2^{2} - 2) / F_{CH}$ 2 : $(2^{12} - 2) / F_{CH}$ 3 : $(2^{13} - 2) / F_{CH}$ 4 : $(2^{14} - 2) / F_{CH}$

* : Low voltage detection reset and clock supervisor are options of 5-V products.

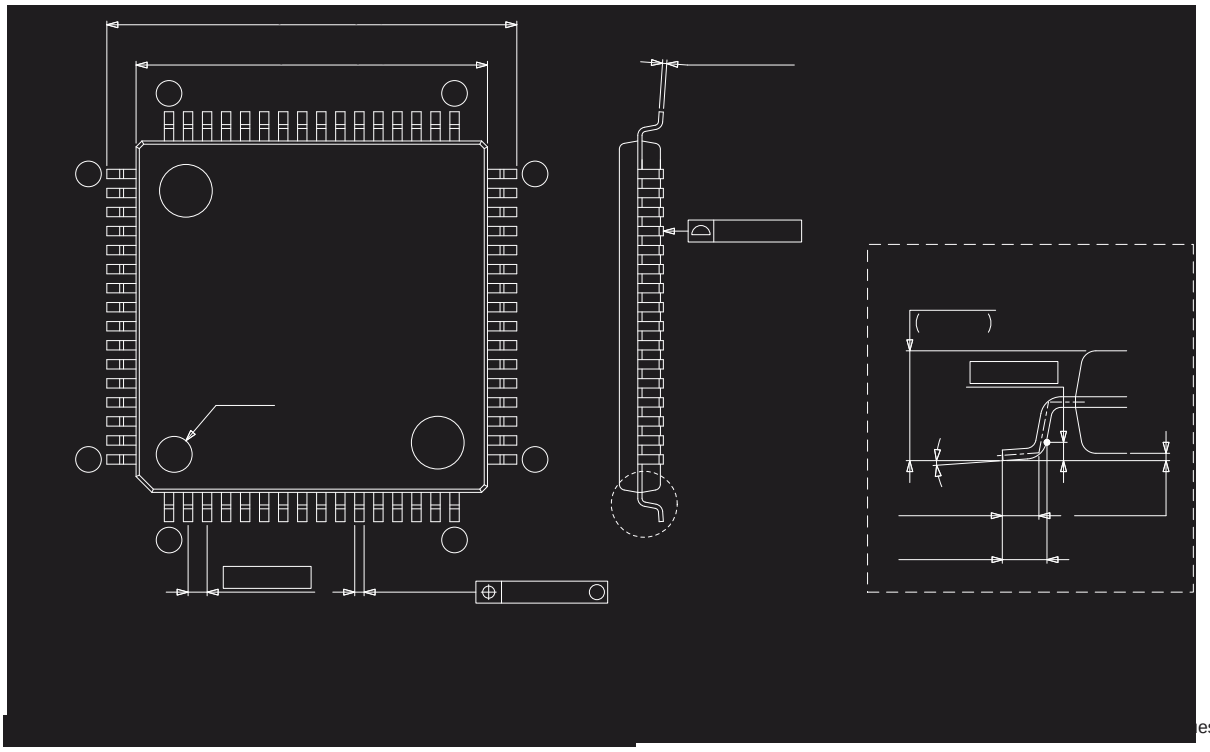
ORDERING INFORMATION

Part number	Package
MB95F166DPMC/MB95166DPMC	64-pin plastic LQFP (FPT-64P-M23)
MB95F166DPMC1/MB95166DPMC1	64-pin plastic LQFP (FPT-64P-M24)
MB2146-301A (MB95FV100D-101PBT)	MCU board (224-ball plastic PFBGA (BGA-224P-M08))

PACKAGE DIMENSIONS



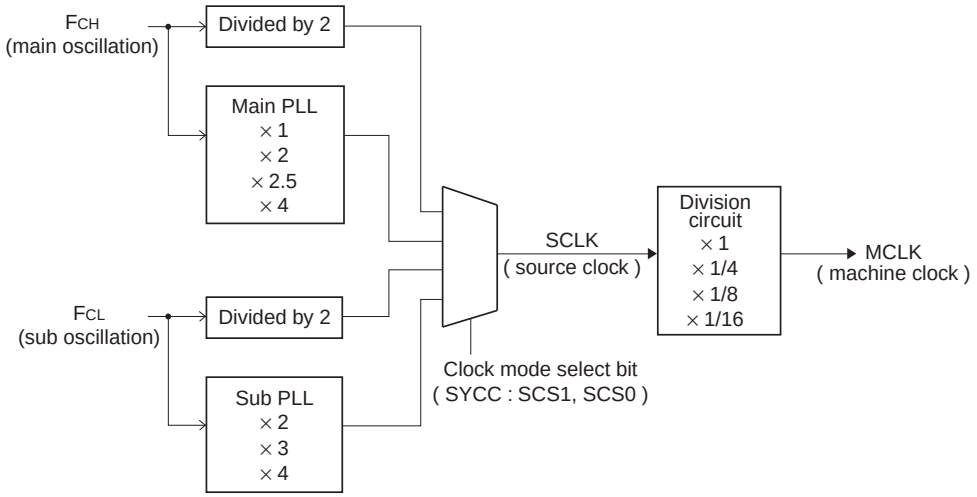
Note 1) * : These dimensions do not include resin protrusion.
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.



Please confirm the latest Package dimension by following URL.
http://edevice.fujitsu.com/package/en-search/

(Continued)

• Outline of clock generation block



MAIN CHANGES IN THIS EDITION

Page	Section	Change Results
—	—	Added the part number; (MB95166D)
2	FEATURE	Changed as follows. (• Flash memory security function → • Flash memory security function (Flash memory device only))
3, 4	PRODUCT LINEUP	Added the row of MB95166D.
3		Changed the Reset output. (Yes → No)
5	OSCILLATION STABILIZATION WAIT TIME	Changed the OSCILLATION STABILIZATION WAIT TIME
	PACKAGES AND CORRESPONDING PRODUCTS	Added the row of MB95166D.
6	DIFFERENCES AMONG PRODUCTS AND NOTES ON SELECTING PRODUCTS	Changed the Notes on Using Evaluation Products Changed the Difference of Memory Spaces Changed the Operating voltage Added the Difference MOD pins
11	I/O CIRCUIT TYPE	Changed the Type B
13		Changed the Type S (• LCD power supply was deleted)
14	HANDLING DEVICES	Added the item of • Serial Communication .
17	CPU CORE	Added the MB95166D in • Memory Map .
23	I/O MAP	Changed the Address 0073_H, 0074_H.
28	ELECTRICAL CHARACTERISTICS 1. Absolute Maximum Ratings	Changed the Remarks of Power supply voltage for LCD (Products with LCD internal division resistance*3 → *3)
31	3. DC Characteristics	Changed the row of Symbol V_{IHM} and V_{ILM}.
32		Added the row of Pull-down resistor (R_{MOD}).
32, 33		Changed the Power supply current.
38, 39	4. AC Characteristics (2) Source Clock/Machine Clock	Changed the Operating voltage - Operating frequency (When T_A = –10 °C to +85 °C) (• Added the graph of MB95166D)
61	MASK OPTION	Added the row of MB95166D.
62	ORDERING INFORMATION	Changed the part numbers. (MB95F166DPMC → MB95F166DPMC/MB95166DPMC) (MB95F166DPMC1 → MB95F166DPMC1/MB95166DPMC1)

The vertical lines marked in the left side of the page show the changes.

MEMO

FUJITSU MICROELECTRONICS LIMITED

Shinjuku Dai-Ichi Seimei Bldg., 7-1, Nishishinjuku 2-chome,
Shinjuku-ku, Tokyo 163-0722, Japan
Tel: +81-3-5322-3347 Fax: +81-3-5322-3387
http://jp.fujitsu.com/fml/en/

For further information please contact:

North and South America
FUJITSU MICROELECTRONICS AMERICA, INC.
1250 E. Arques Avenue, M/S 333
Sunnyvale, CA 94085-5401, U.S.A.
Tel: +1-408-737-5600 Fax: +1-408-737-5999
http://www.fma.fujitsu.com/

Europe
FUJITSU MICROELECTRONICS EUROPE GmbH
Pittlerstrasse 47, 63225 Langen, Germany
Tel: +49-6103-690-0 Fax: +49-6103-690-122
http://emea.fujitsu.com/microelectronics/

Korea
FUJITSU MICROELECTRONICS KOREA LTD.
206 Kosmo Tower Building, 1002 Daechi-Dong,
Gangnam-Gu, Seoul 135-280, Republic of Korea
Tel: +82-2-3484-7100 Fax: +82-2-3484-7111
http://kr.fujitsu.com/fmk/

Asia Pacific
FUJITSU MICROELECTRONICS ASIA PTE. LTD.
151 Lorong Chuan,
#05-08 New Tech Park 556741 Singapore
Tel : +65-6281-0770 Fax : +65-6281-0220
http://www.fmal.fujitsu.com/

FUJITSU MICROELECTRONICS SHANGHAI CO., LTD.
Rm. 3102, Bund Center, No.222 Yan An Road (E),
Shanghai 200002, China
Tel : +86-21-6146-3688 Fax : +86-21-6335-1605
http://cn.fujitsu.com/fmc/

FUJITSU MICROELECTRONICS PACIFIC ASIA LTD.
10/F., World Commerce Centre, 11 Canton Road,
Tsimshatsui, Kowloon, Hong Kong
Tel : +852-2377-0226 Fax : +852-2376-3269
http://cn.fujitsu.com/fmc/en/

Specifications are subject to change without notice. For further information please contact each office.

All Rights Reserved.
The contents of this document are subject to change without notice.
Customers are advised to consult with sales representatives before ordering.
The information, such as descriptions of function and application circuit examples, in this document are presented solely for the purpose of reference to show examples of operations and uses of FUJITSU MICROELECTRONICS device; FUJITSU MICROELECTRONICS does not warrant proper operation of the device with respect to use based on such information. When you develop equipment incorporating the device based on such information, you must assume any responsibility arising out of such use of the information.
FUJITSU MICROELECTRONICS assumes no liability for any damages whatsoever arising out of the use of the information.
Any information in this document, including descriptions of function and schematic diagrams, shall not be construed as license of the use or exercise of any intellectual property right, such as patent right or copyright, or any other right of FUJITSU MICROELECTRONICS or any third party or does FUJITSU MICROELECTRONICS warrant non-infringement of any third-party's intellectual property right or other right by using such information. FUJITSU MICROELECTRONICS assumes no liability for any infringement of the intellectual property rights or other rights of third parties which would result from the use of information contained herein.
The products described in this document are designed, developed and manufactured as contemplated for general use, including without limitation, ordinary industrial use, general office use, personal use, and household use, but are not designed, developed and manufactured as contemplated (1) for use accompanying fatal risks or dangers that, unless extremely high safety is secured, could have a serious effect to the public, and could lead directly to death, personal injury, severe physical damage or other loss (i.e., nuclear reaction control in nuclear facility, aircraft flight control, air traffic control, mass transport control, medical life support system, missile launch control in weapon system), or (2) for use requiring extremely high reliability (i.e., submersible repeater and artificial satellite).
Please note that FUJITSU MICROELECTRONICS will not be liable against you and/or any third party for any claims or damages arising in connection with above-mentioned uses of the products.
Any semiconductor devices have an inherent chance of failure. You must protect against injury, damage or loss from such failures by incorporating safety design measures into your facility and equipment such as redundancy, fire protection, and prevention of over-current levels and other abnormal operating conditions.
Exportation/release of any products described in this document may require necessary procedures in accordance with the regulations of the Foreign Exchange and Foreign Trade Control Law of Japan and/or US export control laws.
The company names and brand names herein are the trademarks or registered trademarks of their respective owners.

Edited: Sales Promotion Department