

Phase Control Thyristors (Hockey PUK Version), 960 A



TO-200AB (E-PUK)

FEATURES

- Center amplifying gate
- Metal case with ceramic insulator
- International standard case TO-200AB (E-PUK)
- Extended temperature range
- Low profile hockey PUK to increase current-carrying capability
- Lead (Pb)-free
- Designed and qualified for industrial level



RoHS
COMPLIANT

PRODUCT SUMMARY

$I_{T(AV)}$	960 A
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TYPICAL APPLICATIONS

- DC motor controls
- Controlled DC power supplies
- AC controllers

MAJOR RATINGS AND CHARACTERISTICS

PARAMETER	TEST CONDITIONS	VALUES	UNITS
$I_{T(AV)}$		960	A
	T_{hs}	80	°C
$I_{T(RMS)}$		2220	A
	T_{hs}	25	°C
I_{TSM}	50 Hz	12 500	A
	60 Hz	13 000	
I^2t	50 Hz	782	kA ² s
	60 Hz	713	
V_{DRM}/V_{RRM}		400 to 600	V
t_q	Typical	100	µs
T_J		- 40 to 150	°C

ELECTRICAL SPECIFICATIONS

VOLTAGE RATINGS

TYPE NUMBER	VOLTAGE CODE	V_{DRM}/V_{RRM} , MAXIMUM REPETITIVE PEAK AND OFF-STATE VOLTAGE V	V_{RSM} , MAXIMUM NON-REPETITIVE PEAK VOLTAGE V	I_{DRM}/I_{RRM} MAXIMUM AT $T_J = T_J$ MAXIMUM mA
ST380CH..C	04	400	500	100
	06	600	700	

ABSOLUTE MAXIMUM RATINGS							
PARAMETER	SYMBOL	TEST CONDITIONS			VALUES	UNITS	
Maximum average on-state current at heatsink temperature	I _{T(AV)}	180° conduction, half sine wave double side (single side) cooled			960 (440)	A	
					80 (110)	°C	
Maximum RMS on-state current	I _{T(RMS)}	DC at 25 °C heatsink temperature double side cooled			2220		
Maximum peak, one-cycle non-repetitive surge current	I _{TSM}	t = 10 ms	No voltage reapplied	Sinusoidal half wave, initial T _J = T _J maximum	12 500	A	
		t = 8.3 ms			13 000		
		t = 10 ms	100 % V _{RRM} reapplied		10 500		
		t = 8.3 ms			11 000		
Maximum I ² t for fusing	I ² t	t = 10 ms	No voltage reapplied		782	kA ² s	
		t = 8.3 ms			713		
		t = 10 ms	100 % V _{RRM} reapplied		553		
		t = 8.3 ms			505		
Maximum I ² √t for fusing	I ² √t	t = 0.1 to 10 ms, no voltage reapplied			7820	kA ² √s	
Low level value of threshold voltage	V _{T(TO)1}	(16.7 % x π x I _{T(AV)} < I < π x I _{T(AV)}), T _J = T _J maximum			0.85	V	
High level value of threshold voltage	V _{T(TO)2}	(I > π x I _{T(AV)}), T _J = T _J maximum			0.88		
Low level value of on-state slope resistance	r _{t1}	(16.7 % x π x I _{T(AV)} < I < π x I _{T(AV)}), T _J = T _J maximum			0.25	mΩ	
High level value of on-state slope resistance	r _{t2}	(I > π x I _{T(AV)}), T _J = T _J maximum			0.24		
Maximum on-state voltage	V _{TM}	I _{pk} = 2900 A, T _J = T _J maximum, t _p = 10 ms sine pulse			1.58	V	
Maximum holding current	I _H	T _J = 25 °C, anode supply 12 V resistive load			600	mA	
Typical latching current	I _L				1000		

SWITCHING				
PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS
Maximum non-repetitive rate of rise of turned-on current	di/dt	Gate drive 20 V, 20 Ω, $t_r \leq 1$ μs $T_J = T_J$ maximum, anode voltage $\leq 80 \% V_{DRM}$	1000	A/μs
Typical delay time	t_d	Gate current 1 A, $di_g/dt = 1$ A/μs $V_d = 0.67 \% V_{DRM}$, $T_J = 25$ °C	1.0	μs
Typical turn-off time	t_q	$I_{TM} = 550$ A, $T_J = T_J$ maximum, $di/dt = 40$ A/μs, $V_R = 50$ V, $dV/dt = 20$ V/μs, gate 0 V 100 Ω, $t_p = 500$ μs	100	

BLOCKING				
PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS
Maximum critical rate of rise of off-state voltage	dV/dt	$T_J = T_J$ maximum linear to 80 % rated V_{DRM}	500	V/μs
Maximum peak reverse and off-state leakage current	I_{RRM} , I_{DRM}	$T_J = T_J$ maximum, rated V_{DRM}/V_{RRM} applied	100	mA



TRIGGERING						
PARAMETER	SYMBOL	TEST CONDITIONS		VALUES		UNITS
				TYP.	MAX.	
Maximum peak gate power	P _{GM}	T _J = T _J maximum, t _p ≤ 5 ms		10.0		W
Maximum average gate power	P _{G(AV)}	T _J = T _J maximum, f = 50 Hz, d% = 50		2.0		
Maximum peak positive gate current	I _{GM}	T _J = T _J maximum, t _p ≤ 5 ms		3.0		A
Maximum peak positive gate voltage	+ V _{GM}	T _J = T _J maximum, t _p ≤ 5 ms		20		V
Maximum peak negative gate voltage	- V _{GM}			5.0		
DC gate current required to trigger	I _{GT}	T _J = - 40 °C	Maximum required gate trigger/ current/voltage are the lowest value which will trigger all units 12 V anode to cathode applied	200	-	mA
		T _J = 25 °C		100	200	
		T _J = 150 °C		40	-	
DC gate voltage required to trigger	V _{GT}	T _J = - 40 °C		2.5	-	V
		T _J = 25 °C		1.8	3.0	
		T _J = 150 °C		1.0	-	
DC gate current not to trigger	I _{GD}	T _J = T _J maximum	Maximum gate current/voltage not to trigger is the maximum value which will not trigger any unit with rated V _{DRM} anode to cathode applied	10		mA
DC gate voltage not to trigger	V _{GD}			0.25		V

THERMAL AND MECHANICAL SPECIFICATIONS					
PARAMETER	SYMBOL	TEST CONDITIONS		VALUES	UNITS
Maximum operating junction temperature range	T_J			- 40 to 150	°C
Maximum storage temperature range	T_{Stg}				
Maximum thermal resistance, junction to heatsink	R_{thJ-hs}	DC operation single side cooled		0.09	K/W
		DC operation double side cooled		0.04	
Maximum thermal resistance, case to heatsink	R_{thC-hs}	DC operation single side cooled		0.02	
		DC operation double side cooled		0.01	
Mounting force, ± 10 %				9800 (1000)	N (kg)
Approximate weight				83	g
Case style		See dimensions - link at the end of datasheet		TO-200AB (E-PUK)	

ΔR_{thJ-hs} CONDUCTION						
CONDUCTION ANGLE	SINUSOIDAL CONDUCTION		RECTANGULAR CONDUCTION		TEST CONDITIONS	UNITS
	SINGLE SIDE	DOUBLE SIDE	SINGLE SIDE	DOUBLE SIDE		
180°	0.010	0.011	0.007	0.007	$T_J = T_J$ maximum	K/W
120°	0.012	0.012	0.012	0.013		
90°	0.015	0.015	0.016	0.017		
60°	0.022	0.022	0.023	0.023		
30°	0.036	0.036	0.036	0.037		

Note

- The table above shows the increment of thermal resistance R_{thJ-hs} when devices operate at different conduction angles than DC

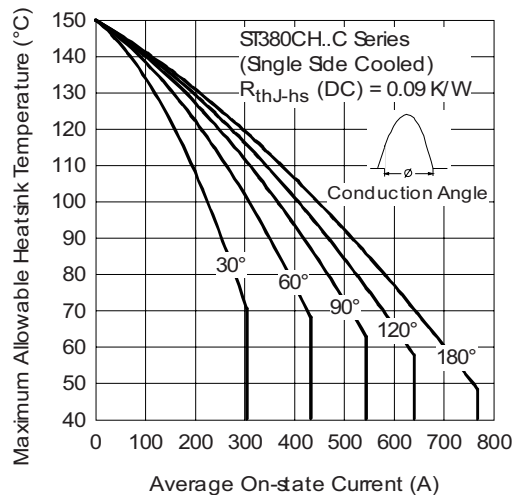


Fig. 1 - Current Ratings Characteristics

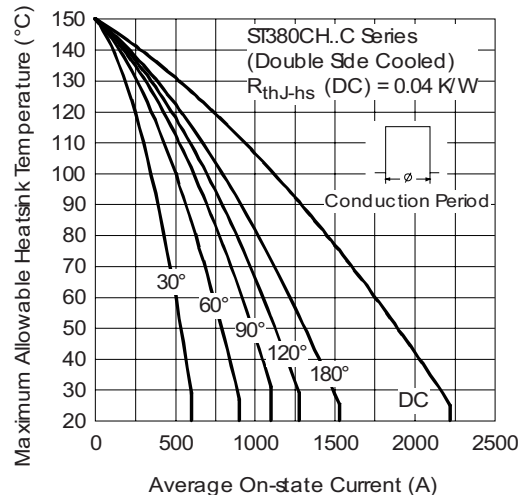


Fig. 4 - Current Ratings Characteristics

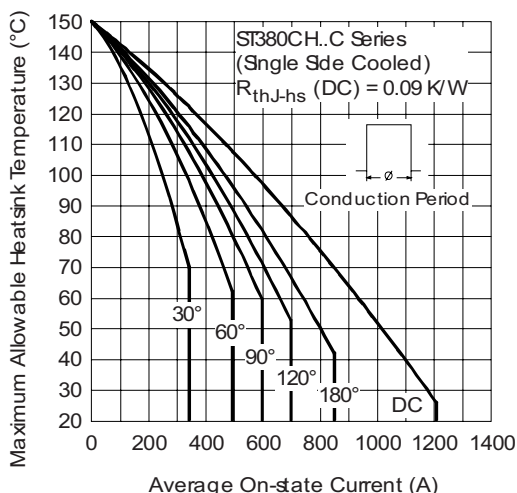


Fig. 2 - Current Ratings Characteristics

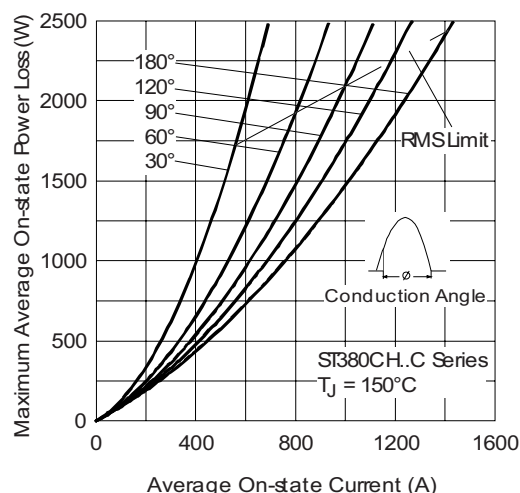


Fig. 5 - On-State Power Loss Characteristics

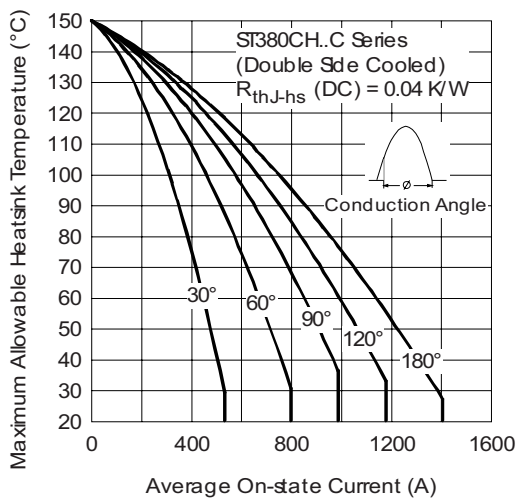


Fig. 3 - Current Ratings Characteristics

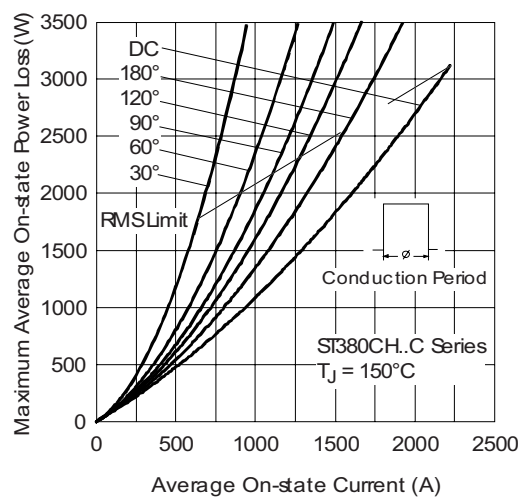


Fig. 6 - On-State Power Loss Characteristics

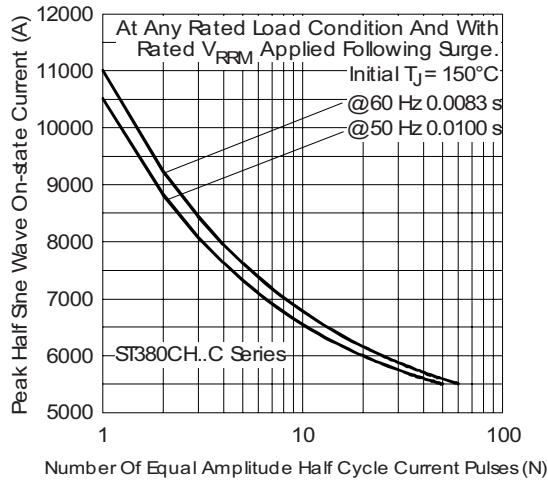


Fig. 7 - Maximum Non-Repetitive Surge Current Single and Double Side Cooled

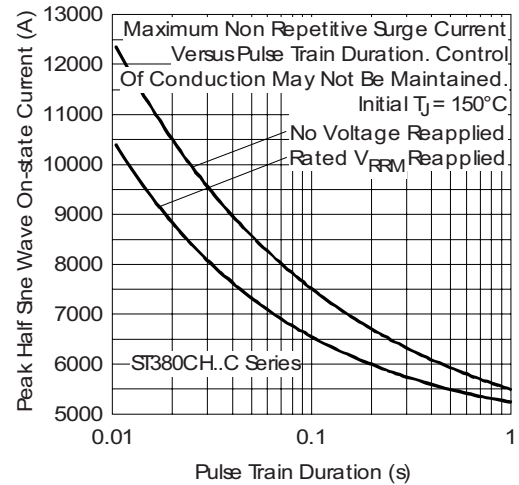


Fig. 8 - Maximum Non-Repetitive Surge Current Single and Double Side Cooled

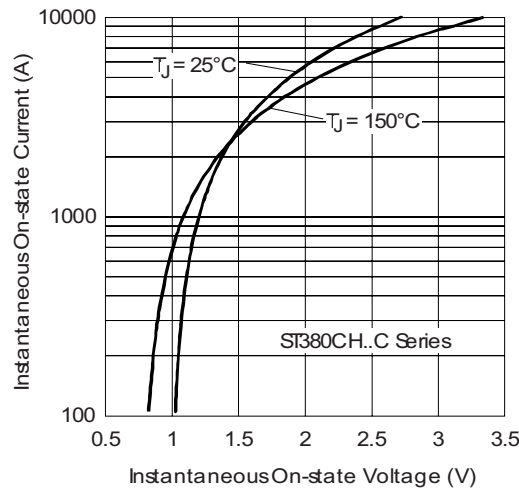


Fig. 9 - On-State Voltage Drop Characteristics

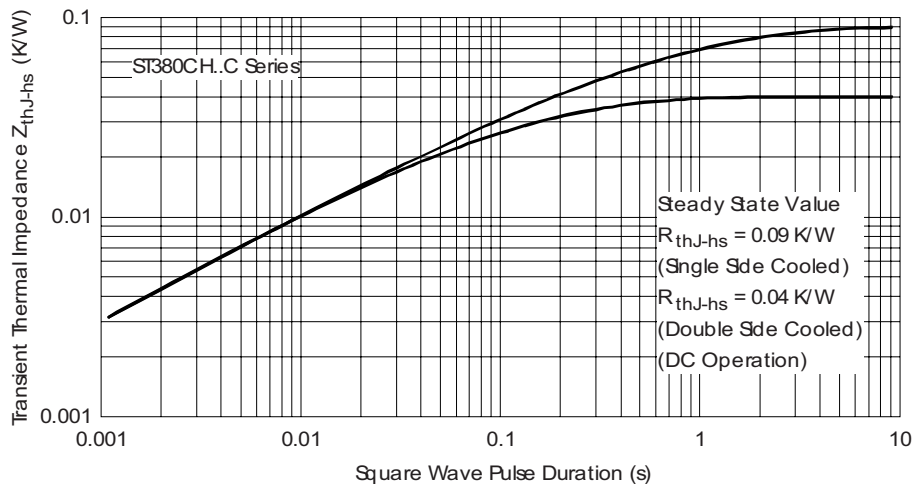
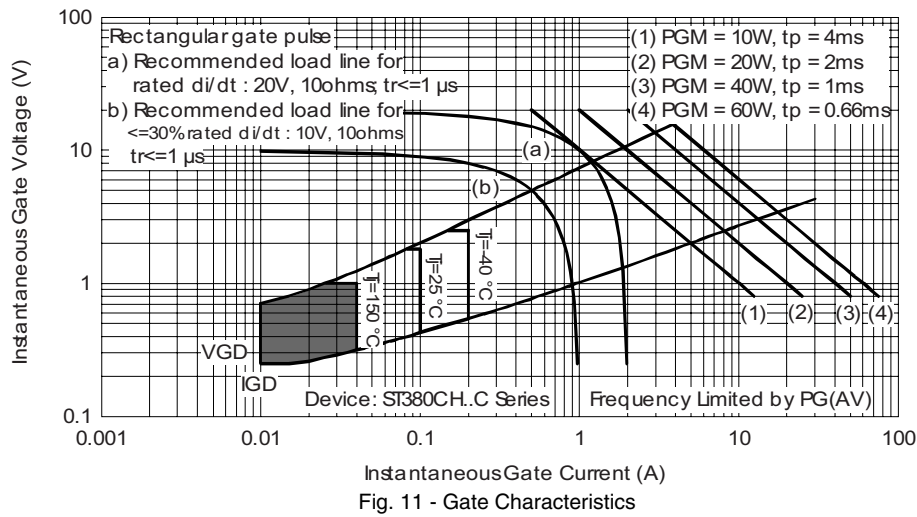


Fig. 10 - Thermal Impedance Z_{thJ-hs} Characteristics

ST380CHPbF Series



Vishay High Power Products Phase Control Thyristors
(Hockey PUK Version), 960 A



ORDERING INFORMATION TABLE

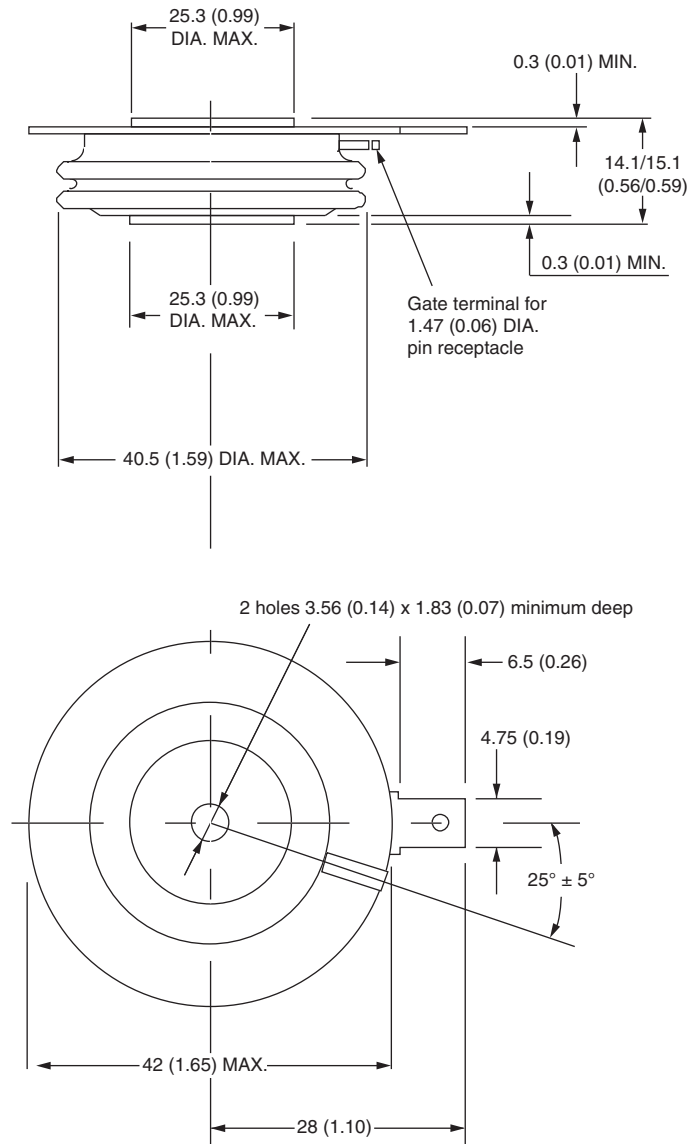
Device code	ST	38	0	CH	06	C	1	-	PbF
	①	②	③	④	⑤	⑥	⑦	⑧	⑨
①	-	Thyristor							
②	-	Essential part number							
③	-	0 = Converter grade							
④	-	CH = Ceramic PUK, high temperature							
⑤	-	Voltage code x 100 = V_{RRM} (see Voltage Ratings table)							
⑥	-	C = PUK case TO-200AB (E-PUK)							
⑦	-	0 = Eyelet terminals (gate and auxiliary cathode unsoldered leads)							
		1 = Fast-on terminals (gate and auxiliary cathode unsoldered leads)							
		2 = Eyelet terminals (gate and auxiliary cathode soldered leads)							
		3 = Fast-on terminals (gate and auxiliary cathode soldered leads)							
⑧	-	Critical dV/dt : • None = 500 V/ μs (standard selection)							
		• L = 1000 V/ μs (special selection)							
⑨	-	Lead (Pb)-free							

LINKS TO RELATED DOCUMENTS	
Dimensions	http://www.vishay.com/doc?95075

TO-200AB (E-PUK)

DIMENSIONS in millimeters (inches)

Anode to gate
Creepage distance: 11.18 (0.44) minimum
Strike distance: 7.62 (0.30) minimum



Quote between upper and lower pole pieces has to be considered after application of mounting force (see thermal and mechanical specification)



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