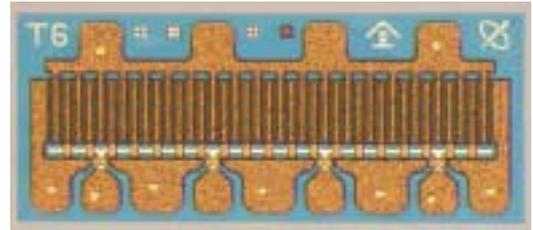


2W High Linearity and High Efficiency GaAs Power FETs

FEATURES

- 2W Typical Power at 6 GHz
- Linear Power Gain: $G_L = 8$ dB Typical at 6 GHz
- High Linearity: $IP_3 = 43$ dBm Typical at 6 GHz
- Non-Via Holes Source for Self-Bias Application
- Suitable for High Reliability Application
- Breakdown Voltage: $BV_{DGO} \geq 18$ V
- $L_g = 0.6$ μ m, $W_g = 5$ mm
- High Power Added Efficiency: Nominal PAE of 43 % at 6 GHz
- Tight V_p ranges control
- High RF input power handling capability
- 100 % DC Tested

PHOTO ENLARGEMENT



DESCRIPTION

The TC1606N is a GaAs Pseudomorphic High Electron Mobility Transistor (PHEMT) GaAs Power FET, which has high linearity and high Power Added Efficiency. The device is processed without via-holes for self-bias applications. The long gate length makes the device to have high breakdown voltage. All devices are 100% DC tested to assure consistent quality. Bond pads are gold plated for either thermo-compression or thermo-sonic wire bonding. Backside gold plating is compatible with standard AuSn die-attach. Typical application include commercial and military high performance power amplifier.

ELECTRICAL SPECIFICATIONS ($T_A = 25$ °C)

Symbol	Conditions	MIN	TYP	MAX	UNIT
P_{1dB}	Output Power at 1dB Gain Compression Point, $f = 6$ GHz $V_{DS} = 8$ V, $I_{DS} = 500$ mA	32.5	33		dBm
G_L	Linear Power Gain, $f = 6$ GHz $V_{DS} = 8$ V, $I_{DS} = 500$ mA		8		dB
IP_3	Intercept Point of the 3 rd -order Intermodulation, $f = 6$ GHz $V_{DS} = 8$ V, $I_{DS} = 500$ mA, $*P_{SCL} = 20$ dBm		43		dBm
PAE	Power Added Efficiency at 1dB Compression Power, $f = 6$ GHz		43		dB
I_{DSS}	Saturated Drain-Source Current at $V_{DS} = 2$ V, $V_{GS} = 0$ V		1.2		A
g_m	Transconductance at $V_{DS} = 2$ V, $V_{GS} = 0$ V		850		mS
V_P	Pinch-off Voltage at $V_{DS} = 2$ V, $I_D = 10$ mA		-1.7**		Volts
BV_{DGO}	Drain-Gate Breakdown Voltage at $I_{DGO} = 2.5$ mA	18	22		Volts
R_{th}	Thermal Resistance		8		°C/W

Note:

* P_{SCL} : Output Power of Single Carrier Level.

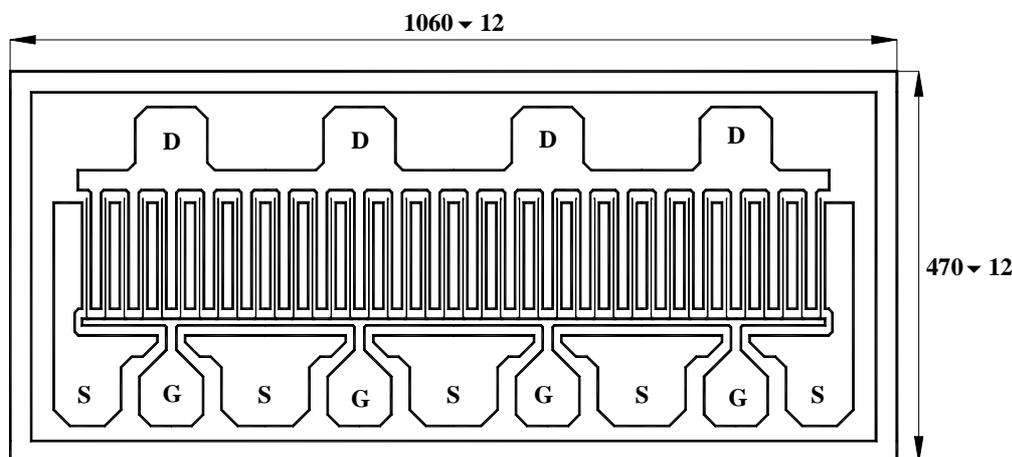
**For the tight control of the pinch-off voltage. TC1606N's are divided into 3 groups:

(1) **TC1606NP1519** : $V_p = -1.5$ V to -1.9 V (2) **TC1606NP1620** : $V_p = -1.6$ V to -2.0 V

(3) **TC1606NP1721** : $V_p = -1.7$ V to -2.1 V In addition, the customers may specify their requirements.

ABSOLUTE MAXIMUM RATINGS (T_A=25 °C)

Symbol	Parameter	Rating
V _{DS}	Drain-Source Voltage	12.0 V
V _{GS}	Gate-Source Voltage	-5.0 V
I _{DS}	Drain Current	I _{DSS}
P _{in}	RF Input Power, CW	30 dBm
P _T	Continuous Dissipation	7.7 W
T _{CH}	Channel Temperature	175 °C
T _{STG}	Storage Temperature	- 65 °C to +175 °C

CHIP DIMENSIONS


Units: Micrometers

Gate Pad: 76.0 x 59.5

Chip Thickness: 50

Drain Pad: 86.0 x 76.0

CHIP HANDLING

DIE ATTACHMENT: Conductive epoxy or eutectic die attach is recommended. Eutectic die attach can be accomplished with Au-Sn (80% Au-20%Sn) perform at stage temperature: 290°C ± 5°C; Handling Tool: Tweezers; Time: less than 1min.

WIRE BONDING: The recommended wire bond method is thermocompression bonding with 0.7 to 1.0 mil (0.018 to 0.025 mm) gold wire. Stage temperature: 220°C to 250°C; Bond Tip Temperature: 150°C; Bond Force: 20 to 30 gms depending on size of wire and Bond Tip Temperature.

HANDLING PRECAUTIONS: The user must operate in a clean, dry environment. Care should be exercised during handling avoid damage to the devices. Electrostatic Discharge (ESD) precautions should be observed at all stages of storage, handling, assembly, and testing. The static discharge must be less than 300V.