LCD Driver for 160 Display Units BL55077

1 General Description

The BL55077 is a general LCD driver IC for 160 units LCD panel. It features a wide operating supply voltage range, incorporates simple communication interface with microcomputer and is suitable for multiple application.

2 Features

- Advanced low power CMOS Technology
- Selection of 1/2 or 1/3 bias, selection of 1/2 or 1/3 or 1/4 duty.
- Operation voltage: 2.5~5.5V
- Serial data interface
- 160(40x4) Display Units
- Low power dissipation design: Power saving mode: Idd=14uA at 5V and Idd=9uA at 3.3V; Sleeping mode: Idd<2uA
- Maybe cascaded up to 16PCs for large LCD applications
- On-chip RC oscillator
- VLCD for adjusting LCD operating voltage
- Excellent EMC immunity
- Compatible with general microcomputer

3 Pin Assignment

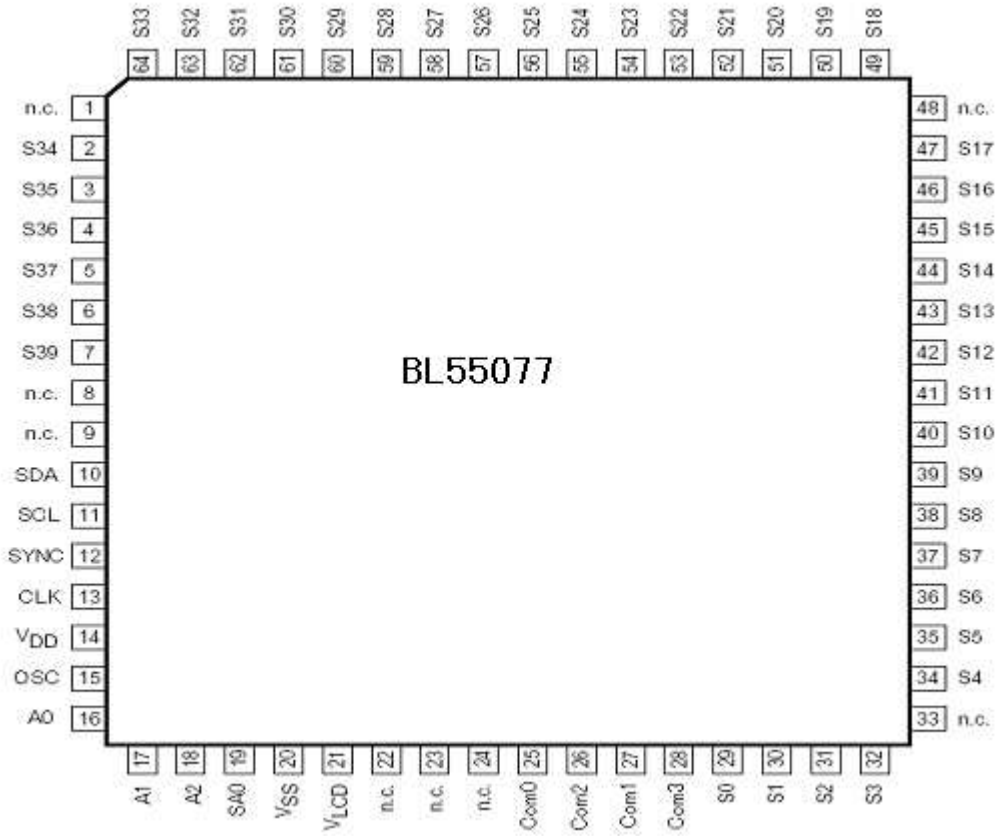


Fig 1

4 Pin Description

Pin No.	Pin name	Function
10	SDA	Serial data input/output
11	SCI	Serial clock input
12	SYNC	Cascade synchronization clock
13	CLK	External clock input
14	Vdd	Supply voltage
15	OSC	Oscillator input
16-18	A0、A1、A2	Subaddress inputs
19	SA0	Slave address input;bit0
20	Vss	ground
21	Vlcd	LCD supply voltage
25-28	Com0、Com2、Com1、Com3	Common terminal driving output
29-32、34-37、49-64、2-7	S0——S39	Segment terminal driving output
1、8、9、22、23、24、33、48	NC	Unused

Tab.1

5 Function Description

1. function circuit

The BL550077 has all function circuits that can directly drive any static or multiplexed LCD containing up to four commons and up to 40 segments. The function circuits include:Power-on reset, LCD bias generator, LCD voltage selector, Oscillator, display RAM, Timing, Display latch, Shift register, Common/segment outputs, input/output bank selector, Blinker, Data pointer, Subaddress counter,etc.

2. display function decription

The display RAM is a static 40x 4-bit RAM which stores LCD data. A logic 1 in the RAM bit-map indicates the on state of the corresponding LCD segment; similarly, a logic 0 indicates the off state. There is a one-to-one correspondence between the RAM addresses and the segment outputs, and between the individual bits of a RAM word and the common outputs. (see Fig.2).

Display RAM address and SEGMENT（S0~S39）output													
COM (Com0~ Com3) 输出		0	1	2	3	。	。	。	。	36	37	38	39
	0												
	1												
	2												
	3												

Fig2

When display data is transmitted to the BL55077, the display bytes received are stored in the display RAM in accordance with the selected LCD drive mode. To illustrate the filling order, an example of a 7-segment numeric display showing all drive modes is given in Fig.3; the RAM filling organization depicted applies equally to other LCD types.

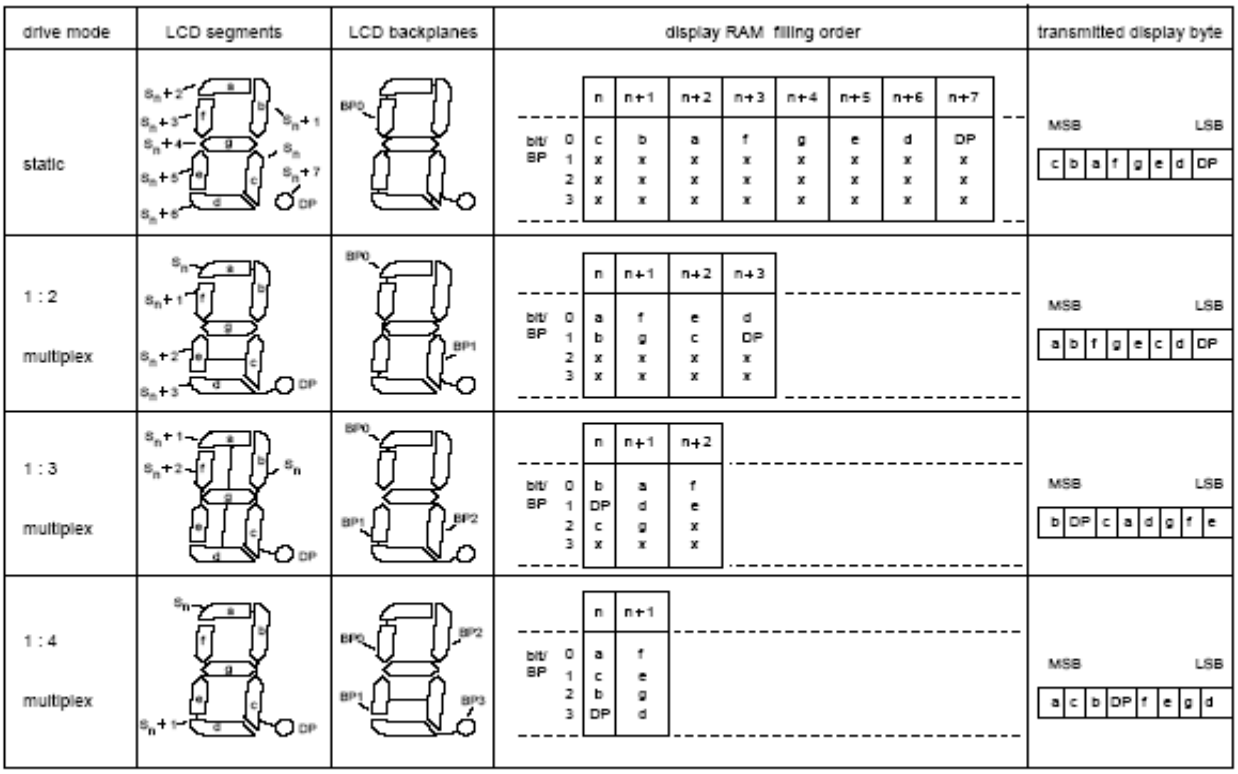


Fig 3

3. I²C-bus protocol

Two I²C-bus slave addresses (0111000 and 0111001) are reserved for the BL55077. The least significant bit of the slave address that a BL55077 will respond to is defined by the level tied at its input SA0. Therefore, two types of BL55077 can be distinguished on the same I²C-bus which allows:

1. Up to 16 BL55077 on the same I2C-bus for very large LCD applications.
2. The use of two types of LCD multiplex on the same I2C-bus.

The I2C-bus protocol is shown in Fig.4. The sequence is initiated with a START condition (S) from the I2C-bus master which is followed by one of the two BL55077 slave addresses available. All BL55077s with the corresponding SA0 level acknowledge in parallel with the slave address but all BL55077s with the alternative SA0 level ignore the whole I2C-bus transfer. After acknowledgement, one or more command bytes (m) follow which define the status of the addressed BL55077s. The last command byte is tagged with a cleared most significant bit, the continuation bit C. The command bytes are also acknowledged by all addressed BL55077s on the bus. After the last command byte, a series of display data bytes(n) may follow. These display bytes are stored in the display RAM at the address specified by the data pointer and the subaddress counter. Both data pointer and subaddress counter are automatically updated and the data is directed to the intended BL55077 device. The acknowledgement after each byte is made only by the (A0, A1 and A2) addressed BL55077. After the last display byte, the I2C-bus master issues a STOP condition (P).

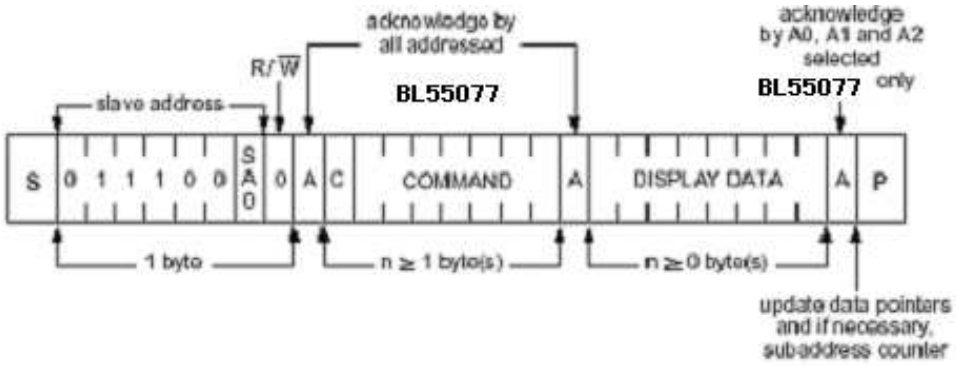
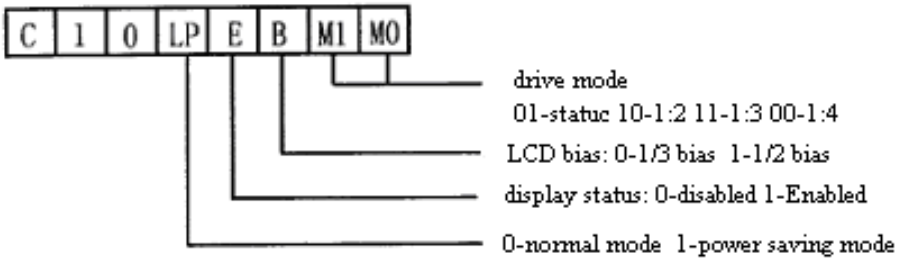


Fig 4

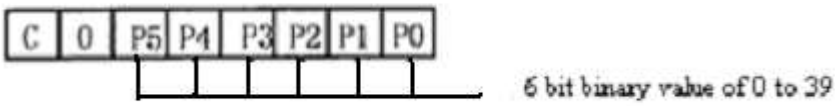
4. command decoder

The command decoder identifies command bytes that arrive on the I^2C-bus. All available commands carry a continuation bit C in their most significant bit position. The five commands available to the BL55077 are defined in Fig 5.

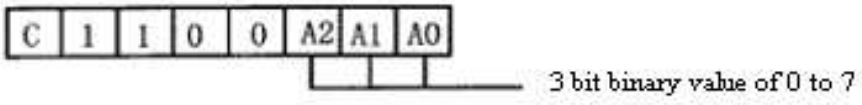
A. Mode set



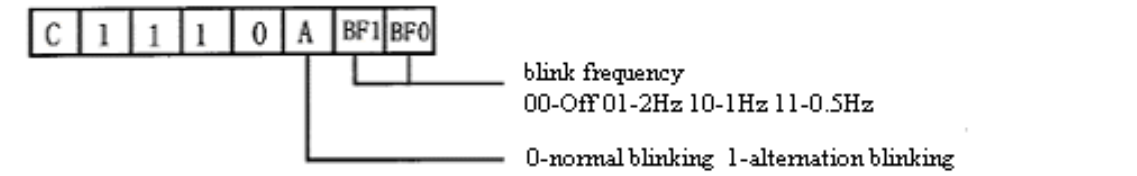
B. Load data pointer



C. Device select



D. Blink control



E. Sleep control

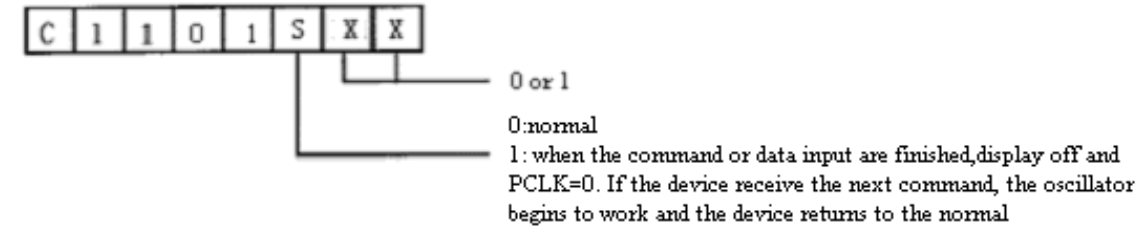


Fig 5

6 Absolute Maximum Rating

Parameter	Symbol	Rating	Unit
Supply voltage	Vdd	-0.5～+6.0	V
LCD operating voltage	Vlcd	0～ Vdd	V
Input voltage	Vi	Vss-0.5～Vdd+0.5	V
Output voltage	Vo	Vlcd-0.5～Vdd+0.5	V
Vdd,Vss,Vlcd current	Idd,Iss,Ilcd	-50～+50	mA
Maximum power consumption	Ptot	400	mW
Operating temperature	Topr	-40～ +75	°C
Storage temperature	Tstg	-65～ +150	°C

7 DC Characteristic

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
Vdd	IC Operating voltage		2.5	-	5.5	V
Vlcd	LCD operating voltage		0	-	Vdd-2	V
Idd1	Supply current	Vdd=5V, VLCD=0V, Normal mode, internal oscillator	-	25	50	uA
Idd2	Supply current	Vdd=5V, VLCD=0V, power saving mode, internal oscillator	-	14	30	uA
Idd3	Supply current	Vdd=3.3V, VLCD=0V, Normal mode, internal oscillator	-	16	30	uA
Idd4	Supply current	Vdd=3.3V, VLCD=0V, power saving mode, internal oscillator	-	9	15	uA
I_{SL}	Sleep current	Vdd=5V,VLCD=0V	-	1.5	2	uA
ViL	Low voltage input	SDA,SCL	Vss	-	0.3Vdd	V
ViH	High voltage input	SDA,SCL	0.7Vdd	-	6.0	V
Rph	Pull high resister	SYNC	30	60	100	kΩ

8 AC Characteristic

Ta=25°C

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
Fclk	Oscillator frequency	Vdd=5V,normal mode	125	180	300	KHz
Fclk	Oscillator frequency	Vdd=3.3V, power saving mode	21	31	48	KHz
Tclk	Half oscillator cycle		1	-	3	uA
Tsh1	CS start hold time		5	-		us
Tsh2	SCL start hold time		5	-		us
tlow	High time		5	-		us
thig	Low time		4	-		us
thd	SCL hold time		250			ns

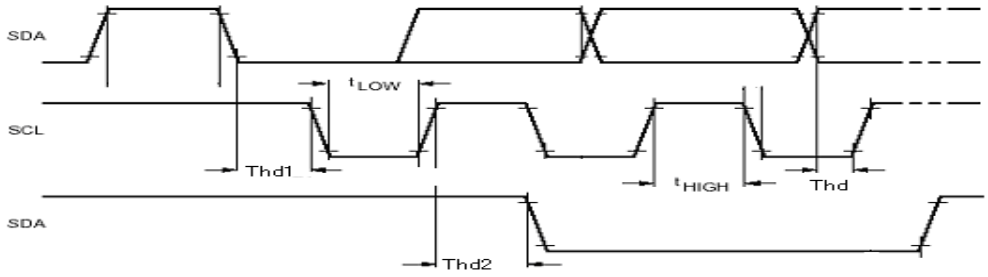


Fig 6

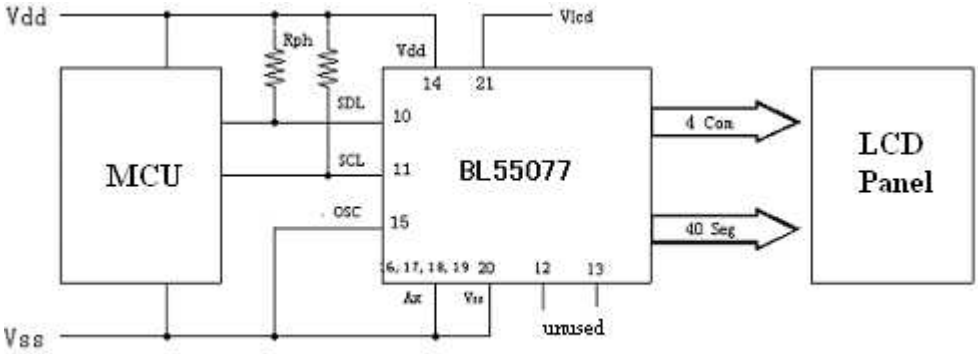
9 Typical Application Circuit

Note:1/ when I²C are idle mode,SDA and SCL must be connect to high level(by pull up resistor),otherwise the device maybe can not go into power saving mode.

2/ In power-saving mode, SCL frequency must be less than 21KHz.

3/ Work at 1/3 bias, Vdd – Vlcd must be more than 2.9V。

1/ single application



2/ cascade application

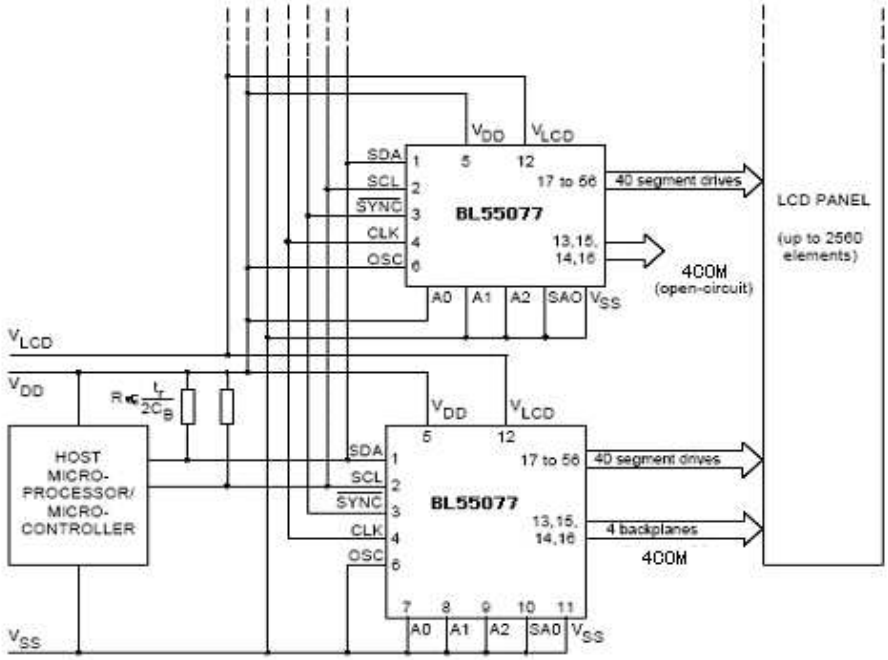
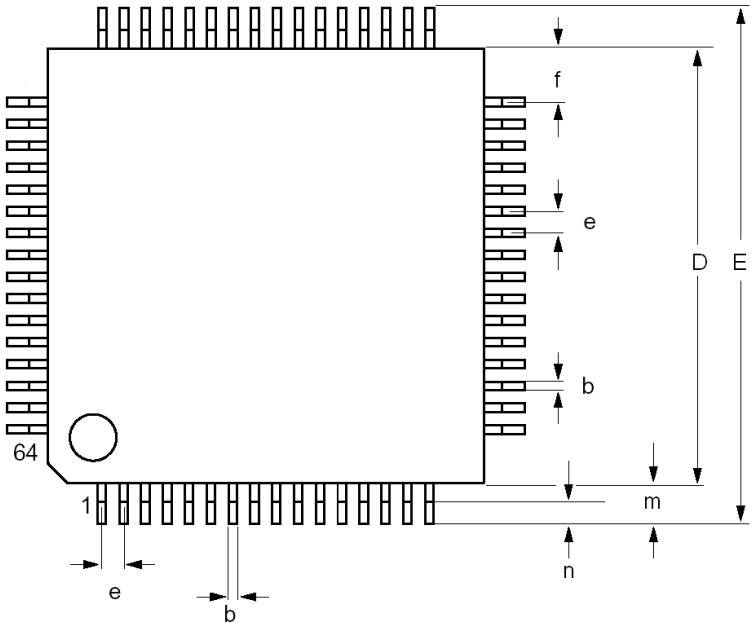


Fig 7

10 Package Outline LQFP64



Unit	D	E	e	b	f	m	n
mm(tolerance)	10.0(0.1)	12.0(0.15)	0.5	0.22(0.05)	1.25(0.2)	1.0	0.6(0.15)