



1.8V CMOS 16-BIT BUFFER/ DRIVER WITH INVERTED 3-STATE OUTPUTS

IDT74AUC16240

FEATURES:

- ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
- 1.8V Optimized
- 0.8V to 2.7V Operating Range
- Inputs/outputs tolerant up to 3.6V
- $\pm 9\text{mA}$ @ 2.3V output drivers
- Supports hot insertion
- Available in TSSOP, TVSOP, and VFBGA packages

APPLICATIONS:

- high performance, low voltage communications systems
- high performance, low voltage computing systems

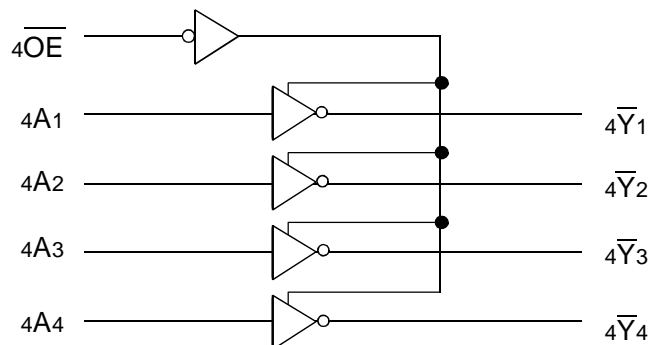
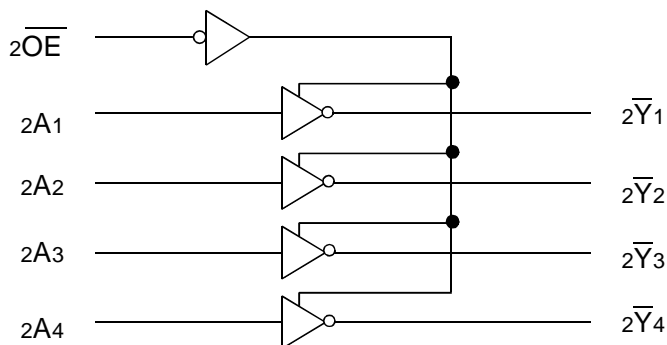
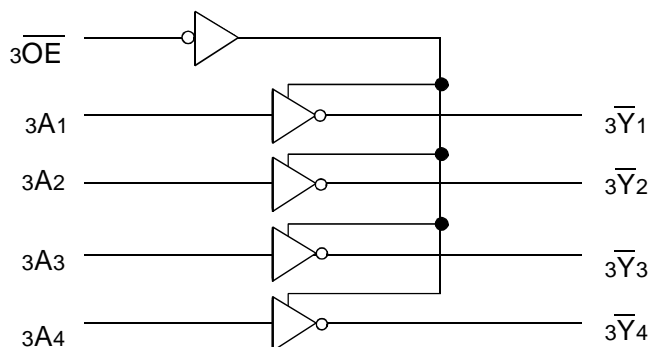
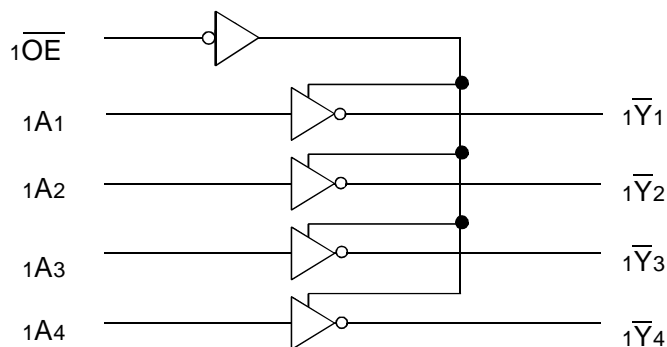
DESCRIPTION:

This 16-bit buffer/driver is built using advanced CMOS technology. The AUC16240 is designed specifically to improve the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. The device can be used as four 4-bit buffers, two 8-bit buffers, or one 16-bit buffer. It provides inverted outputs and symmetrical active-low output-enable ($\overline{\text{OE}}$) inputs.

This device is fully specified for partial power-down applications using IOFF. The IOFF circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

To ensure the high-impedance state during power up or power down, $\overline{\text{OE}}$ should be tied to V_{DD} through a pull-up resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

FUNCTIONAL BLOCK DIAGRAM



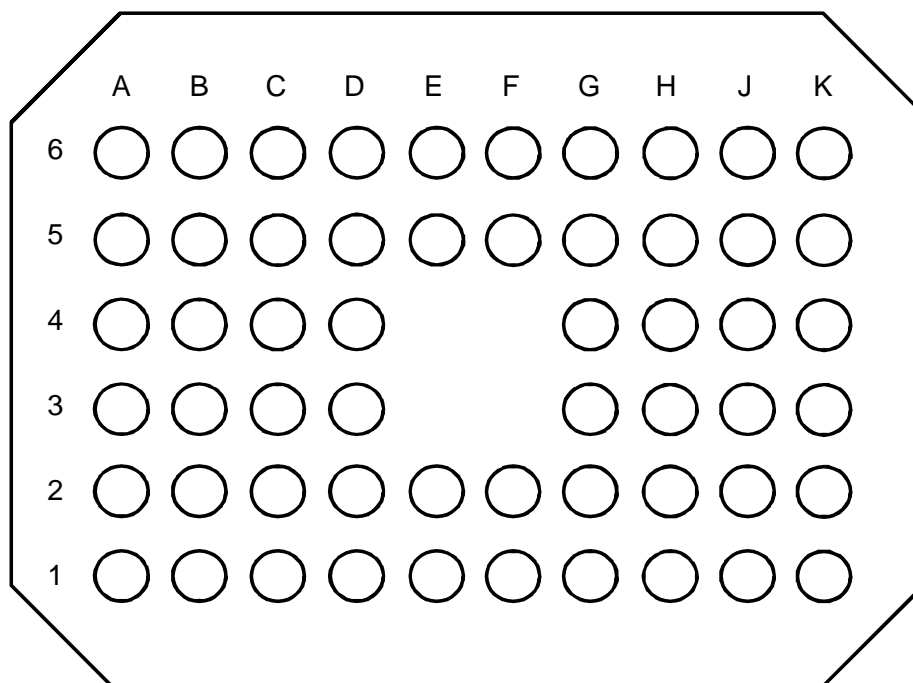
PINOUT CONFIGURATION

6	$2\overline{OE}$	1A2	1A4	2A2	2A4	3A1	3A3	4A1	4A3	$3\overline{OE}$
5	NC	1A1	1A3	2A1	2A3	3A2	3A4	4A2	4A4	NC
4	NC	GND	V _{DD}	GND			GND	V _{DD}	GND	NC
3	NC	GND	V _{DD}	GND			GND	V _{DD}	GND	NC
2	NC	$1\overline{Y}1$	$1\overline{Y}3$	$2\overline{Y}1$	$2\overline{Y}3$	$3\overline{Y}2$	$3\overline{Y}4$	$4\overline{Y}2$	$4\overline{Y}4$	NC
1	$1\overline{OE}$	$1\overline{Y}2$	$1\overline{Y}4$	$2\overline{Y}2$	$2\overline{Y}4$	$3\overline{Y}1$	$3\overline{Y}3$	$4\overline{Y}1$	$4\overline{Y}3$	$4\overline{OE}$
	A	B	C	D	E	F	G	H	J	K

VFBGA

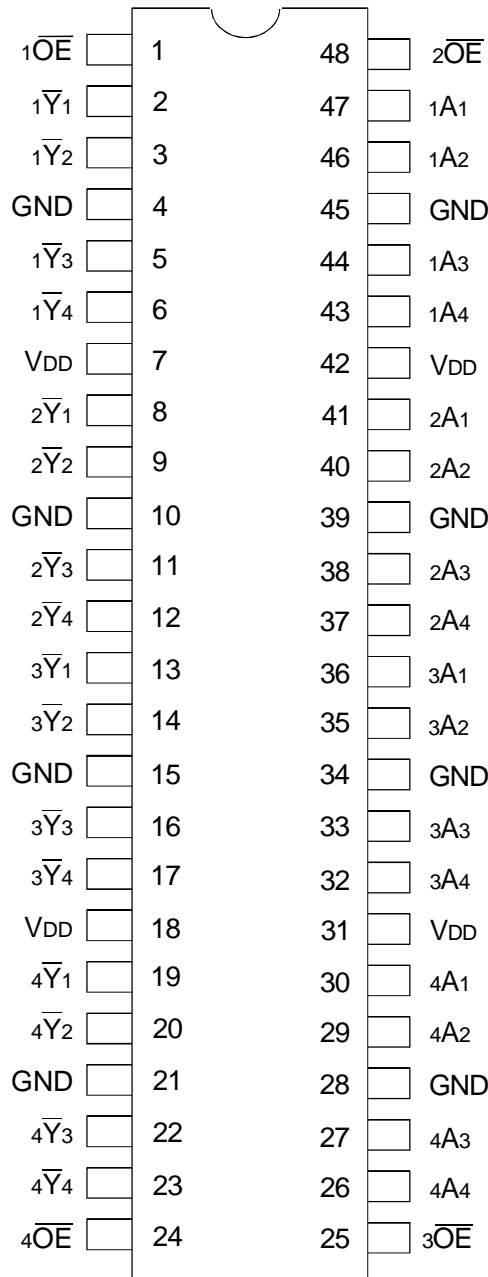
NOTE:
NC = No Internal Connection

56 BALL VFBGA PACKAGE LAYOUT



TOP VIEW

PIN CONFIGURATION



TSSOP/ TVSOP
TOP VIEW

PIN DESCRIPTION

Pin Names	Description
xOE	3-State Output Enable Inputs (Active Low)
xAx	Data Inputs
xYx	3-State Outputs

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Description	Max	Unit
VTERM	Terminal Voltage with Respect to GND (all input and VDD terminals)	-0.5 to +3.6	V
VTERM	Terminal Voltage with Respect to GND (any I/O or Output terminals in high-impedance or power-off state)	-0.5 to +3.6	V
VTERM	Terminal Voltage with Respect to GND (any I/O or Output terminals in high or low state)	-0.5 to +3.6	V
TSTG	Storage Temperature	-65 to +150	°C
IOUT	Continuous DC Output Current	±20	mA
I _{IK}	Continuous Clamp Current, V _i < 0, or V _i > V _{DD}	±50	mA
I _{OK}	Continuous Clamp Current, V _o < 0	-50	mA
I _{DD}	Continuous Current through each VDD or GND	±100	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0MHz, V_{DD} = 2.5V)

Symbol	Parameter	Conditions	Typ.	Max.	Unit
C _{IN} (1)	Input Capacitance	V _{IN} = 0V	3	4	pF
C _{OUT} (2)	Output Capacitance	V _{OUT} = 0V	5.5	6	pF
C _I (3)	Input Port Capacitance	V _{IN} = 0V	3	4	pF

NOTES:

1. Applies to Control Inputs.
2. Applies to Data Outputs.
3. Applies to Data Inputs.

FUNCTION TABLE (EACH 4-BIT BUFFER)(1)

Inputs		Output
xOE	xAx	xYx
L	H	L
L	L	H
H	X	Z

NOTE:

1. H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
Z = High-Impedance

RECOMMENDED OPERATING CHARACTERISTICS⁽¹⁾

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
V _{DD}	Supply Voltage		0.8	2.7	V
V _{IH}	Input HIGH Voltage Level	V _{DD} = 0.8V	V _{DD}	—	V
		V _{DD} = 1.1V to 1.3V	0.65 x V _{DD}	—	
		V _{DD} = 1.4V to 1.6V	0.65 x V _{DD}	—	
		V _{DD} = 1.65V to 1.95V	0.65 x V _{DD}	—	
		V _{DD} = 2.3V to 2.7V	1.7	—	
V _{IL}	Input LOW Voltage Level	V _{DD} = 0.8V	—	0	V
		V _{DD} = 1.1V to 1.3V	—	0.35 x V _{DD}	
		V _{DD} = 1.4V to 1.6V	—	0.35 x V _{DD}	
		V _{DD} = 1.65V to 1.95V	—	0.35 x V _{DD}	
		V _{DD} = 2.3V to 2.7V	—	0.7	
V _I	Input Voltage		0	2.7	V
V _O	Output Voltage	Active State	0	V _{DD}	V
		3-State	0	2.7	
I _{OH}	HIGH Level Output Current	V _{DD} = 0.8V	—	-0.7	mA
		V _{DD} = 1.1V	—	-3	
		V _{DD} = 1.4V	—	-5	
		V _{DD} = 1.65V	—	-8	
		V _{DD} = 2.3V	—	-9	
I _{OL}	LOW Level Output Current	V _{DD} = 0.8V	—	0.7	mA
		V _{DD} = 1.1V	—	3	
		V _{DD} = 1.4V	—	5	
		V _{DD} = 1.65V	—	8	
		V _{DD} = 2.3V	—	9	
Δt/Δv	Input Transition Rise or Fall Rate	V _{DD} = 0.8V to 1.3V	—	20	ns/V
		V _{DD} = 1.6V to 1.95V	—	10	
		V _{DD} = 2.7V	—	5	
T _A	Operating Free-Air Temperature		-40	+85	°C

NOTE:

1. All unused inputs of the device must be held at V_{DD} or GND to ensure proper operation.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE⁽¹⁾

Following Conditions Apply Unless Otherwise Specified:

Operating Conditions: T_A = -40°C to +85°C

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	
I _{IH}	Input HIGH or LOW Current	V _{DD} = 2.7V, V _I = V _{DD} or GND	—	—	±5	μA	
I _{IL}	All Inputs						
I _{OFF}	Input/Output Power Off Leakage	V _{DD} = 0V, V _{IN} or V _O ≤ 2.7V	—	—	±10	μA	
I _{OZH}	High Impedance Output Current (3-State Output Pins)	V _{DD} = 2.7V	V _O = V _{DD}	—	—	±10	μA
			V _O = GND	—	—	±10	
I _{DDL}	Quiescent Power Supply Current	V _{DD} = 0.8V to 2.7V V _{IN} = GND or V _{DD}	—	—	20	μA	
I _{DDH}							
I _{DDZ}							

NOTE:

1. All unused inputs of the device must be held at V_{DD} or GND to ensure proper operation.

OUTPUT DRIVE CHARACTERISTICS

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ.	Max.	Unit
VOH	Output HIGH Voltage	VDD = 0.8V - 2.7V	IOH = -100µA	VDD - 0.1	—	—	V
		VDD = 0.8V	IOH = -0.7mA	—	0.55	—	
		VDD = 1.1V ⁽²⁾	IOH = -3mA	0.8	—	—	
		VDD = 1.4V ⁽³⁾	IOH = -5mA	1	—	—	
		VDD = 1.65V ⁽⁴⁾	IOH = -8mA	1.2	—	—	
		VDD = 2.3V ⁽⁵⁾	IOH = -9mA	1.8	—	—	
VOL	Output LOW Voltage	VDD = 0.8V - 2.7V	IOH = 100µA	—	—	0.2	V
		VDD = 0.8V	IOL = 0.7mA	—	0.25	—	
		VDD = 1.1V ⁽²⁾	IOL = 3mA	—	—	0.3	
		VDD = 1.4V ⁽³⁾	IOL = 5mA	—	—	0.4	
		VDD = 1.65V ⁽⁴⁾	IOL = 8mA	—	—	0.45	
		VDD = 2.3V ⁽⁵⁾	IOL = 9mA	—	—	0.6	

NOTES:

1. VIL and VIH must be within the min. or max. range shown in the DC ELECTRICAL CHARACTERISTICS table for the appropriate VDD range. TA = -40°C to +85°C.
2. Demonstrates operation for nominal VDD = 1.2V.
3. Demonstrates operation for nominal VDD = 1.5V.
4. Demonstrates operation for nominal VDD = 1.8V.
5. Demonstrates operation for nominal VDD = 2.5V.

OPERATING CHARACTERISTICS, TA = 25°C

Symbol	Parameter	Test Conditions	VDD = 0.8V	VDD = 1.2V	VDD = 1.5V	VDD = 1.8V	VDD = 2.5V	Unit
CPD	Power Dissipation Capacitance Outputs Enabled	CL = 0pF f = 10MHz	24	24	25	26	30	pF
CPD	Power Dissipation Capacitance Outputs Disabled		2	2	2	3	4	pF

SWITCHING CHARACTERISTICS⁽¹⁾

Symbol	Parameter	VDD = 0.8V	VDD = 1.2V±0.1V			VDD = 1.5V±0.1V			VDD = 1.8V±0.15V			VDD = 2.5V±0.2V		Unit
		Typ.	Min.	Max.	Min.	Max.	Min.	Typ.	Max.	Min.	Max.			
tPLH tPHL	Propagation Delay xAx to xYx	5.9	0.9	2.6	0.7	1.8	0.6	1.4	2	0.4	1.6	ns		
tPZH tPZL	Output Enable Time xOE to xYx	7.9	1.2	3.8	0.8	2.5	0.7	1.5	2.5	0.7	2	ns		
tPHZ tPLZ	Output Disable Time xOE to xYx	9.3	2.1	6	1.5	4.8	1.8	2.7	4.5	0.6	2.3	ns		

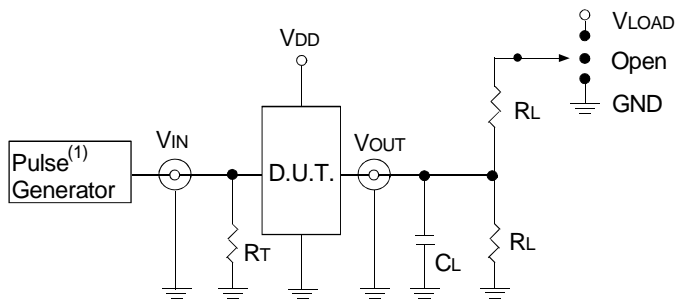
NOTE:

1. See TEST CIRCUITS AND WAVEFORMS. TA = -40°C to +85°C.

TEST CIRCUITS AND WAVEFORMS

TEST CONDITIONS⁽¹⁾

Symbol	V _{DD} = 0.8V	V _{DD} = 1.2V±0.1V	V _{DD} = 1.5V±0.1V	V _{DD} = 1.8V±0.15V	V _{DD} = 2.5V±0.2V	Unit
V _{LOAD}	2xV _{DD}	2xV _{DD}	2xV _{DD}	2xV _{DD}	2xV _{DD}	V
V _T	V _{DD} /2	V _{DD} /2	V _{DD} /2	V _{DD} /2	V _{DD} /2	V
V _{LZ}	100	100	100	150	150	mV
V _{HZ}	100	100	100	150	150	mV
R _L	2	2	2	1	0.5	KΩ
C _L	15	15	15	30	30	pF



Test Circuits for All Outputs

DEFINITIONS:

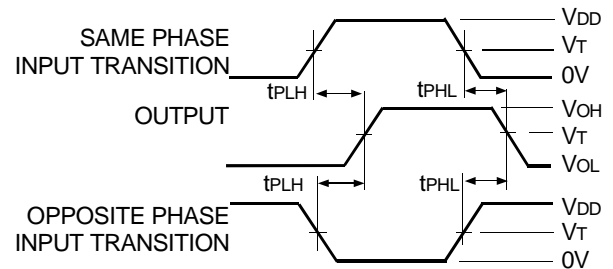
C_L = Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

NOTE:

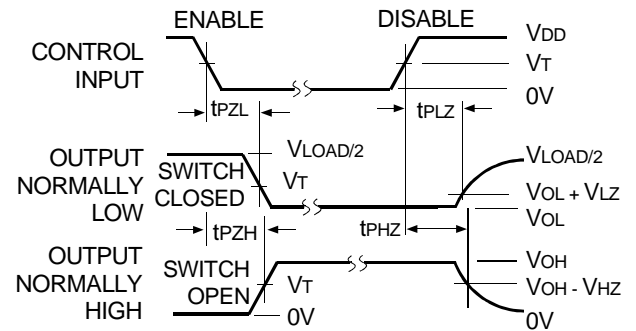
1. Pulse Generator for All Pulses: Rate ≤ 10MHz; Slew Rate ≥ 1V/ns.

SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	V _{LOAD}
Disable High Enable High	GND
All Other Tests	Open



Propagation Delay

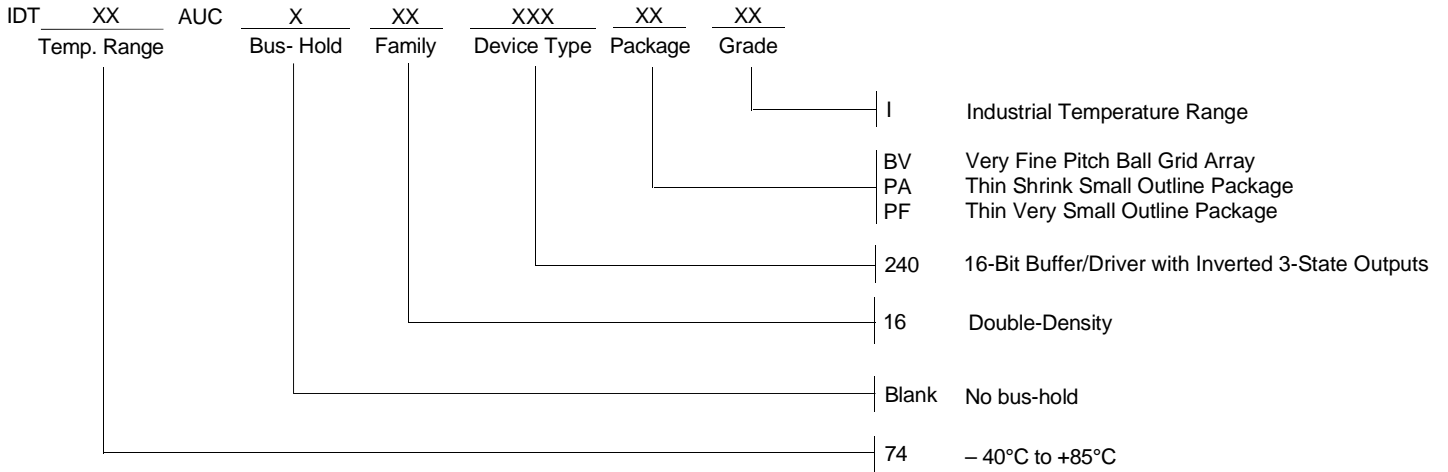


NOTE:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.

Enable and Disable Times

ORDERING INFORMATION



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