

# SCRs

JAN & JANTX 2N3027-2N3032

## 0.5 Amp, Planar



### FEATURES

- JAN and JANTX Types Available
- Fully Characterized for "Worst Case" Design
- Passivated Planar Construction for Maximum Reliability and Parameter Uniformity
- Low On-State Voltage and Fast Switching at High Current Levels
- Typical Turn-On Time: 0.12 $\mu$ s
- Typical Recovery Time: 0.1 $\mu$ s
- Pulse Currents: to 30A

### DESCRIPTION

The 2N3027 series of planar SCRs (controlled switches) are intended for use in military and space applications requiring a high degree of reliability. They offer a unique combination of extremely fast switching, precise triggering, high pulse power, small size, intrinsic parameter stability, and high radiation tolerance.

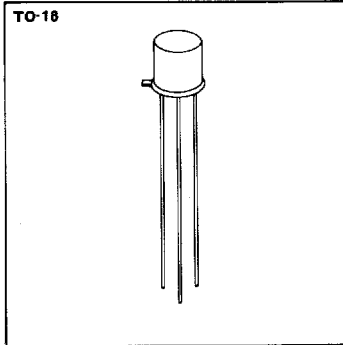
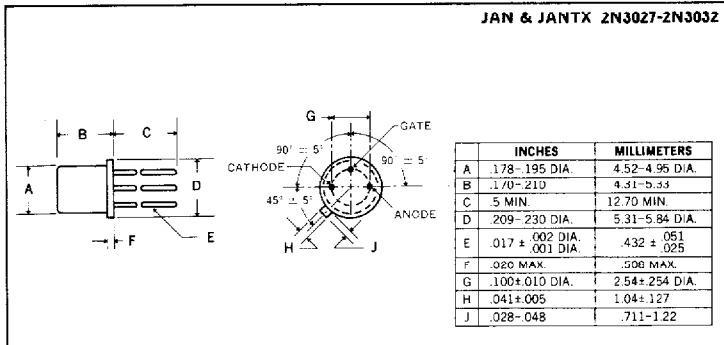
The JAN and JANTX types are specified under MIL-S-19500/419, and are included in MIL-STD-701 as recommended types for military usage.

### ABSOLUTE MAXIMUM RATINGS

	JAN & JANTX 2N3027 JAN & JANTX 2N3030	JAN & JANTX 2N3028 JAN & JANTX 2N3031	JAN & JANTX 2N3029 JAN & JANTX 2N3032
Repetitive Peak Off-State Voltage, $V_{DRM}$	30V	60V	100V
Repetitive Peak Reverse Voltage, $V_{RRM}$	30V	60V	100V
D.C. On-State Current, $I_T$			
100°C Case		500mA	
75°C Ambient		250mA	
Repetitive Peak On-State Current, $I_{T(RM)}$		30A	
Surge (Non-Rep.) On-State Current, $I_{TSM}$			
50ms		5A	
8ms		8A	
Peak Gate Current, $I_{GM}$		250mA	
Average Gate Current, $I_{G(AV)}$		25mA	
Reverse Gate Voltage		5V	
Reverse Gate Current		3mA	
Storage Temperature Range		-65°C to +200°C	
Operating Temperature Range		-65°C to +150°C	

Note: Blocking voltage ratings apply over the operating temperature range, provided the gate is connected to the cathode through an appropriate resistor, or adequate gate bias is used. (See section on bias stabilization.)

### MECHANICAL SPECIFICATIONS



**Microsemi Corp.**  
Watertown  
The diode experts

**ELECTRICAL SPECIFICATIONS (at 25°C unless noted) 2N3027 — 2N3028 — 2N3029**

Parameter	Symbol	Min.	Typical	Max.	Units	Test Conditions
SUBGROUP 1 Visual and Mechanical						MIL-STD-750 Method 2071
SUBGROUP 2 (25°C Tests)						
Off-State Current	$I_{DRM}$	—	.002	0.1	$\mu A$	$R_{GK} = 1K, V_{DRM} = \text{Rating}$
Reverse Current	$I_{RRM}$	—	.002	0.1	$\mu A$	$R_{GK} = 1K, V_{RRM} = \text{Rating}$
Reverse Gate Voltage	$V_{GR}$	5	8	—	V	$I_{GR} = 0.1mA$
Gate Trigger Current	$I_{GT}$	-5	8	200	$\mu A$	$R_{GS} = 10K, V_D = 5V$
Gate Trigger Voltage	$V_{GT}$	.40	.55	.80	V	$R_{GS} = 100\Omega, V_D = 5V$
On-State Voltage	$V_T$	0.8	1.2	1.5	V	$I_T = 1A$ (pulse test)
Holding Current	$I_H$	0.3	0.7	5.0	mA	$R_{GK} = 1K, V_D = 5V$
SUBGROUP 3 (25°C Tests)						
Off-State Voltage — Critical Rate of Rise	$dv_c/dt$	30 15	60 30	—	$V/\mu s$	$R_{GK} = 1K, V_D = 30V$ (2N3027) $R_{GK} = 1K, V_D = 60V$ (2N3028)
Gate Trigger-on Pulse Width	$t_{pg}(\text{on})$	10	25	—	$\mu s$	$R_{GK} = 1K, V_D = 100V$ (2N3029)
Delay Time	$t_d$	—	.07	0.2	$\mu s$	$I_G = 10mA, I_T = 1A, V_D = 30V$
Rise Time	$t_r$	—	.08	—	$\mu s$	$I_G = 10mA, I_T = 1A, V_D = 30V$
Circuit Commutated Turn-off Time	$t_g$	—	.04	—	$\mu s$	$I_G = 10mA, I_T = 1A, V_D = 30V$
SUBGROUP 4 (150°C Tests)						
High Temp. Off-State Current	$I_{DRM}$	—	2	20	$\mu A$	$R_{GK} = 1K, V_{DRM} = \text{Rating}$
High Temp. Reverse Current	$I_{RRM}$	—	20	50	$\mu A$	$R_{GK} = 1K, V_{RRM} = \text{Rating}$
High Temp. Gate Trigger Voltage	$V_{GT}$	.10	.15	0.6	V	$R_{GS} = 100\Omega, V_D = 5V$
High Temp. Holding Current	$I_H$	.05	.20	1.0	mA	$R_{GK} = 1K, V_D = 5V$
SUBGROUP 5 (-65°C Tests)						
Low Temp. Gate Trigger Voltage	$V_{GT}$	0.6	0.75	1.1	V	$R_{GS} = 100\Omega, V_D = 5V$
Low Temp. Gate Trigger Current	$I_{GT}$	0	150	1.2	mA	$R_{GS} = 10K, V_D = 5V$
Low Temp. Holding Current	$I_H$	0.5	3.5	10	mA	$R_{GK} = 1K, V_D = 5V$



**ELECTRICAL SPECIFICATIONS (at 25°C unless noted) 2N3030 — 2N3031 — 2N3032**

Parameter	Symbol	Min.	Typical	Max.	Units	Test Conditions
SUBGROUP 1 Visual and Mechanical						MIL-STD-750 Method 2071
SUBGROUP 2 (25°C Tests)						
Off-State Current	$I_{DRM}$	—	.002	0.1	$\mu A$	$R_{GK} = 1K, V_{DRM} = \text{Rating}$
Reverse Current	$I_{RRM}$	—	.002	0.1	$\mu A$	$R_{GK} = 1K, V_{RRM} = \text{Rating}$
Reverse Gate Voltage	$V_{GR}$	5	8	—	V	$I_{GR} = 0.1mA$
Gate Trigger Current	$I_{GT}$	-5	—	20	$\mu A$	$R_{GS} = 10K, V_D = 5V$
Gate Trigger Voltage	$V_{GT}$	0.44	—	0.6	V	$R_{GS} = 100\Omega, V_D = 5V$
On-State Voltage	$V_T$	0.8	1.2	1.5	V	$I_T = 1A$ (pulse test)
Holding Current	$I_H$	0.3	1.0	4.0	mA	$R_{GK} = 1K, V_D = 5V$
SUBGROUP 3 (25°C Tests)						
Off-State Voltage — Critical Rate of Rise	$dv_c/dt$	30 15	60 30	—	$V/\mu s$	$R_{GK} = 1K, V_D = 30V$ (2N3030) $R_{GK} = 1K, V_D = 60V$ (2N3031)
Gate Trigger-on Pulse Width	$t_{pg}(\text{on})$	10	25	—	$\mu s$	$R_{GK} = 1K, V_D = 100V$ (2N3032)
Delay Time	$t_d$	—	.05	0.1	$\mu s$	$I_G = 10mA, I_T = 1A, V_D = 30V$
Rise Time	$t_r$	—	.01	—	$\mu s$	$I_G = 10mA, I_T = 1A, V_D = 30V$
Circuit Commutated Turn-off Time	$t_g$	—	.05	—	$\mu s$	$I_G = 10mA, I_T = 1A, V_D = 30V$
SUBGROUP 4 (150°C Tests)						
High Temp. Off-State Current	$I_{DRM}$	—	2	20	$\mu A$	$R_{GK} = 1K, V_{DRM} = \text{Rating}$
High Temp. Reverse Current	$I_{RRM}$	—	20	50	$\mu A$	$R_{GK} = 1K, V_{RRM} = \text{Rating}$
High Temp. Gate Trigger Voltage	$V_{GT}$	.10	.15	0.4	V	$R_{GS} = 100\Omega, V_D = 5V$
High Temp. Holding Current	$I_H$	.05	.30	2.0	mA	$R_{GK} = 1K, V_D = 5V$
SUBGROUP 5 (-65°C Tests)						
Low Temp. Gate Trigger Voltage	$V_{GT}$	0.44	0.8	0.95	V	$R_{GS} = 100\Omega, V_D = 5V$
Low Temp. Gate Trigger Current	$I_{GT}$	0	0.4	0.5	mA	$R_{GS} = 10K, V_D = 5V$
Low Temp. Holding Current	$I_H$	0.5	5.0	8	mA	$R_{GK} = 1K, V_D = 5V$

**High Reliability Processing**

The 2N3027-2N3032 series provides a complete range of high reliability processing from the standard devices that undergo extensive electrical testing, through JAN and JANTX levels. 100% processing, Group B, and Group C tests for JAN and JANTX devices is shown below. For further details, see MIL-S-19500/419(EL).

**100% Screening TX Types**

- High Temperature Storage
- Temperature Cycling
- Constant Acceleration
- Fine & Gross Hermetic Seal
- Electrical Test
- Burn-in
- Electrical Test

**Group B Tests**

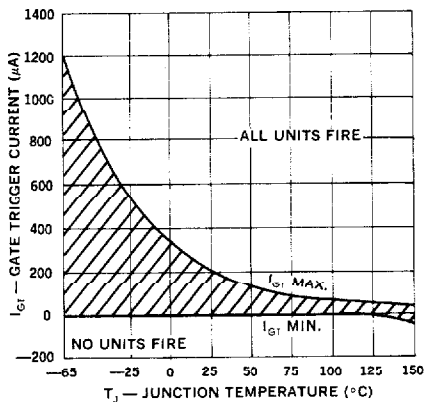
- Subgroup 1 — Physical Dimensions
- Subgroup 2 — Solderability
  - Temperature Cycling
  - Thermal Shock
  - Constant Acceleration
  - Moisture Resistance
- Subgroup 3 — Surge Current
- Subgroup 4 — Blocking Life Test
- Subgroup 5 — Storage Life Test
- Subgroup 6 — Operating Life Test

**Group C Tests**

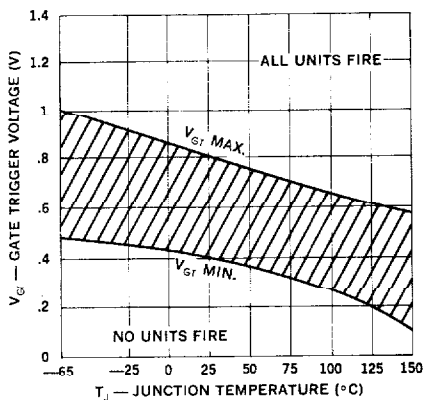
- Subgroup 1 — Shock
  - Vibration, Variable Frequency
- Subgroup 2 — Salt Atmosphere
- Subgroup 3 — Terminal Strength
- Subgroup 4 — High Temp. Anode Voltage — Critical rate or rise
- Subgroup 5 — Storage Life Test
- Subgroup 6 — Operating Life Test

**TYPICAL CHARACTERISTICS**  
2N3027 — 2N3028 — 2N3029

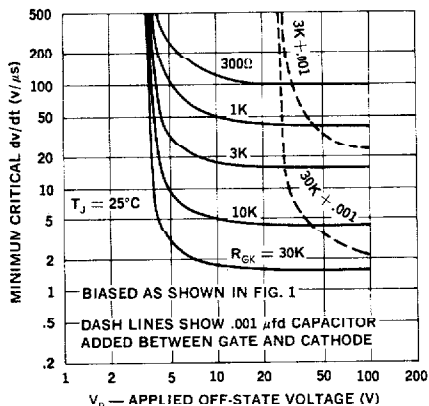
**1 Gate Trigger Current**



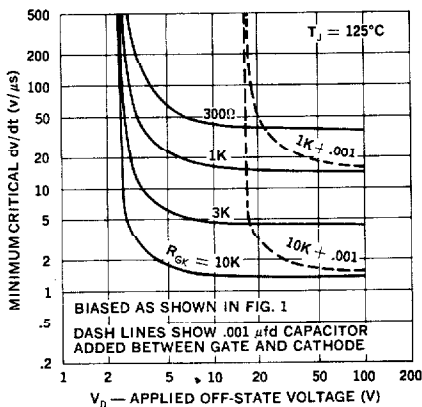
**2 Gate Trigger Voltage**



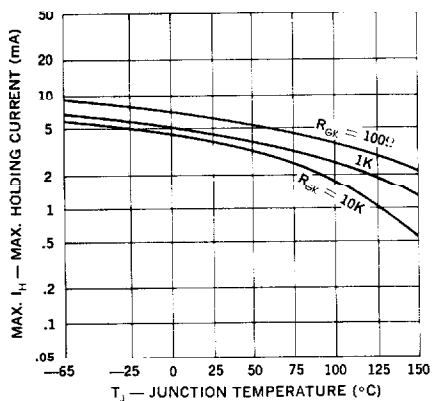
**3 Min. Critical dv/dt (25°C — R Bias)**



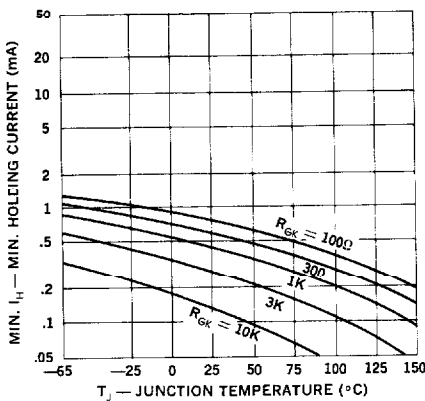
**4 Min. Critical dv/dt (125°C — R Bias)**



**5 Max. Holding Current (Resistor Bias)**

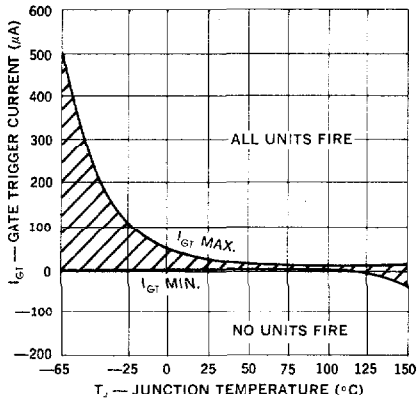


**6 Min. Holding Current (Resistor Bias)**

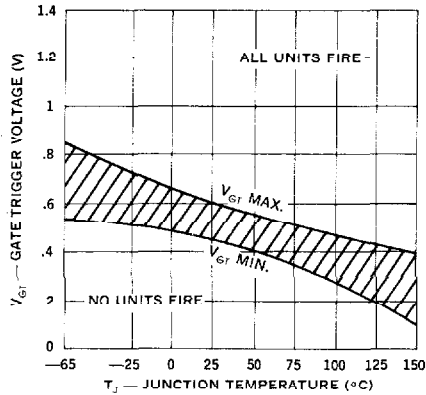


**TYPICAL CHARACTERISTICS**  
2N3030 — 2N3031 — 2N3032

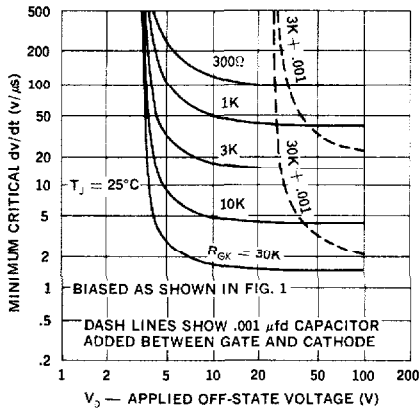
**1 Gate Trigger Current**



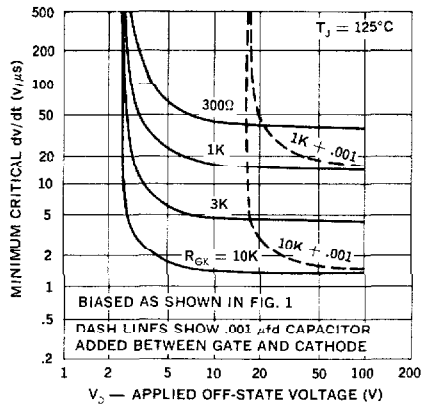
**2 Gate Trigger Voltage**



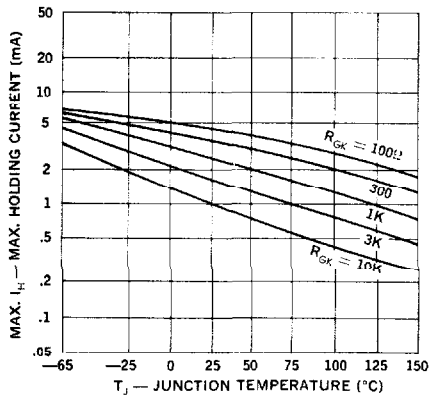
**3 Min. Critical dv/dt (25°C — R Bias)**



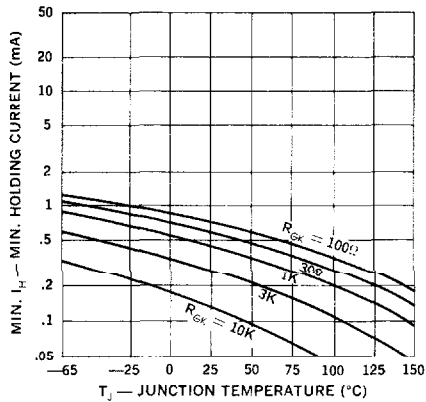
**4 Min. Critical dv/dt (125°C — R Bias)**



**5 Max. Holding Current (Resistor Bias)**

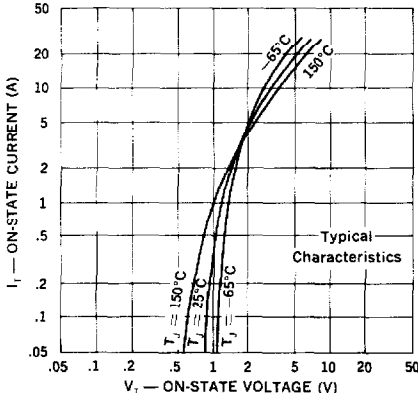


**6 Min. Holding Current (Resistor Bias)**

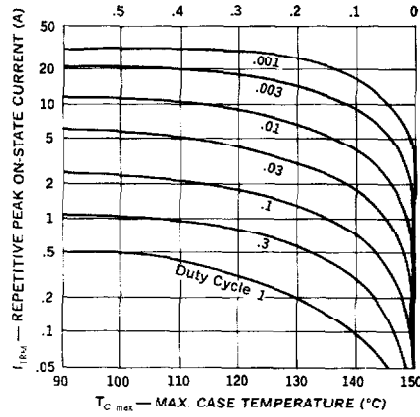


**CURRENT RATINGS**

**C1 Forward on Current vs. Voltage**

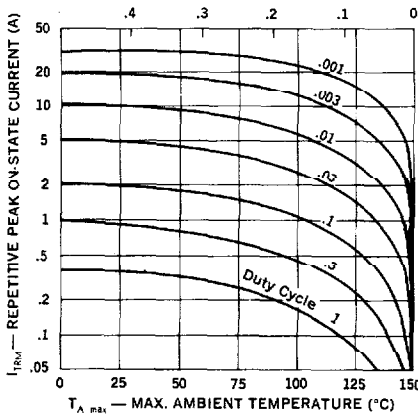


**C2 Peak Current vs. Case Temperature**  
 $P_A$  — POWER DISSIPATION (W)

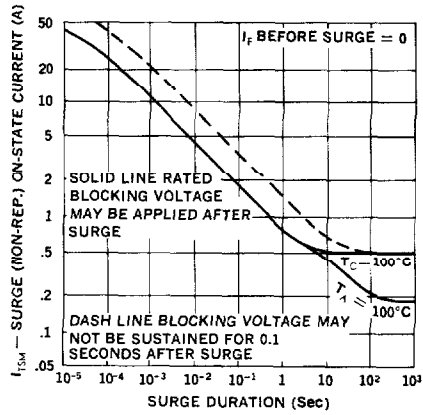


**C3 Peak Current vs. Ambient Temperature**  
**TO-18 Ratings (see note)**

$P_A$  — POWER DISSIPATION (W)

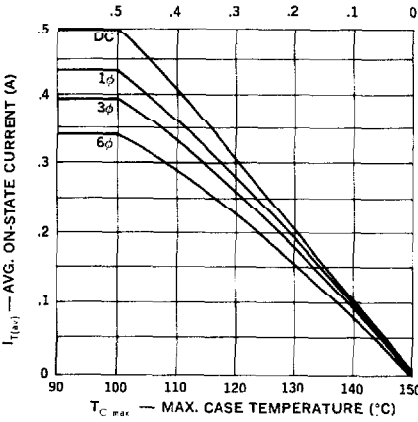


**C4 Surge Current vs. Time**



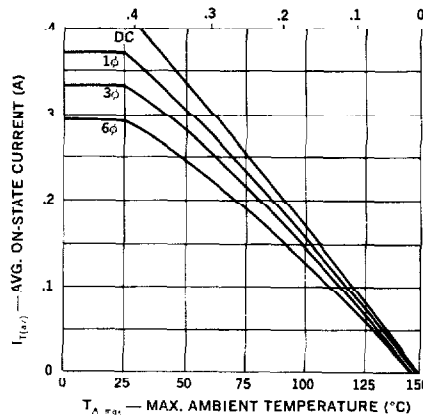
**C5 Average Current vs. Case Temperature**

$P_A$  — POWER DISSIPATION (W)



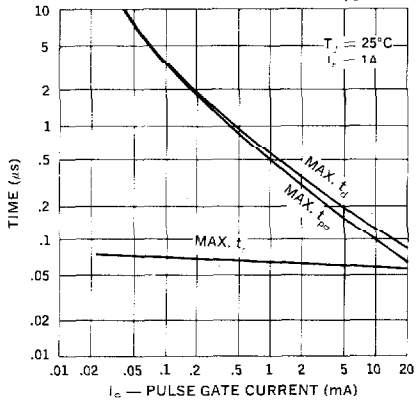
**C6 Average Current vs. Ambient Temperature**  
**TO-18 Ratings (see note)**

$P_A$  — POWER DISSIPATION (W)

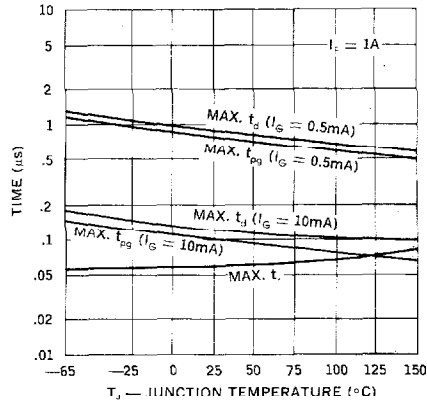


SWITCHING SPEEDS

S1 Maximum Delay Time  $t_d$ , Rise Time  $t_r$ , and Gate Trigger Pulse Width  $t_{pg}$  (on)

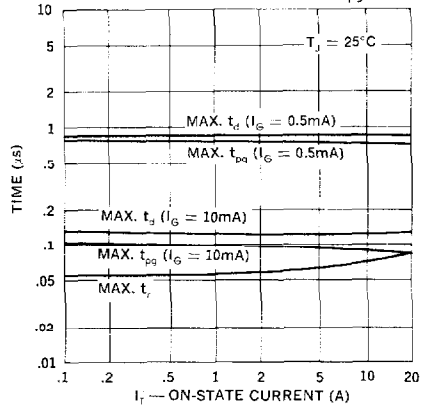


S2 Maximum Delay Time  $t_d$ , Rise Time  $t_r$ , and Gate Trigger Pulse Width  $t_{pg}$  (on)

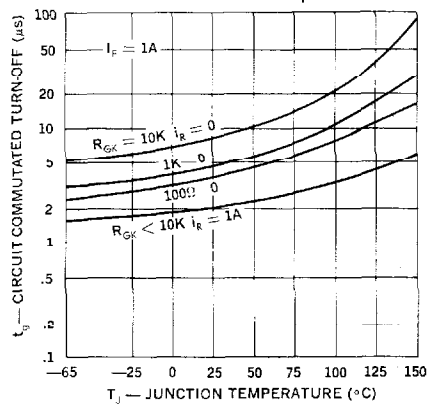


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S3 Maximum Delay Time  $t_d$ , Rise Time  $t_r$ , and Gate Trigger Pulse Width  $t_{pg}$  (on)



S4 Maximum Circuit Commutated Turn-off Time  $t_q$



S5 Maximum Circuit Commutated Turn-off Time  $t_q$

