ANALOG DEVICES

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APPLICATION NOTE

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EMC-Compliant RS-485 Communication Networks

by James Scanlon

INTRODUCTION

In real industrial and instrumentation (I&I) applications, RS-485 communication links must work in harsh electromagnetic environments. Large transient voltages caused by lightning strikes, electrostatic discharge, and other electromagnetic phenomenon can cause damage to communication ports. These data ports must meet certain electromagnetic compatibility (EMC) regulations to ensure that they can survive in their final installation environments.

Within these requirements, there are three transient immunity standards: electrostatic discharge, electrical fast transients, and surge. Leaving EMC considerations to the end of the design cycle leads to penalties, such as engineering budget and schedule overruns. Many EMC problems are not simple or obvious and must be considered at the start of product design.

This application note describes each of these transients, presents the design solution methodology, and demonstrates three different EMC-compliant solutions for three different cost/protection levels for RS-485 communication ports. These different solutions are illustrated in Figure 1.

Analog Devices, Inc., and Bourns, Inc., have partnered to extend their offering of system oriented solutions by co-developing the industry's first EMC-compliant RS-485 interface customer design tool.

This tool provides, up to and including, Level 4 protection levels for IEC 61000-4-2 ESD, IEC 61000-4-4 EFT, and IEC 61000-4-5 surge. It gives designers the design options depending upon the level of protection required and available budgets. These design tools allow designers to reduce risk of project slippage due to EMC problems by considering them at the start of the design cycle.

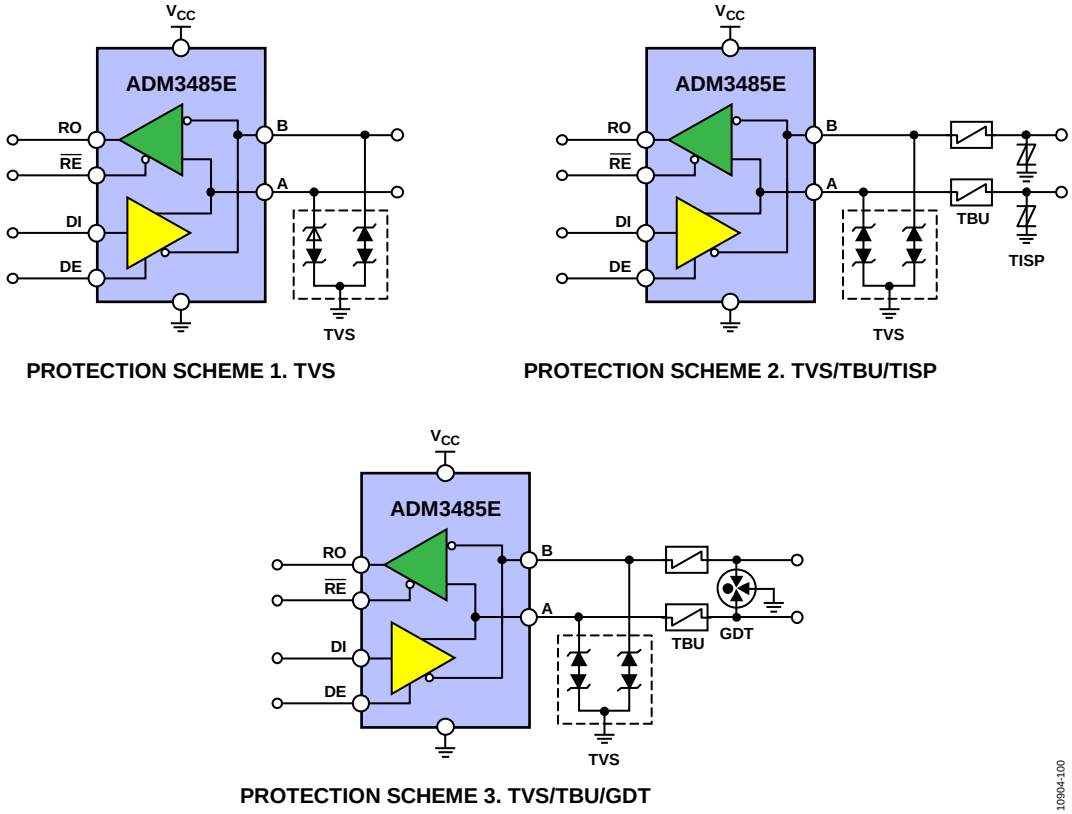

Figure 1. Three EMC Compliant Solutions

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REVISION HISTORY

2/13—Revision 0: Initial Version

RS-485 STANDARD

I&I applications require the transmission of data between multiple systems, often over very long distances. The RS-485 bus standard is one of the most widely used physical layer bus designs in I&I applications. Applications for RS-485 include process control networks; industrial automation; remote terminals; building automation, such as heating, ventilation, and air conditioning (HVAC); security systems; motor control; and motion control.

The key features of RS-485 that make it ideal for use in I&I communications applications are

- Long distance links—up to 4000 feet.
- Bidirectional communications possible over a single pair of twisted cables.
- Differential transmission increases noise immunity and decreases noise emissions.
- Multiple drivers and receivers can be connected on the same bus.
- Wide common-mode range (−7 V to +12 V) allows for differences in ground potential between the driver and receiver.
- TIA/EIA-485-A allow for data rates of tens of Mbps.

TIA/EIA-485-A, the telecommunication industry's most widely used transmission line standard, describes the physical layer of the RS-485 interface and is normally used with a higher level protocol, such as Profibus, Interbus, Modbus, or BACnet. This allows for robust data transmission over relatively long distances.

In real applications, however, lightning strikes, power induction and direct contact, power source fluctuations, inductive switching, and electrostatic discharge can cause damage to RS-485 transceivers by generating large transient voltages. Designers must ensure that equipment does not just work in ideal conditions, but that it must also work in real world situations. In order to ensure that these designs can survive in electrically harsh environments, various government agencies and regulatory bodies have imposed EMC regulations. Compliance with these regulations assures the end user that designs will operate as desired in these harsh electromagnetic environments.

ELECTROMAGNETIC COMPATIBILITY

EMC is the ability of an electronic system to function satisfactorily in its intended electromagnetic environment without introducing intolerable electromagnetic disturbances to that environment. An electromagnetic environment is composed of both radiated and conducted energy. Therefore, EMC has two aspects, emission and susceptibility.

Emission is the unwanted generation of electromagnetic energy by a product. It is often desirable to control emission in order to create an electromagnetically-compatible environment.

Susceptibility is a measure of the ability of electronic products to tolerate the influence of electromagnetic energy radiated or conducted from other electronic products or electromagnetic influences. Immunity is the opposite of susceptibility. Equipment that has high susceptibility has low immunity.

The international electrotechnical commission (IEC) is the world's leading organization that prepares and publishes international standards for all electrical, electronic, and related technologies. Since 1996, all electronic equipment sold to or within the European community must meet EMC levels as defined in specification IEC 61000-4-x.

The IEC 61000 specifications define the set of EMC immunity requirements that apply to electrical and electronic equipment intended for use in residential, commercial, and light industrial environments. Within this set of specifications, there are three types of high voltage transients that electronic designers need to be concerned about for data communication lines. These are

- IEC 61000-4-2 Electrostatic Discharge (ESD)
- IEC 61000-4-4 Electrical Fast Transients (EFT)
- IEC 61000-4-5 Surge Immunity

This application note deals with increasing the protection level of RS-485 ports to protect against the these three main EMC transients.

Each of these specifications defines a test method to assess the immunity of electronic and electrical equipment against the defined phenomenon. The following sections provide a summary of each of these tests.

ELECTROSTATIC DISCHARGE

ESD is the sudden transfer of electrostatic charge between bodies at different potentials caused by near contact or induced by an electric field. It has the characteristics of high current in a short time period.

An object can become charged due to a number of mechanisms. A charge can occur by simple contact with another charged object. It can also occur as a result of triboelectric charging, which is the generation of static electricity caused by rubbing two substances together. Alternatively, an object can be charged as a result of induction charging. In this case, there is no physical contact with the charged object yet charging can occur if it is within the electric field of the charged object.

The primary purpose of the IEC 61000-4-2 test is to determine the immunity of systems to external ESD events outside the system during operation. IEC 61000-4-2 specifies testing using two coupling methods, contact discharge and air-gap discharge. Contact discharge implies the discharge gun is placed in direct connection with the unit under tested. Air gap discharge uses a higher test voltage, but does not make direct contact with the unit under test.

During air discharge testing, the charged electrode of the discharge gun is moved toward the unit under test until a discharge occurs as an arc across the air gap. The discharge gun does not make direct contact with the unit under test. A number of factors affect the results and repeatability of the air discharge test, including humidity, temperature, barometric pressure, distance, and rate of approach to the unit under test. This method is a better representation of an actual ESD event, but is not as repeatable. Therefore, contact discharge is the preferred test method.

IEC 61000-4-2 specifies voltage test levels for different environmental conditions along with a current waveform. Table 1 shows the relationship between the environment and the test voltage. The test levels should be selected in accordance with the most realistic installation and environment conditions the final product will be subjected to.

Level 1 is the least severe and Level 4 the most severe. Level 1 and Level 2 are for products installed in controlled environments that have antistatic material. Level 3 and Level 4 are for products installed in more severe environments where ESD events with higher voltages are more common.

Figure 2 shows the 8 kV contact discharge current waveform as described in the specification. Some of the key waveform parameters to note are fast rise times of less than 1 ns and short pulse widths of approximately 60 ns. This equates to a pulse with total energy in the range of tens of mJ.

The test is performed with single discharges. The test point is subjected to at least 10 positive and 10 negative discharges. A 1 s interval between discharges is recommended.

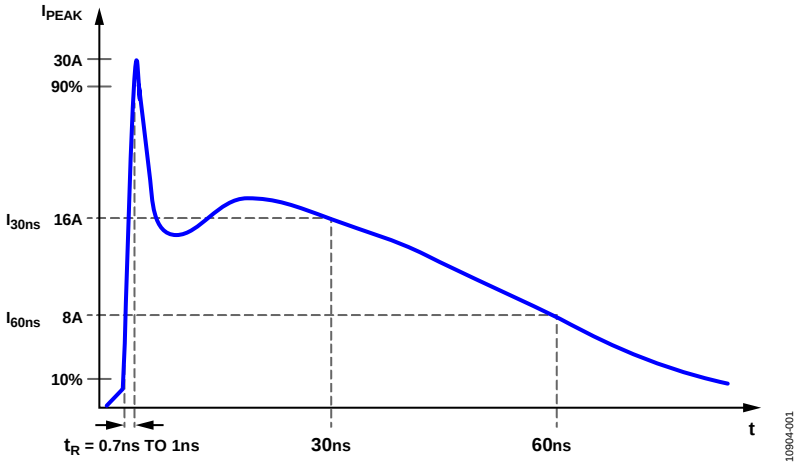

Figure 2. IEC 61000-4-2 ESD Waveform (8 kV)

Table 1. IEC 61000-4-2 Test Levels and Installation Classes

Level/Class	Relative Humidity As Low as %	Antistatic Material	Synthetic Material	Contact Discharge Test Voltage (kV)	Air Discharge Test Voltage (kV)
1	35	X		2	2
2	10	X		4	4
3	50		X	6	8
4	10		X	8	15

ELECTRICAL FAST TRANSIENTS

Electrical fast transient testing involves coupling a number of extremely fast transient impulses onto the signal lines to represent transient disturbances associated with external switching circuits that are capacitively coupled onto the communication ports. This may include relay and switch contact bounce or transients originating from the switching of inductive or capacitive loads—all of which are common in industrial environments. The EFT test defined in IEC 61000-4-4 attempts to simulate the interference resulting from these types of events.

Figure 3 shows the EFT 50 Ω load waveform. The EFT waveform is described in terms of a voltage across 50 Ω impedance from a generator with 50 Ω output impedance. The output waveform consists of a 15 ms burst 5 kHz high voltage transients repeated at 300 ms intervals. Each individual pulse has a rise time of 5 ns and pulse duration of 50 ns, measured between the 50% point on the rising and falling edges of the waveform. Similar to the ESD transient, the EFT pulse has the characteristics of fast rise time and short pulse width. The total energy in a single pulse is similar to that of an ESD pulse. Voltages applied to the data ports can be as high as 2 kV.

These fast burst transients are coupled onto the communication lines using a capacitive clamp. The EFT is capacitively coupled onto the communication lines by the clamp rather than direct contact. This also reduces the loading caused by the low output impedance of the EFT generator. The coupling capacitance between the clamp and cable depends on cable diameter, shielding, and insulation on the cable.

IEC 61000-4-4 specifies voltage test levels for different environmental conditions. Table 2 shows the test voltage and pulse repetition rates for the different test levels. The test levels should be selected according to the most realistic installation and environmental conditions the final product will be subjected to. Traditionally, 5 kHz repetition rates are used, however this rate is generally dependent on the end manufacturers specification.

- Level 1 well protected
- Level 2 protected environments
- Level 3 typical industrial environment
- Level 4 severe industrial environment

Table 2. IEC 61000-4-4 Test Levels

	Data Port Test Voltages and Repetition Rates	
Level	Voltage Peak (kV)	Repetition Rate (kHz)
1	0.25	5 or 100
2	0.5	5 or 100
3	1	5 or 100
4	2	5 or 100

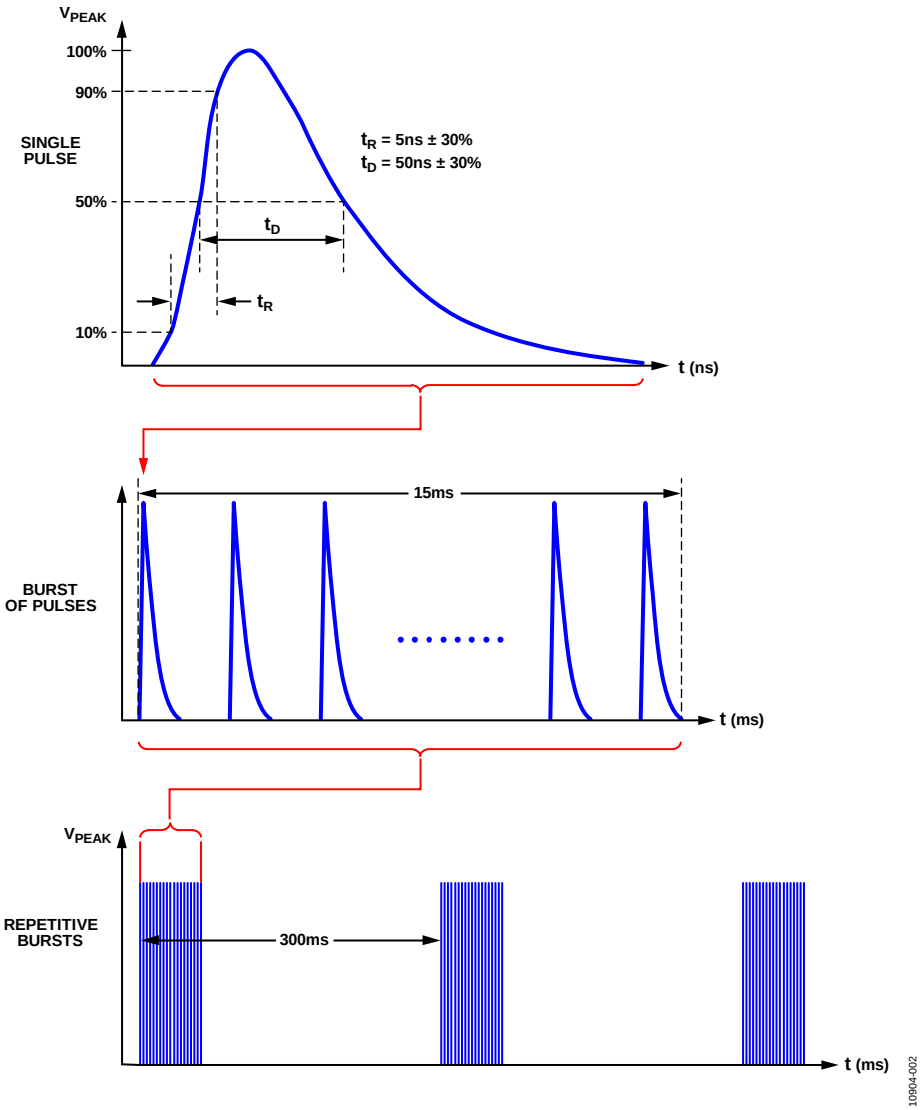

Figure 3. IEC 61000-4-4 EFT 50 Ω Waveform

SURGE

Surge transients are caused by overvoltages from switching or lightning transients. Switching transients can result from power system switching, load changes in power distribution systems, or various system faults, such as short circuits and arching faults to the grounding system of the installation. Lightning transients can be a result of high currents and voltages injected into the circuit from nearby lightning strikes. IEC 61000-4-5 defines waveforms, test methods, and test levels for evaluating the immunity of electrical and electronic equipment when subjected to these surges.

The waveforms are specified as the outputs of a waveform generator in terms of open-circuit voltage and short-circuit current. Two waveforms are described. The 10 µs/700 µs combination waveform is used to test ports intended for connection to symmetrical communication lines, for example telephone exchange lines. The 1.2 µs/50 µs combination waveform generator is used in all other cases, in particular short distance signal connections. For RS-485 ports, the 1.2 µs/50 µs waveform is predominantly used. The waveform generator has an effective output impedance of 2 Ω, thus the surge transient has high currents associated with it.

Figure 4 shows the 1.2 µs /50 µs surge transient waveform. ESD and EFT have similar rise times, pulse widths, and energy levels. With surge, the rise time of the pulse is 1.25 µs and the pulse width is 50 µs. The surge pulse energy can have energy levels that are three to four orders of magnitude larger than the energy in an ESD or EFT pulse. Therefore, the surge transient is considered the most severe of the EMC transient specs. Due to the similarities between ESD and EFT, the design of the circuit protection can be similar, however, due to its high energy, surge must be dealt with differently. This is one of the main issues in developing protection circuitry that improves the immunity of data ports to all three transients while remaining cost effective.

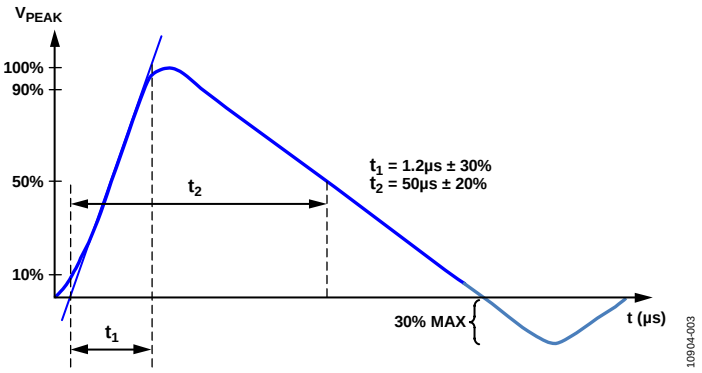

Figure 4. IEC 61000-4-5 Surge 1.2 µs/50 µs Waveform

Resistors couple the surge transient onto the communication line. Figure 5 shows the coupling network for a half-duplex RS-485 device. The total parallel sum of the resistance is 40 Ω. For the half-duplex device, each resistor is 80 Ω.

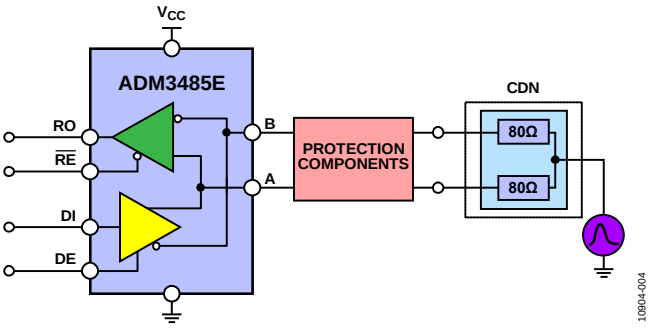

Figure 5. Surge Coupling Network for a Half-Duplex RS-485 Device

Table 3. IEC 61000-4-5 Test Levels

Level	Open-Circuit Test Voltage
1	0.5 kV
2	1 kV
3	2 kV
4	4 kV
X	Special

The test levels as defined in the IEC 61000-4-5 are shown in Table 3. Level X can be above, below, or in between the other levels. This is usually specified in the product standard. The test levels should be selected according to the installation conditions. There are six classes of installations defined in the specification.

- Class 0 (well protected electrical environment)
- Class 1 (partially protected electrical environment)
- Class 2 (electrical environment where cables are well separated, even at short runs)
- Class 3 (electrical environment where power and signal cables run in parallel)
- Class 4 (electrical environment where the interconnections are running as outdoor cables along with power cables, and cables are used for both electronic and electrical circuits)
- Class 5 (electrical environment for electronic equipment connected to telecommunication cables and overhead power lines in a nondensely populated environment)
- Class X (special conditions specified in the product specifications)

Class 0 has no surge transient treat associated with it. Class 5 has the most severe transient stress level.

A summary of the installation classes and the surge voltage for each class is shown in Table 4. Table 4 shows the test voltages associated with each class for line to ground coupling for symmetric and unsymmetrical lines. It is important that the final environment class is known to ensure the product is immune to the threat level.

Table 4. IEC 61000-4-5 Installation Classes

Installation Class	Unsymetrical Lines Test levels	Symetrical Lines Test Levels
0	NA	NA
1	0.5 kV	0.5 kV
2	1 kV	1 kV
3	2 kV	2 kV
4	4 kV	2 kV
5	4 kV	4 kV

During the surge test, five positive, and five negative pulses are applied to the data ports with a maximum time interval of 1 minute between each pulse. The standard states that the device should be set up in normal operating conditions for the duration of the test.

PASS/FAIL CRITERIA

When transients are applied to the system under test, the results are categorized into four pass/fail criteria. Following is a list of the pass/fail criteria giving examples how each might relate to an RS-485 transceiver:

A. Normal performance; no bit errors would occur during or after the transient is applied.
B. Temporary loss of function or temporary degradation of performance not requiring an operator; bit errors might occur during and for a limited time after the transient is applied.
C. Temporary loss of function or temporary degradation of performance requiring an operator; a latch-up event may occur that could be removed after a power on reset with no permanent or degradation to the device.
D. Loss of function with permanent damage to equipment. The device fails the test.

Criteria A is the most desirable and Criteria D is unacceptable. Permanent damage results in system downtime and the expense of repair and replacement. For mission critical systems, Criteria B and Criteria C are also unacceptable because the system must operate without errors during transient events.

THEORY OF PROTECTION

There are three main ways to prevent EMC problems.

- Suppress the transient at source.
- Make the coupling path as inefficient as possible.
- Make the device less susceptible to the transient.

Often it is not possible to remove the source of the transient, for example, it is not possible to control where lightning strikes occur. Reducing the possibility of coupling is often beyond the manufacturers control when the final product is installed. In order to ensure the product is EMC compatible, it is often necessary for the manufacturer to add protection to the data ports to make the product less susceptible to these transients.

When designing protection circuitry to protect against transients, consider the following:

- It must prevent or limit damage caused by the transient and allow the system to return to normal operation with minimal impact on performance.
- The protection scheme should be robust enough to deal with the type of transients and voltage levels the system would be subjected to in the field.
- The length of time associated with the transient is an important factor. For long transients, heating effects can cause certain protection schemes to fail.
- Under normal operation conditions, the protection circuitry should not interfere with the system operation.
- If the protection circuitry fails during overstress, it should fail in a way that protects the system.

There are two main types of protection schemes used to protect against transients. Overcurrent protection is used to limit peak current and overvoltage protection is used to limit peak voltages. There is a broad range of overcurrent and overvoltage protection technologies and components available in the market, each one with its own advantages and disadvantages. Developing protection for a system usually requires the use of both overvoltage and overcurrent protection devices.

Figure 6 shows a typical design for a protection scheme. The design can be characterized by having primary and secondary protection. Primary protection diverts most of the transient energy away from the system and is typically located at the interface between the system and the environment. It is designed to remove the majority of the energy by diverting the transient to ground.

The function of the secondary protection is to protect various parts of the system from any transient voltages and currents let through by the primary protection. The secondary protection is usually designed to be more specific to the part of the system it is protecting. It is optimized to ensure that it protects against these residual transients while allowing normal operation of these sensitive parts of the system. It is essential that both the primary and secondary designs are specified to work together in conjunction with the system input/output to minimize the stress on the protected circuit.

These designs typically include a coordinating element, such as a resistance or a nonlinear overcurrent protection device, between the primary and secondary protection devices to ensure that coordination occurs.

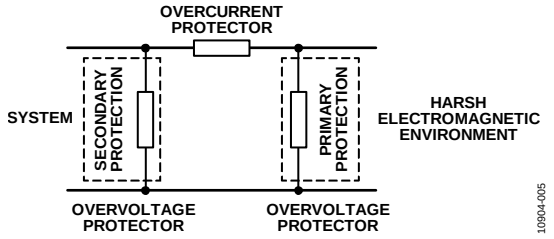

Figure 6. Protection Scheme—Block Diagram

RS-485 TRANSIENT SUPPRESSION NETWORKS

EMC transient events vary in time, so the dynamic performance and the matching of the dynamic characteristics of the protection components with the input/output stage of the protected device leads to successful EMC design. Component data sheets generally only contain dc data, which is of limited value given that the dynamic breakdowns and I/V characteristics can be quite different from the dc values. Careful design, characterization, and an understanding of the dynamic performance of the input/output stage of the protected device and the protection components is required to ensure that the circuit meets EMC standards.

This application note presents three different fully characterized EMC-compliant solutions. Each solution was certified by an independent external EMC compliance test house, and each provides different cost/protection levels for the Analog Devices ADM3485E 3.3 V RS-485 transceiver with enhanced ESD protection using a selection of Bourns external circuit protection components. The Bourns external circuit protection components used consist of transient voltage suppressors (CDSOT23-SM712), transient blocking units (TBU-CA065-200-WH), thyristor surge protectors (TISP4240M3BJR-S), and gas discharge tubes (2038-15-SM-RPLF).

Each solution was characterized to ensure the dynamic I/V performance of the protection components protect the dynamic I/V characteristics of the ADM3485E RS-485 bus pins. It is the interaction between the input/output stage of the ADM3485E and the external protection components that function together to protect against the transient events.

PROTECTION SCHEME 1

The EFT and ESD transient have similar energy levels, while the surge waveform has energy levels three to four magnitudes greater. Protecting against ESD and EFT is accomplished in a similar manner, but protecting against high levels of surge requires solutions that are more complex. The first solution described protects up to Level 4 ESD and EFT and Level 2 surge. The 1.2 µs/50 µs waveform is used in all surge testing described in this application note.

This solution uses the Bourns CDSOT23-SM712 transient voltage suppressor (TVS) array which consists of two bidirectional TVS diodes as illustrated in Figure 7. Table 5 shows the voltage levels protected against for ESD, EFT, and surge transients.

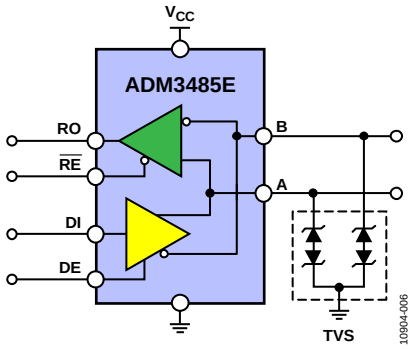

Figure 7. Protection Scheme 1—TVS

Table 5. Scheme 1 Protection Levels

ESD (-4-2)		EFT (-4-4)		Surge (-4-5)	
Level	**Voltage (Contact/Air)**	**Level**	**Voltage**	**Level**	**Voltage**
4	8 kV/15 kV	4	2 kV	2	1 kV

A TVS is a silicon-based device. Under normal operating conditions, the TVS has high impedance to ground; ideally, it is an open circuit. The protection is accomplished by clamping the overvoltage from a transient to a voltage limit. This is done by the low impedance avalanche breakdown of a PN junction. When a transient voltage larger than the breakdown voltage of the TVS is generated, the TVS clamps the transient to a predetermined level that is less than the breakdown voltage of the devices that it is protecting. The transients are clamped instantaneously (< 1 ns) and the transient current is diverted away from the protected device to ground.

It is important to ensure that the breakdown voltage of the TVS is outside the normal operating range of the pins protected. As demonstrated in Figure 8, the unique feature of the CDSOT23-SM712 is that it has asymmetrical breakdown voltages of +13.3 V and −7.5 V to match the transceiver common-mode range of +12 V to −7 V, therefore providing optimum protection while minimizing overvoltage stresses on the ADM3485E RS-485 transceiver.

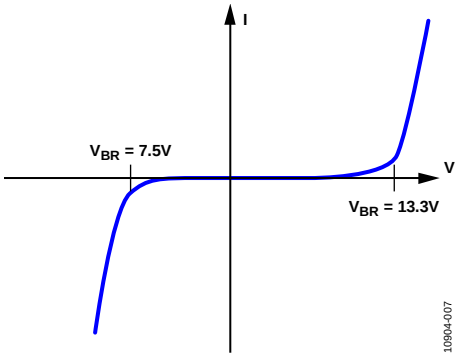

Figure 8. CDSOT23-SM712 I/V Characteristic

PROTECTION SCHEME 2

The previous solution protects up to Level 4 ESD and EFT, but only to Level 2 surge. To improve the surge protection level, the protection circuitry gets more complex. The protection solution presented in this section protects up to Level 4 surge.

The CDSOT23-SM712 is specifically designed for RS-485 data ports. The next two solutions build on the CDSOT23-SM712 to provide higher levels of circuit protection. In this solution, the CDSOT23-SM712 provides secondary protection while the TISP4240M3BJR-S provides the primary protection.

Coordination between the primary and secondary protection devices, and overcurrent protection is accomplished using the TBU-CA065-200-WH. Table 6 shows the voltage levels protected against for ESD, EFT, and surge transients with this solution. Figure 9 shows a representation of the complete solution.

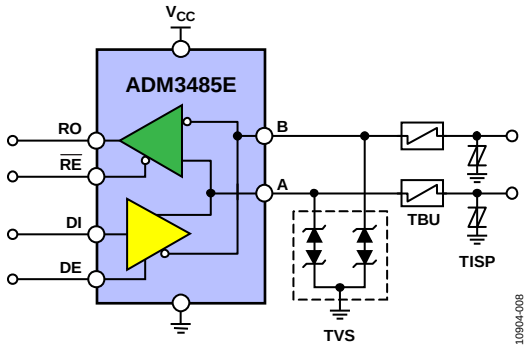

Figure 9. Protection Scheme 2—TVS/TBU/TISP

Table 6. Scheme 2 Protection Levels

ESD (-4-2)		EFT (-4-4)		Surge (-4-5)	
Level	**Voltage (Contact/Air)**	**Level**	**Voltage**	**Level**	**Voltage**
4	8 kV/15 kV	4	2 kV	4	4 kV

When a transient is applied to the protection circuit, the TVS breaks down providing a low impedance path to ground to protect the device. With large voltages and currents, there is a need to protect the TVS and limit the current through it. This is done using a transient blocking unit (TBU), which is an active high speed overcurrent protection element. The TBU in this design is the Bourns TBU-CA065-200-WH.

A TBU blocks current rather than shunting it to ground. As a series component, it reacts to current through the device rather than the voltage across the interface. A TBU is a high speed overcurrent protection component with a preset current limit and a high voltage withstand capability. When an overcurrent occurs and the TVS breaks down due to the transient event, the current in the TBU will rise to the current limiting level set by the device. At this point, the TBU disconnects the protected circuitry from the surge in less than 1 µs.

During the remainder of the transient, the TBU remains in the protected blocking state, with very low current (<1 mA) passing through the protected circuit. Under normal operating conditions, the TBU exhibits low impedance, so it has minimal impact on normal circuit operation. In blocking mode, it has very high impedance to block transient energy. After the transient event, the TBU automatically resets to its low impedance state and reinstates the system allowing resumption of normal operation.

Like all overcurrent protection technologies, the TBU has a maximum breakdown voltage, so a primary protection device must clamp the voltage and redirect the transient energy to ground. This is commonly done using technologies, such as gas discharge tubes or solid-state thyristors, such as the totally integrated surge protector (TISP). The TISP acts as a primary protection device. When its predefined protection voltage is exceeded, it provides a crowbar low impedance path to ground, thus diverting the majority of the transient energy away from the system and other protection devices.

The nonlinear voltage-current characteristic of the TISP limits overvoltage by diverting the resultant current. As a thyristor, a TISP has a discontinuous voltage-current characteristic caused by the switching action between high and low voltage regions. Figure 10 shows the voltage-current characteristic of the device. Before the TISP device switches into a low voltage state, with low impedance to ground to shunt the transient energy, a clamping action is caused by the avalanche breakdown region.

In limiting an overvoltage, the protected circuitry will be exposed to a high voltage for the brief time period that the TISP device is in the breakdown region, before it switches into a low voltage protected on-state. The TBU will protect the downstream circuitry from high currents resulting from this high voltage. When the diverted current falls below a critical value, the TISP device automatically resets allowing normal system operation to resume.

As described, all three components work together in conjunction with the system input/output to protect the system from high voltage and current transients.

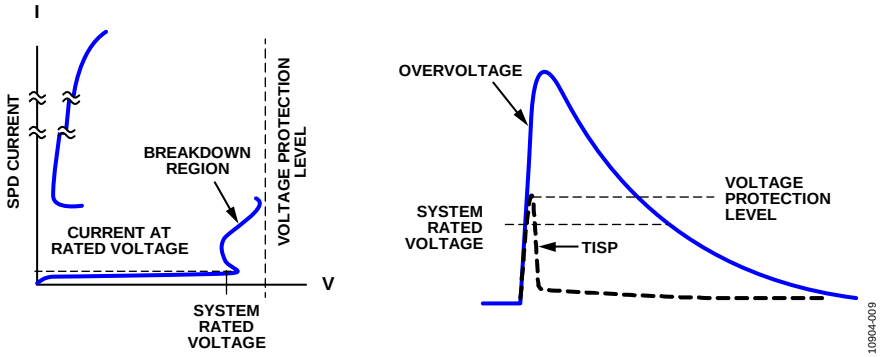

Figure 10. TISP Switching Characteristic and Voltage Limiting Waveshape

PROTECTION SCHEME 3

Protection levels above Level 4 surge are often required. The protection scheme shown in Figure 11 protects RS-485 ports up to and including 6 kV surge transients. It operates in a similar fashion to Protection Scheme 2; however, in this circuit, a gas discharge tube (GDT) is used in place of the TISP to protect the TBU, which is, in turn, protecting the TVS, the secondary protection device. The GDT will provide protection to higher overvoltage and overcurrent stress than the TISP described in the Protection Scheme 2 section. The GDT for this protection scheme is the Bourns 2038-15-SM-RPLF. The TISP is rated at 220 A vs. the GDT rating of 5 kA per conductor. Table 7 summarizes the protection levels provided by this design.

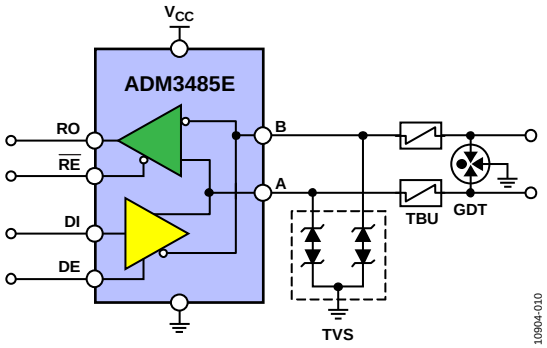

Figure 11. Protection Scheme 3—TVS/TBU/GDT

Table 7. Scheme 3 Protection Levels

ESD (-4-2)		EFT (-4-4)		Surge (-4-5)	
Level	**Voltage (Contact/Air)**	**Level**	**Voltage**	**Level**	**Voltage**
4	8 kV/15 kV	4	2 kV	X	6 kV

Predominately used as a primary protection device, a GDT provides a low impedance path to ground to protect against overvoltage transients. When a transient voltage reaches the GDT spark-over voltage, the GDT switches from a high impedance off-state to arc mode. In arc mode, the GDT becomes a virtual short, providing a crowbar current path to ground and diverting the transient current away from the protected device.

Figure 12 shows the typical characteristics of a GDT. When the voltage across a GDT increases, the gas in the tube starts to ionize due to the charge developed across it. This is known as the glow region. In this region, the increased current flow creates an avalanche effect that transitions the GDT into a virtual short circuit, allowing current to pass through the device. During the short-circuit event, the voltage developed across the device is known as the arc voltage. The transition time between the glow and arc region is highly dependent on the physical characteristics of the device.

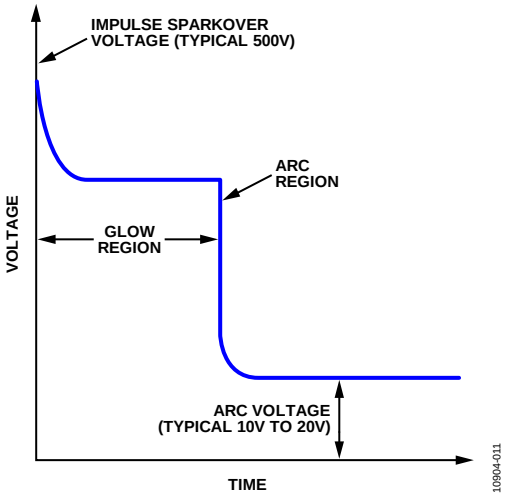

Figure 12. GDT Characteristic Waveform

CONCLUSION

This application note describes the three IEC standards of interest that deal with transient immunity. In real industrial applications, RS-485 communication ports subjected to these transients can be damaged. EMC problems discovered late in a product design cycle may require expensive redesign and can often lead to schedule overruns. EMC problems should therefore be considered at the start of the design cycle and not at a later stage where it may be too late to achieve the desired EMC performance.

The key challenge in designing EMC-compliant solutions for RS-485 networks is matching the dynamic performance of the external protection components with the dynamic performance of the input/output structure of the RS-485 device.

This application note demonstrated three different EMC compliant solutions for RS-485 communication ports, giving the designer options depending on the level of protection required. The EVAL-CN0313-SDPZ is industry's first EMC-compliant RS-485 customer design tool, providing up to Level 4 protection levels for ESD, EFT, and surge. The protection levels offered by the different protection schemes are summarized in Table 7.

While these design tools do not replace the due diligence or qualification required at the system level, they allow the designer to reduce the risk of project slippage due to EMC problems at the start of the design cycle, thus reducing design time and time to market. For more information, visit: www.analog.com/RS485emc.

Table 4. Three ADM3485E EMC-Compliant Schemes

	ESD (-4-2)		EFT(-4-4)		Surge (-4-5)	
Protection Scheme	**Level**	**Voltage (Contact/Air)**	**Level**	**Voltage**	**Level**	**Voltage**
1. TVS	4	8 kV/15 kV	4	2 kV	2	1 kV
2. TVS/TBU/TISP	4	8 kV/15 kV	4	2 kV	4	4 kV
3. TVS/TBU/GDT	4	8 kV/15 kV	4	2 kV	X	6 kV

REFERENCES

More information regarding interface and isolation products is listed in this section (also see the Analog Devices website).

See the Bourns website for information on parts mentioned in this document as well as for the First Principles document and the Bournes Telecom Protection Guide.

ADM3485E Data Sheet. Analog Devices, Inc.

Electromagnetic Compatibility (EMC) Part 4-2: Testing and Measurement Techniques—Electrostatic Discharge Immunity Test (IEC 61000-4-2:2008 (Ed.2.0)).

Electromagnetic Compatibility (EMC) Part 4-4: Testing and Measurement Techniques—Electrical Fast Transient/Burst Immunity Test (IEC 61000-4-4:2012 (Ed3.0)).

Electromagnetic Compatibility (EMC) Part 4-5: Testing and Measurement Techniques—Surge Immunity Test (IEC 61000-4-5:2005 (Ed2.0)).

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Marais, Hein. "RS-485/RS-422 Circuit Implementation Guide." Application Note AN-960. Analog Devices, Inc.

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