International IƆR Rectifier

IRLR3717
IRLU3717

HEXFET® Power MOSFET

| V_{DSS}	$R_{DS(on)}$ max	Qg
20V	**4.0mΩ**	**21nC**

Applications

- High Frequency Synchronous Buck Converters for Computer Processor Power
- High Frequency Isolated DC-DC Converters with Synchronous Rectification for Telecom and Industrial Use

Benefits

- Very Low $R_{DS(on)}$ at 4.5V V_{GS}
- Ultra-Low Gate Impedance
- Fully Characterized Avalanche Voltage and Current

D-Pak	I-Pak
IRLR3717	IRLU3717
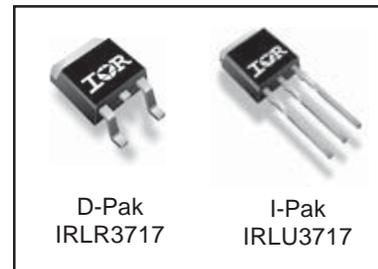
Absolute Maximum Ratings

	Parameter	Max.	Units
V_{DS}	Drain-to-Source Voltage	20	V
V_{GS}	Gate-to-Source Voltage	± 20	
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V	120④	A
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ 10V	81④	
I_{DM}	Pulsed Drain Current ①	460	
P_D @T_C = 25°C	Maximum Power Dissipation	89	W
P_D @T_C = 100°C	Maximum Power Dissipation	44	
	Linear Derating Factor	0.59	W/°C
T_J	Operating Junction and	-55 to + 175	°C
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	——	1.69	°C/W
$R_{\theta JA}$	Junction-to-Ambient (PCB Mount) ⑤	——	50	
$R_{\theta JA}$	Junction-to-Ambient	——	110	

Notes ① through ⑤ are on page 11

Static @ T$_J$ = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
BV$_{DSS}$	Drain-to-Source Breakdown Voltage	20	—	—	V	V$_{GS}$ = 0V, I$_D$ = 250µA
ΔBV$_{DSS}$/ΔT$_J$	Breakdown Voltage Temp. Coefficient	—	12	—	mV/°C	Reference to 25°C, I$_D$ = 1mA
R$_{DS(on)}$	Static Drain-to-Source On-Resistance	—	3.4	4.0	mΩ	V$_{GS}$ = 10V, I$_D$ = 15A ③
		—	4.6	5.5		V$_{GS}$ = 4.5V, I$_D$ = 12A ③
V$_{GS(th)}$	Gate Threshold Voltage	1.55	2.0	2.45	V	V$_{DS}$ = V$_{GS}$, I$_D$ = 250µA
ΔV$_{GS(th)}$/ΔT$_J$	Gate Threshold Voltage Coefficient	—	-6.4	—	mV/°C	
I$_{DSS}$	Drain-to-Source Leakage Current	—	—	1.0	µA	V$_{DS}$ = 16V, V$_{GS}$ = 0V
		—	—	150		V$_{DS}$ = 16V, V$_{GS}$ = 0V, T$_J$ = 125°C
I$_{GSS}$	Gate-to-Source Forward Leakage	—	—	100	nA	V$_{GS}$ = 20V
	Gate-to-Source Reverse Leakage	—	—	-100		V$_{GS}$ = -20V
gfs	Forward Transconductance	49	—	—	S	V$_{DS}$ = 10V, I$_D$ = 12A
Q$_g$	Total Gate Charge	—	21	31		
Q$_{gs1}$	Pre-Vth Gate-to-Source Charge	—	6.4	—		V$_{DS}$ = 10V
Q$_{gs2}$	Post-Vth Gate-to-Source Charge	—	1.9	—	nC	V$_{GS}$ = 4.5V
Q$_{gd}$	Gate-to-Drain Charge	—	7.2	—		I$_D$ = 12A
Q$_{godr}$	Gate Charge Overdrive	—	5.5	—		See Fig. 16
Q$_{sw}$	Switch Charge (Q$_{gs2}$ + Q$_{gd}$)	—	9.1	—		
Q$_{oss}$	Output Charge	—	13	—	nC	V$_{DS}$ = 10V, V$_{GS}$ = 0V
t$_{d(on)}$	Turn-On Delay Time	—	14	—		V$_{DD}$ = 10V, V$_{GS}$ = 4.5V ③
t$_r$	Rise Time	—	14	—	ns	I$_D$ = 12A
t$_{d(off)}$	Turn-Off Delay Time	—	5.8	—		Clamped Inductive Load
t$_f$	Fall Time	—	16	—		
C$_{iss}$	Input Capacitance	—	2830	—		V$_{GS}$ = 0V
C$_{oss}$	Output Capacitance	—	920	—	pF	V$_{DS}$ = 10V
C$_{rss}$	Reverse Transfer Capacitance	—	420	—		f = 1.0MHz

Avalanche Characteristics

	Parameter	Typ.	Max.	Units
E$_{AS}$	Single Pulse Avalanche Energy②	—	460	mJ
I$_{AR}$	Avalanche Current ①	—	12	A
E$_{AR}$	Repetitive Avalanche Energy ①	—	8.9	mJ

Diode Characteristics

|	Parameter	Min.	Typ.	Max.	Units	Conditions
I$_S$	Continuous Source Current (Body Diode)	—	—	120④	A	MOSFET symbol showing the integral reverse p-n junction diode.
I$_{SM}$	Pulsed Source Current (Body Diode) ①	—	—	460		
V$_{SD}$	Diode Forward Voltage	—	—	1.0	V	T$_J$ = 25°C, I$_S$ = 12A, V$_{GS}$ = 0V ③
t$_{rr}$	Reverse Recovery Time	—	22	33	ns	T$_J$ = 25°C, I$_F$ = 12A, V$_{DD}$ = 10V
Q$_{rr}$	Reverse Recovery Charge	—	13	19	nC	di/dt = 100A/µs ③
t$_{on}$	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				
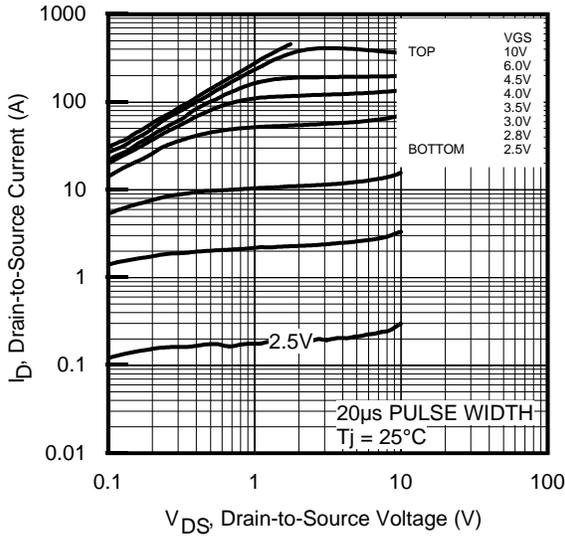
Fig 1. Typical Output Characteristics
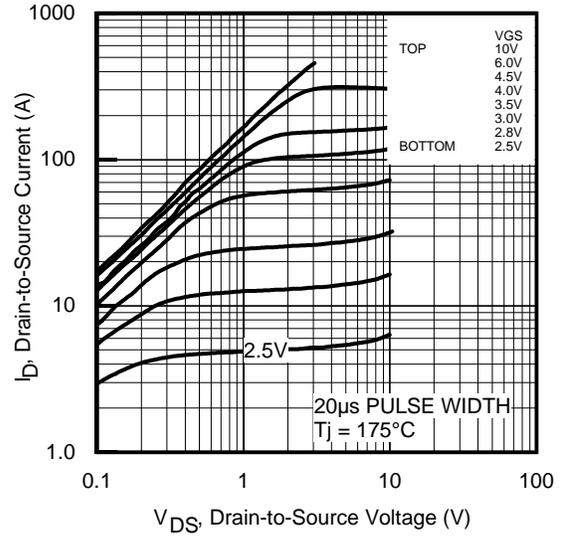
Fig 2. Typical Output Characteristics
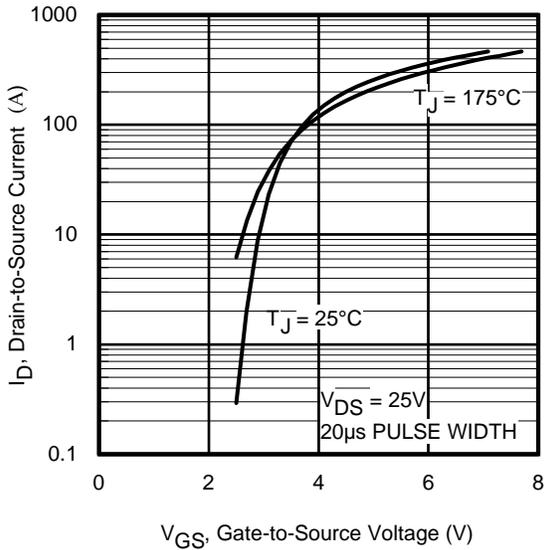

Fig 3. Typical Transfer Characteristics
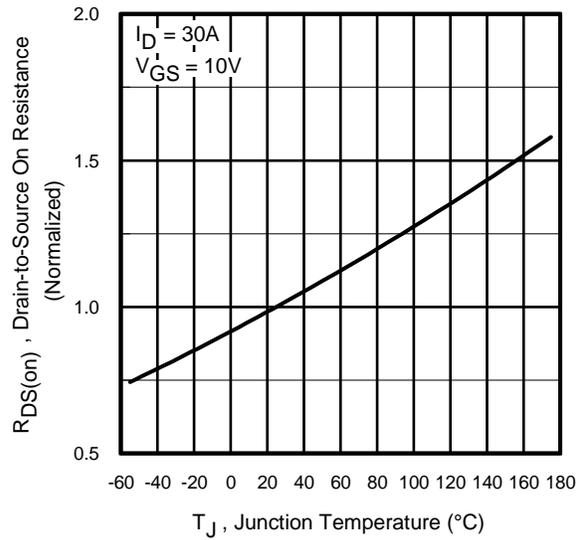
Fig 4. Normalized On-Resistance
vs. Temperature

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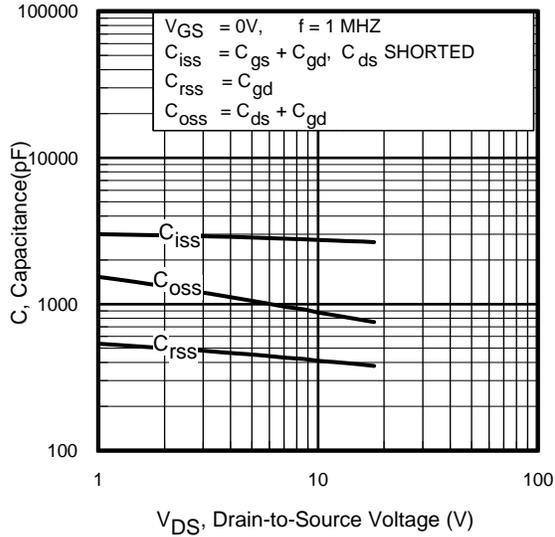
Fig 5. Typical Capacitance vs.
Drain-to-Source Voltage

$V_{GS} = 0V$, f = 1 MHZ
$C_{iss} = C_{gs} + C_{gd}$, C_{ds} SHORTED
$C_{rss} = C_{gd}$
$C_{oss} = C_{ds} + C_{gd}$

C_{iss}
C_{oss}
C_{rss}

C, Capacitance(pF)
V_{DS}, Drain-to-Source Voltage (V)
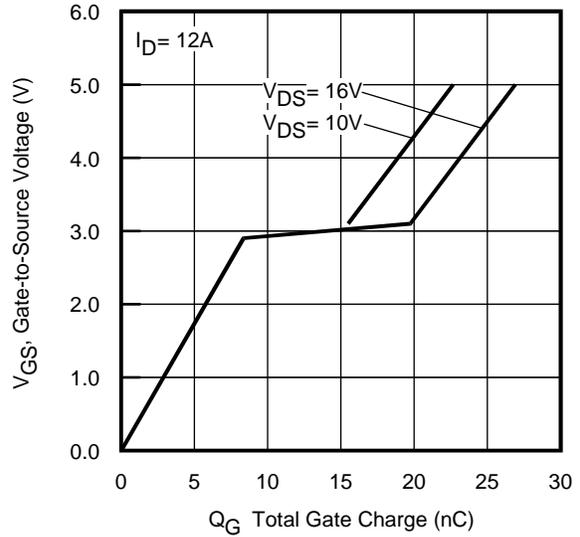
Fig 6. Typical Gate Charge vs.
Gate-to-Source Voltage

$I_D = 12A$
$V_{DS} = 16V$
$V_{DS} = 10V$

V_{GS}, Gate-to-Source Voltage (V)
Q_G Total Gate Charge (nC)
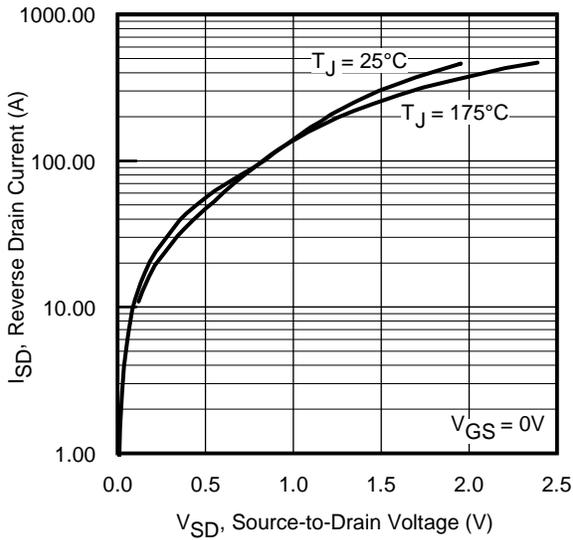
Fig 7. Typical Source-Drain Diode
Forward Voltage

$T_J = 25°C$
$T_J = 175°C$
$V_{GS} = 0V$

I_{SD}, Reverse Drain Current (A)
V_{SD}, Source-to-Drain Voltage (V)
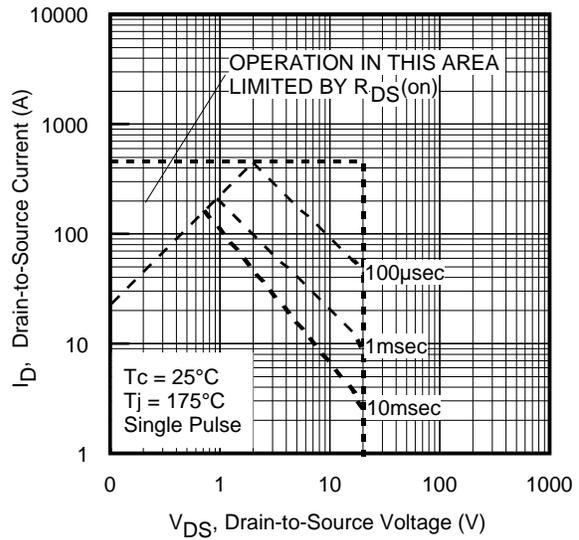
Fig 8. Maximum Safe Operating Area

OPERATION IN THIS AREA
LIMITED BY R_{DS}(on)
100µsec
1msec
10msec
Tc = 25°C
Tj = 175°C
Single Pulse

I_D, Drain-to-Source Current (A)
V_{DS}, Drain-to-Source Voltage (V)

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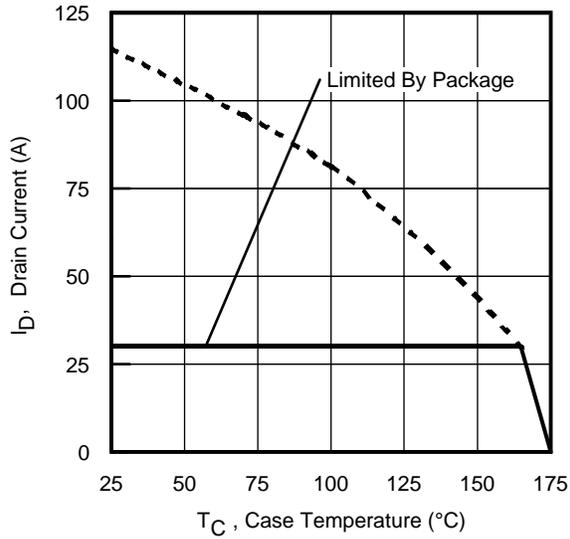
IRLR3717/IRLU3717

Fig 9. Maximum Drain Current vs. Case Temperature
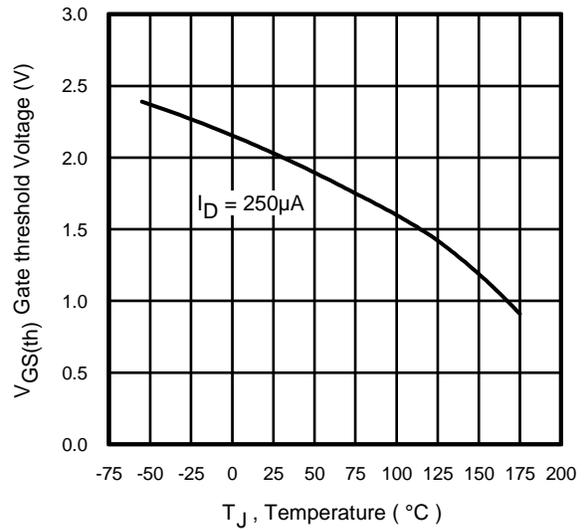
Fig 10. Threshold Voltage vs. Temperature

Ri (°C/W)	τi (sec)
0.771	0.000430
0.629	0.006491
0.291	0.072119

Notes:
1. Duty Factor D = t1/t2
2. Peak Tj = P dm x Zthjc + Tc
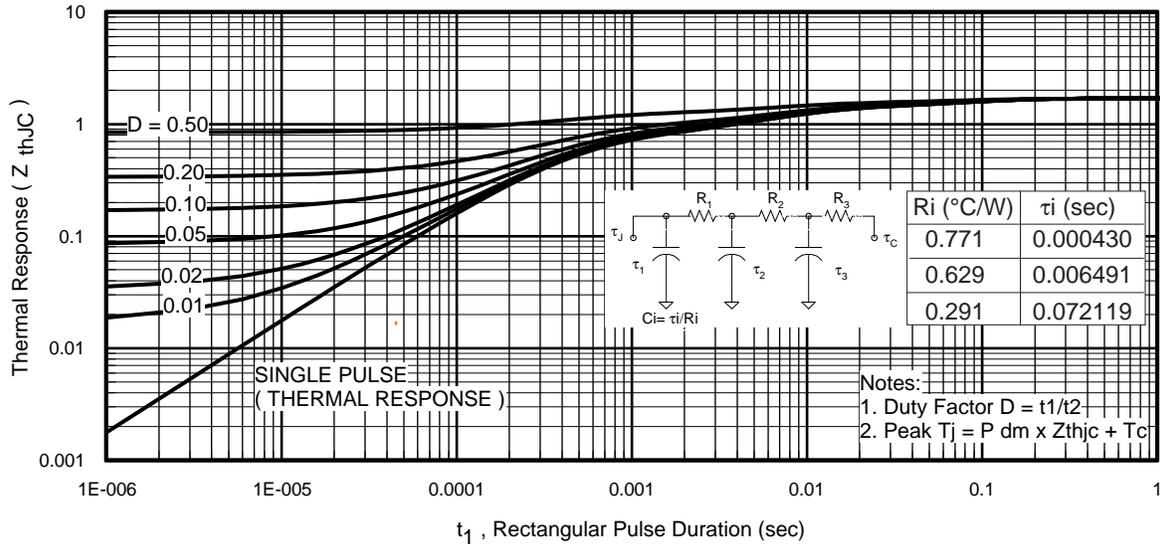
Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

IRLR3717/IRLU3717
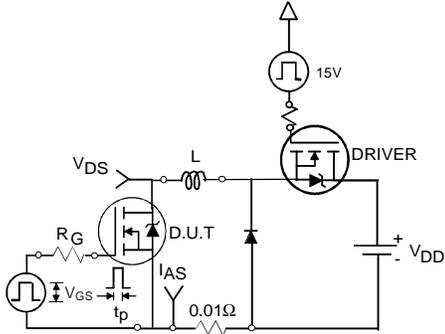
Fig 12a. Unclamped Inductive Test Circuit
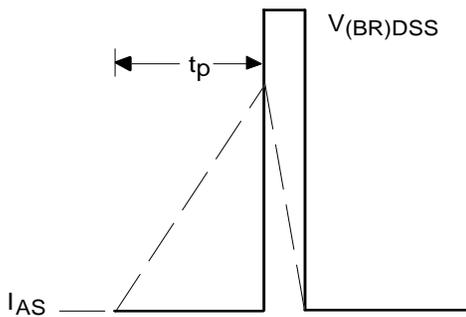
Fig 12b. Unclamped Inductive Waveforms

	I_D
TOP	8.2A
	9.7A
BOTTOM	12A

Fig 12c. Maximum Avalanche Energy vs. Drain Current

Fig 13. Gate Charge Test Circuit
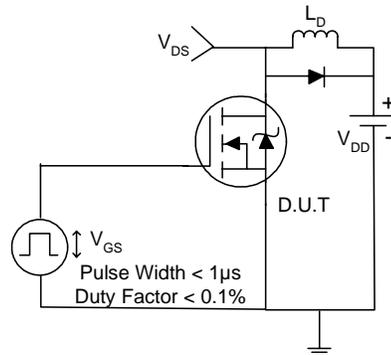
Fig 14a. Switching Time Test Circuit
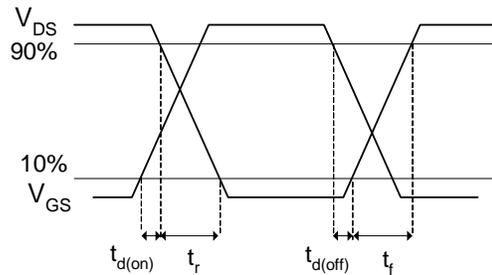
Fig 14b. Switching Time Waveforms

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IRLR3717/IRLU3717

D.U.T

Circuit Layout Considerations
- Low Stray Inductance
- Ground Plane
- Low Leakage Inductance Current Transformer

R_G

V_{DD}

- dv/dt controlled by R_G
- Driver same type as D.U.T.
- I_{SD} controlled by Duty Factor "D"
- D.U.T. - Device Under Test

① Driver Gate Drive

P.W. | Period | $D = \dfrac{P.W.}{Period}$

$V_{GS}=10V$ *

② D.U.T. I_{SD} Waveform

Reverse Recovery Current

Body Diode Forward Current

di/dt

③ D.U.T. V_{DS} Waveform

Diode Recovery dv/dt

V_{DD}

Re-Applied Voltage

Body Diode Forward Drop

④ Inductor Curent

Ripple ≤ 5%

I_{SD}

* V_{GS} = 5V for Logic Level Devices

Fig 15. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs

Id

Vds

Vgs

Vgs(th)

Qgs1 Qgs2 Qgd Qgodr
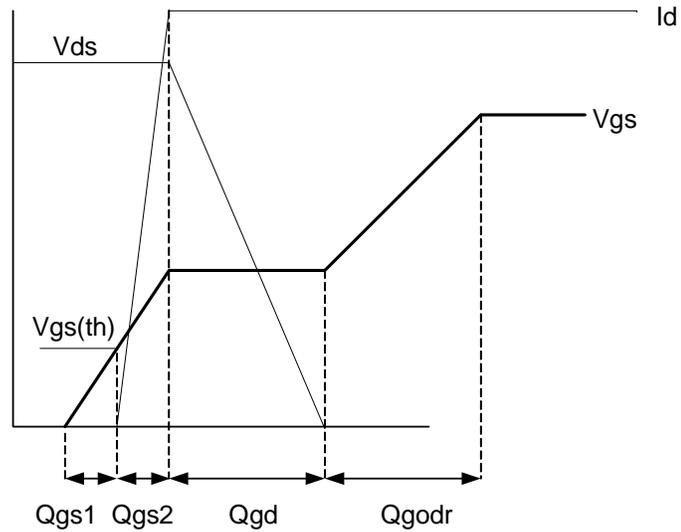
Fig 16. Gate Charge Waveform

IRLR3717/IRLU3717

Power MOSFET Selection for Non-Isolated DC/DC Converters

Control FET

Special attention has been given to the power losses in the switching elements of the circuit - Q1 and Q2. Power losses in the high side switch Q1, also called the Control FET, are impacted by the $R_{ds(on)}$ of the MOSFET, but these conduction losses are only about one half of the total losses.

Power losses in the control switch Q1 are given by;

$$P_{loss} = P_{conduction} + P_{switching} + P_{drive} + P_{output}$$

This can be expanded and approximated by;

$$P_{loss} = \left(I_{rms}^{\ 2} \times R_{ds(on)} \right)$$
$$+ \left(I \times \frac{Q_{gd}}{i_g} \times V_{in} \times f \right) + \left(I \times \frac{Q_{gs2}}{i_g} \times V_{in} \times f \right)$$
$$+ \left(Q_g \times V_g \times f \right)$$
$$+ \left(\frac{Q_{oss}}{2} \times V_{in} \times f \right)$$

This simplified loss equation includes the terms Q_{gs2} and Q_{oss} which are new to Power MOSFET data sheets.

Q_{gs2} is a sub element of traditional gate-source charge that is included in all MOSFET data sheets. The importance of splitting this gate-source charge into two sub elements, Q_{gs1} and Q_{gs2}, can be seen from Fig 16.

Q_{gs2} indicates the charge that must be supplied by the gate driver between the time that the threshold voltage has been reached and the time the drain current rises to I_{dmax} at which time the drain voltage begins to change. Minimizing Q_{gs2} is a critical factor in reducing switching losses in Q1.

Q_{oss} is the charge that must be supplied to the output capacitance of the MOSFET during every switching cycle. Figure A shows how Q_{oss} is formed by the parallel combination of the voltage dependant (non-linear) capacitance's C_{ds} and C_{dg} when multiplied by the power supply input buss voltage.

Synchronous FET

The power loss equation for Q2 is approximated by;

$$P_{loss} = P_{conduction} + P_{drive} + P_{output}^*$$
$$P_{loss} = \left(I_{rms}^{\ 2} \times R_{ds(on)} \right)$$
$$+ \left(Q_g \times V_g \times f \right)$$
$$+ \left(\frac{Q_{oss}}{2} \times V_{in} \times f \right) + \left(Q_{rr} \times V_{in} \times f \right)$$

*dissipated primarily in Q1.

For the synchronous MOSFET Q2, $R_{ds(on)}$ is an important characteristic; however, once again the importance of gate charge must not be overlooked since it impacts three critical areas. Under light load the MOSFET must still be turned on and off by the control IC so the gate drive losses become much more significant. Secondly, the output charge Q_{oss} and reverse recovery charge Q_{rr} both generate losses that are transfered to Q1 and increase the dissipation in that device. Thirdly, gate charge will impact the MOSFETs' susceptibility to Cdv/dt turn on.

The drain of Q2 is connected to the switching node of the converter and therefore sees transitions between ground and V_{in}. As Q1 turns on and off there is a rate of change of drain voltage dV/dt which is capacitively coupled to the gate of Q2 and can induce a voltage spike on the gate that is sufficient to turn the MOSFET on, resulting in shoot-through current . The ratio of Q_{gd}/Q_{gs1} must be minimized to reduce the potential for Cdv/dt turn on.
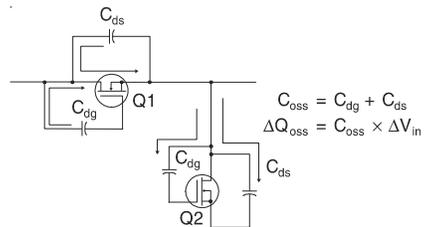

Figure A: Q_{oss} Characteristic

International
IΩR Rectifier

D-Pak (TO-252AA) Package Outline

Dimensions are shown in millimeters (inches)

6.73 (.265)
6.35 (.250)
- A -

5.46 (.215)
5.21 (.205)

1.27 (.050)
0.88 (.035)

4

6.22 (.245)
5.97 (.235)

1.02 (.040)
1.64 (.025)

1   2   3

- B -

1.52 (.060)
1.15 (.045)

3X 0.89 (.035)
0.64 (.025)

2X 1.14 (.045)
0.76 (.030)

⊕ | 0.25 (.010) | Ⓜ A Ⓜ B

2.28 (.090)

4.57 (.180)

2.38 (.094)
2.19 (.086)

1.14 (.045)
0.89 (.035)

0.58 (.023)
0.46 (.018)

6.45 (.245)
5.68 (.224)

10.42 (.410)
9.40 (.370)

0.51 (.020)
MIN.

0.58 (.023)
0.46 (.018)

LEAD ASSIGNMENTS
1 - GATE
2 - DRAIN
3 - SOURCE
4 - DRAIN

NOTES:
1 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
2 CONTROLLING DIMENSION : INCH.
3 CONFORMS TO JEDEC OUTLINE TO-252AA.
4 DIMENSIONS SHOWN ARE BEFORE SOLDER DIP,
   SOLDER DIP MAX. +0.16 (.006).

D-Pak (TO-252AA) Part Marking Information

Notes: This part marking information applies to devices produced before 02/26/2001

EXAMPLE: THIS IS AN IRFR120
          WITH ASSEMBLY
          LOT CODE 9U1P

INTERNATIONAL
RECTIFIER
LOGO

IRFU120
IΩR 016
9U   1P

DATE CODE
YEAR = 0
WEEK = 16
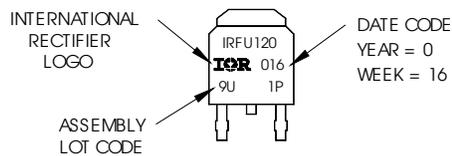
ASSEMBLY
LOT CODE

Notes: This part marking information applies to devices produced after 02/26/2001

EXAMPLE: THIS IS AN IRFR120
          WITH ASSEMBLY
          LOT CODE 1234
          ASSEMBLED ON WW 16, 1999
          IN THE ASSEMBLY LINE "A"

INTERNATIONAL
RECTIFIER
LOGO

IRFU120
IΩR 916A
12   34

PART NUMBER

DATE CODE
YEAR 9 = 1999
WEEK 16
LINE A

ASSEMBLY
LOT CODE
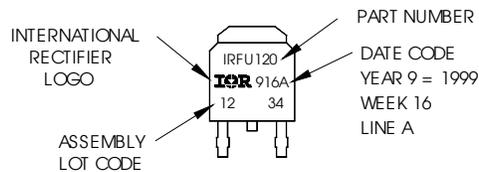
IRLR3717/IRLU3717

I-Pak (TO-251AA) Package Outline

Dimensions are shown in millimeters (inches)

6.73 (.265)
6.35 (.250)
- A -

5.46 (.215)
5.21 (.205)

1.27 (.050)
0.88 (.035)

4

1.52 (.060)
1.15 (.045)

6.22 (.245)
5.97 (.235)

1   2   3

- B -

2.28 (.090)
1.91 (.075)

9.65 (.380)
8.89 (.350)

3X   1.14 (.045)
0.76 (.030)

3X   0.89 (.035)
0.64 (.025)

2.28 (.090)
2X

⊕ 0.25 (.010) Ⓜ A Ⓜ B

2.38 (.094)
2.19 (.086)

0.58 (.023)
0.46 (.018)

6.45 (.245)
5.68 (.224)

1.14 (.045)
0.89 (.035)

0.58 (.023)
0.46 (.018)

LEAD ASSIGNMENTS
1 - GATE
2 - DRAIN
3 - SOURCE
4 - DRAIN

NOTES:
1 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
2 CONTROLLING DIMENSION : INCH.
3 CONFORMS TO JEDEC OUTLINE TO-252AA.
4 DIMENSIONS SHOWN ARE BEFORE SOLDER DIP,
   SOLDER DIP MAX. +0.16 (.006).

## I-Pak (TO-251AA) Part Marking Information

Notes: This part marking information applies to devices produced before 02/26/2001

EXAMPLE: THIS IS AN IRFR120
          WITH ASSEMBLY
          LOT CODE 9U1P

INTERNATIONAL
RECTIFIER
LOGO

IRFU120
IQR 016
9U   1P

DATE CODE
YEAR = 0
WEEK = 16
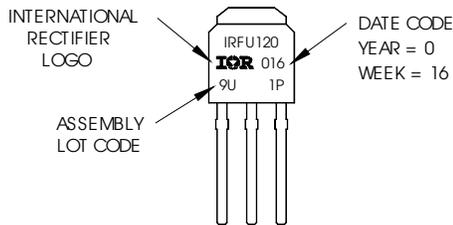
ASSEMBLY
LOT CODE

Notes: This part marking information applies to devices produced after 02/26/2001

EXAMPLE: THIS IS AN IRFR120
          WITH ASSEMBLY
          LOT CODE 5678
          ASSEMBLED ON WW 19, 1999
          IN THE ASSEMBLY LINE "A"

INTERNATIONAL
RECTIFIER
LOGO

IRFU120
IQR 919A
56   78

PART NUMBER
DATE CODE
YEAR 9 = 1999
WEEK 19
LINE A

ASSEMBLY
LOT CODE
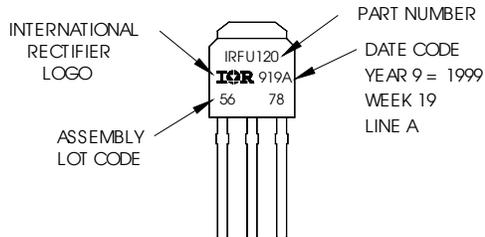
D-Pak (TO-252AA) Tape & Reel Information

Dimensions are shown in millimeters (inches)

TR

16.3 (.641)
15.7 (.619)

12.1 (.476)
11.9 (.469)

FEED DIRECTION

TRR   TRL

16.3 (.641)
15.7 (.619)

8.1 (.318)
7.9 (.312)

FEED DIRECTION
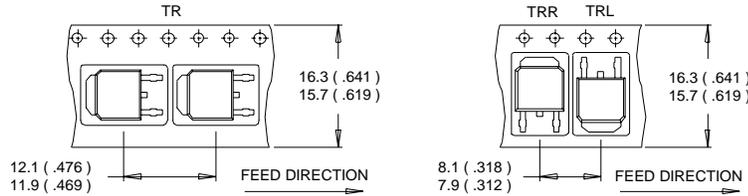
NOTES :
1. CONTROLLING DIMENSION : MILLIMETER.
2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
3. OUTLINE CONFORMS TO EIA-481 & EIA-541.

∅ 13 INCH

16 mm
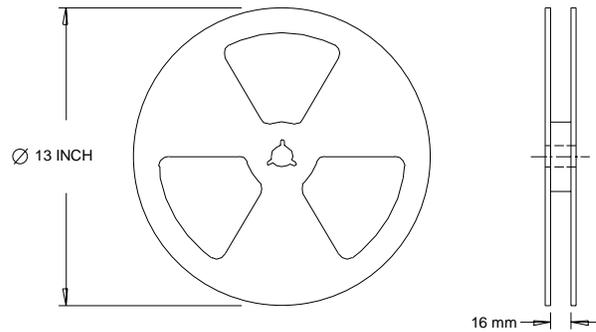
NOTES :
1. OUTLINE CONFORMS TO EIA-481.

Notes:

① Repetitive rating; pulse width limited by
   max. junction temperature.

② Starting T_J = 25°C, L = 6.4mH, R_G = 25Ω,
   I_{AS} = 12A.

③ Pulse width ≤ 400µs; duty cycle ≤ 2%.

④ Calculated continuous current based on maximum allowable
   junction temperature. Package limitation current is 30A.

⑤ When mounted on 1" square PCB (FR-4 or G-10 Material).
   For recommended footprint and soldering techniques refer to
   application note #AN-994.

Data and specifications subject to change without notice.
This product has been designed and qualified for the Industrial market.
Qualification Standards can be found on IR's Web site.

International
IR Rectifier