19-3256; Rev 0; 4/04

Dual, Low-Power, 500Mbps ATE Drivers/Comparators with 2mA Load

General Description

The MAX9961/MAX9962 dual, low-power, high-speed, pin electronics driver/comparator/load (DCL) ICs include, for each channel, a three-level pin driver, a dual comparator, variable clamps, and an active load. The driver features a wide voltage range and high-speed operation, includes high-impedance and active-termination (3rd-level drive) modes, and is highly linear even at low voltage swings. The dual comparator provides low dispersion (timing variation) over a wide variety of input conditions. The clamps provide damping of high-speed device-under-test (DUT) waveforms when the device is configured as a high-impedance receiver. The programmable load supplies up to 2mA of source and sink current. The load facilitates contact/continuity testing and pullup of high-output-impedance devices.

The MAX9961A/MAX9962A provide tight matching of offset for the drivers and the comparators, allowing reference levels to be shared across multiple channels in cost-sensitive systems. Use the MAX9961B/MAX9962B for system designs that incorporate independent reference levels for each channel.

The MAX9961/MAX9962 provide high-speed, differential control inputs compatible with LVPECL, LVDS, and GTL. The MAX9961/MAX9962 are available with optional internal termination resistors. The open-collector comparator outputs are available with or without internal pullup resistors. The optional internal resistors significantly reduce the discrete component count on the circuit board.

A 3-wire, low-voltage, CMOS-compatible serial interface programs the low-leakage, slew-rate limit, and tri-state/terminate operational configurations of the MAX9961/MAX9962.

The MAX9961/MAX9962s' operating range is -1.5V to +6.5V with power dissipation of only 900mW per channel. The devices are available in a 100-pin, 14mm x 14mm body, and 0.5mm pitch TQFP. An exposed 8mm x 8mm die pad on the top (MAX9961) or bottom (MAX9962) of the package facilitates efficient heat removal. The device is specified to operate with an internal die temperature of +70°C to +100°C, and features a die temperature monitor output.

Applications

Low-Cost Mixed-Signal/System-on-Chip ATE

Commodity Memory ATE

PCI or VXI Programmable Digital Instruments

Features

- ♦ **Low Power Dissipation: 900mW/Channel (typ)**
- ♦ **High Speed: 500Mbps at 3V$_{P-P}$**
- ♦ **Programmable 2mA Active-Load Current**
- ♦ **Low Timing Dispersion**
- ♦ **Wide -1.5V to +6.5V Operating Range**
- ♦ **Active Termination (3rd-Level Drive)**
- ♦ **Low-Leakage Mode: 15nA (max)**
- ♦ **Integrated Clamps**
- ♦ **Interface Easily with Most Logic Families**
- ♦ **Integrated PMU Connection**
- ♦ **Digitally Programmable Slew Rate**
- ♦ **Internal Termination Resistors**
- ♦ **Low Offset Error**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE**
MAX9961ADCCQ	0°C to +70°C	100 TQFP-EPR
MAX9961AGCCQ*	0°C to +70°C	100 TQFP-EPR
MAX9961ALCCQ	0°C to +70°C	100 TQFP-EPR
MAX9961BDCCQ	0°C to +70°C	100 TQFP-EPR
MAX9961BGCCQ*	0°C to +70°C	100 TQFP-EPR
MAX9961BLCCQ	0°C to +70°C	100 TQFP-EPR
MAX9962ADCCQ*	0°C to +70°C	100 TQFP-EP
MAX9962AGCCQ*	0°C to +70°C	100 TQFP-EP
MAX9962ALCCQ*	0°C to +70°C	100 TQFP-EP
MAX9962BDCCQ*	0°C to +70°C	100 TQFP-EP
MAX9962BGCCQ*	0°C to +70°C	100 TQFP-EP
MAX9962BLCCQ*	0°C to +70°C	100 TQFP-EP

*Future product—contact factory for availability.
**EPR = Exposed pad reversed (top), EP = exposed pad (bottom).

Pin Configurations appear at end of data sheet.

Selector Guide appears at end of data sheet.

Dual, Low-Power, 500Mbps ATE Drivers/Comparators with 2mA Load

ABSOLUTE MAXIMUM RATINGS

V_{CC} to GND .....-0.3V to +11.5V
V_{EE} to GND .....-7.0V to +0.3V
V_{CC} - V_{EE} .....-0.3V to +18V
GS to GND .....±1V
DATA_, NDATA_, RCV_, NRCV_, LDEN_, NLDEN_ to GND .....-2.5V to +5.0V
DATA_ to NDATA_, RCV_ to NRCV_, LDEN_ to NLDEN_ .....±1.5V
$V_{CCO\_}$ to GND .....-0.3V to +5V
SCLK, DIN, $\overline{CS}$, $\overline{RST}$, TDATA_, TRCV_, TLDEN_ to GND .....-1.0V to +5V
DHV_, DLV_, DTV_, CHV_, CLV_, COM_, FORCE_, SENSE_ to GND .....-2.5V to +7.5V
DUT_, LDH_, LDL_ to GND .....-2.5V to +7.5V
CPHV_ to GND .....-2.5V to +8.5V
CPLV_ to GND .....-3.5V to +7.5V
DHV_ to DLV_ .....±10V
DHV_ to DTV_ .....±10V
DLV_ to DTV_ .....±10V
CHV_ or CLV_ to DUT_ .....±10V
CH_, NCH_, CL_, NCL_ to GND .....-2.5V to +5V
All Other Pins to GND .....(V_{EE} - 0.3V) to (V_{CC} + 0.3V)
DHV_, DLV_, DTV_, CHV_, CLV_, CPHV_, CPLV_ Current .....±10mA
TEMP Current .....-0.5mA to +20mA
DUT_ Short Circuit to -1.5V to +6.5V .....Continuous
Power Dissipation (T_A = +70°C)
MAX9961_ _CCQ (derate 167mW/°C above +70°C) 13.3W*
MAX9962_ _CCQ (derate 45.5mW/°C above +70°C) 3.6W*
Storage Temperature Range .....-65°C to +150°C
Junction Temperature .....+125°C
Lead Temperature (soldering, 10s) .....+300°C

**Dissipation wattage values are based on still air with no heat sink for the MAX9961 and slug soldered to board copper for the MAX9962. Actual maximum allowable power dissipation is a function of heat extraction technique and may be substantially higher.*

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +9.75V, V_{EE} = -5.25V, $V_{CCO\_}$ = +2.5V, SC1 = SC0 = 0, $V_{CPHV\_}$ = +7.2V, $V_{CPLV\_}$ = -2.2V, $V_{LDH\_}$ = $V_{LDL\_}$ = 0, V_{GS} = 0, T_J = +85°C, unless otherwise noted. All temperature coefficients are measured at T_J = +70°C to +100°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLIES						
Positive Supply	V_{CC}		9.5	9.75	10.5	V
Negative Supply	V_{EE}		-6.5	-5.25	-4.5	V
Positive Supply Current (Note 2)	I_{CC}	$V_{LDH\_}$ = $V_{LDL\_}$ = 0		90	110	mA
		$V_{LDH\_}$ = $V_{LDL\_}$ = 5V		100	120	
Negative Supply Current (Note 2)	I_{EE}	$V_{LDH\_}$ = $V_{LDL\_}$ = 0		-180	-200	mA
		$V_{LDH\_}$ = $V_{LDL\_}$ = 5V		-190	-210	
Power Dissipation	P_D	(Notes 2, 3)		1.8	2.1	W
DUT_ CHARACTERISTICS						
Operating Voltage Range	V_{DUT}	(Note 4)	-1.5		+6.5	V
Leakage Current in High-Impedance Mode	I_{DUT}	LLEAK = 0, 0 ≤ $V_{DUT\_}$ ≤ 3V			±1.5	µA
		LLEAK = 0, $V_{DUT\_}$ = -1.5V, +6.5V			±3	
Leakage Current in Low-Leakage Mode		LLEAK = 1; $V_{DUT\_}$ = -1.5V, 0, +3V; $V_{LDH\_}$ = $V_{LDL\_}$ = 0, 5V; T_J < +90°C			±15	nA
		LLEAK = 1, $V_{DUT\_}$ = 6.5V, T_J < +90°C, $V_{CHV\_}$ = $V_{CLV\_}$ = 6.5V, $V_{LDH\_}$ = V_{LDL} = 0, 5V			±30	
Combined Capacitance	C_{DUT}	Driver in term mode (DUT_ = DTV_)		1		pF
		Driver in high-impedance mode		5		
Low-Leakage Enable Time		(Notes 5, 7)		20		µs

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +9.75V, V_{EE} = -5.25V, $V_{CCO\_}$ = +2.5V, SC1 = SC0 = 0, $V_{CPHV\_}$ = +7.2V, $V_{CPLV\_}$ = -2.2V, $V_{LDH\_}$ = $V_{LDL\_}$ = 0, V_{GS} = 0, T_J = +85°C, unless otherwise noted. All temperature coefficients are measured at T_J = +70°C to +100°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Low-Leakage Disable Time		(Notes 6, 7)		20		µs
Low-Leakage Recovery		Time to return to the specified maximum leakage after a 3V, 4V/ns step at DUT_ (Note 7)		15		µs
LEVEL PROGRAMMING INPUTS (DHV_, DLV_, DTV_, CHV_, CLV_, CPHV_, CPLV_, COM_, LDH_, LDL_)						
Input Bias Current	I_{BIAS}				±25	µA
Settling Time		To 0.1% of full-scale change (Note 7)		1		µs
DIFFERENTIAL CONTROL INPUTS (DATA_, NDATA_, RCV_, NRCV_, LDEN_, NLDEN_)						
Input High Voltage	V_{IH}		0.85		3.50	V
Input Low Voltage	V_{IL}		-0.20		+3.10	V
Differential Input Voltage	V_{DIFF}		±0.15		±1.00	V
Input Bias Current		MAX996_ _DCCQ,			±25	µA
Input Termination Voltage	$V_{TDATA\_}$ $V_{TRCV\_}$ $V_{TLDEN\_}$	MAX996_ _GCCQ, MAX996_ _LCCQ	-0.2		+3.5	V
Input Termination Resistor		MAX996_ _GCCQ, MAX996_ _LCCQ, between signal and corresponding termination voltage input	48		52	Ω
SINGLE-ENDED CONTROL INPUTS ($\overline{CS}$, SCLK, DIN, $\overline{RST}$)						
Internal Threshold Reference	V_{THRINT}		1.05	1.25	1.45	V
Internal Reference Output Resistance	R_O			20		kΩ
External Threshold Reference	V_{THR}		0.43		1.73	V
Input High Voltage	V_{IH}		V_{THR} + 0.20		3.5	V
Input Low Voltage	V_{IL}		-0.1		V_{THR} - 0.20	V
Input Bias Current	I_B				±25	µA
SERIAL INTERFACE TIMING (Figure 4)						
SCLK Frequency	f_{SCLK}				50	MHz
SCLK Pulse-Width High	t_{CH}		8			ns
SCLK Pulse-Width Low	t_{CL}		8			ns
$\overline{CS}$ Low to SCLK High Setup	t_{CSS0}		3.5			ns
$\overline{CS}$ High to SCLK High Setup	t_{CSS1}		3.5			ns
SCLK High to $\overline{CS}$ High Hold	t_{CSH1}		3.5			ns
DIN to SCLK High Setup	t_{DS}		3.5			ns
DIN to SCLK High Hold	t_{DH}		3.5			ns
$\overline{CS}$ Pulse-Width High	t_{CSWH}		20			ns

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +9.75V, V_{EE} = -5.25V, $V_{CCO\_}$ = +2.5V, SC1 = SC0 = 0, $V_{CPHV\_}$ = +7.2V, $V_{CPLV\_}$ = -2.2V, $V_{LDH\_}$ = $V_{LDL\_}$ = 0, V_{GS} = 0, T_J = +85°C, unless otherwise noted. All temperature coefficients are measured at T_J = +70°C to +100°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
TEMPERATURE MONITOR (TEMP)							
Nominal Voltage		T_J = +70°C, $R_L \geq 10M\Omega$			3.43		V
Temperature Coefficient					+10		mV/°C
Output Resistance					15		kΩ
DRIVERS (Note 8)							
DC OUTPUT CHARACTERISTICS ($R_L \geq 10M\Omega$)							
DHV_, DLV_, DTV_ Output Offset Voltage	V_{OS}	At DUT_ with $V_{DHV\_}$, $V_{DTV\_}$, $V_{DLV\_}$ independently tested at +1.5V	MAX996_A			±15	mV
			MAX996_B			±100	
DHV_, DLV_, DTV_ Output-Offset Temperature Coefficient					±65		µV/°C
DHV_, DLV_, DTV_ Gain	Av	Measured with $V_{DHV\_}$, $V_{DLV\_}$, and $V_{DTV\_}$ at 0 and 4.5V		0.960		1.001	V/V
DHV_, DLV_, DTV_ Gain Temperature Coefficient					-35		ppm/°C
Linearity Error		$V_{DUT\_}$ = 1.5V, 3V (Note 9)				±5	mV
		Full range (Notes 9, 10)				±15	
DHV_ to DLV_ Crosstalk		$V_{DLV\_}$ = 0, $V_{DHV\_}$ = 200mV, 6.5V				±2	mV
DLV_ to DHV_ Crosstalk		$V_{DHV\_}$ = 5V, $V_{DLV\_}$ = -1.5V, +4.8V				±2	mV
DTV_ to DLV_ and DHV_ Crosstalk		$V_{DHV\_}$ = 3V, $V_{DLV\_}$ = 0, $V_{DTV\_}$ = -1.5V, +6.5V				±2	mV
DHV_ to DTV_ Crosstalk		$V_{DTV\_}$ = 1.5V, $V_{DLV\_}$ = 0, $V_{DHV\_}$ = 1.6V, 3V				±3	mV
DLV_ to DTV_ Crosstalk		$V_{DTV\_}$ = 1.5V, $V_{DHV\_}$ = 3V, $V_{DLV\_}$ = 0V, 1.4V				±3	mV
DHV_, DTV_, DLV_ DC Power-Supply Rejection Ratio	PSRR	(Note 11)		40			dB
Maximum DC Drive Current	$I_{DUT\_}$			±60		±120	mA
DC Output Resistance	$R_{DUT\_}$	$I_{DUT\_}$ = ±30mA (Note 12)		49	50	51	Ω
DC Output Resistance Variation	$\Delta R_{DUT\_}$	$I_{DUT\_}$ = ±1mA to ±8mA			0.5		Ω
		$I_{DUT\_}$ = ±1mA to ±40mA			1	2.5	
Sense Resistance	R_{SENSE}			7.50	10	13.75	kΩ
Force Resistance	R_{FORCE}			320	400	500	Ω
Force Capacitance	C_{FORCE}				1		pF
DYNAMIC OUTPUT CHARACTERISTICS (Z_L = 50Ω)							
Drive-Mode Overshoot		$V_{DLV\_}$ = 0, $V_{DHV\_}$ = 0.1V			30		mV
		$V_{DLV\_}$ = 0, $V_{DHV\_}$ = 1V			40		
		$V_{DLV\_}$ = 0, $V_{DHV\_}$ = 3V			50		
Term-Mode Overshoot		(Note 13)			0		mV

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +9.75V, V_{EE} = -5.25V, $V_{CCO\_}$ = +2.5V, SC1 = SC0 = 0, $V_{CPHV\_}$ = +7.2V, $V_{CPLV\_}$ = -2.2V, $V_{LDH\_}$ = $V_{LDL\_}$ = 0, V_{GS} = 0, T_J = +85°C, unless otherwise noted. All temperature coefficients are measured at T_J = +70°C to +100°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Settling Time to Within 25mV		3V step (Note 14)		10		ns
Settling Time to Within 5mV		3V step (Note 14)		20		ns
TIMING CHARACTERISTICS (Z_L = 50Ω) (Note 15)						
Prop Delay, Data to Output	t_{PDD}			2.2		ns
Prop Delay Match, t_{LH} vs. t_{HL}		$3V_{P-P}$		±50		ps
Prop Delay Match, Drivers Within Package		(Note 16)		40		ps
Prop Delay Temperature Coefficient				+3		ps/°C
Prop Delay Change vs. Pulse Width		$3V_{P-P}$, 40MHz, 2.5ns to 22.5ns pulse width, relative to 12.5ns pulse width		±60		ps
Prop Delay Change vs. Common-Mode Voltage		$V_{DHV\_}$ - $V_{DLV\_}$ = 1V, $V_{DHV\_}$ = 0 to 6V		85		ps
Prop Delay, Drive to High Impedance	t_{PDDZ}	$V_{DHV\_}$ = 1.0V, $V_{DLV\_}$ = -1.0V, $V_{DTV\_}$ = 0		3.1		ns
Prop Delay, High Impedance to Drive	t_{PDZD}	$V_{DHV\_}$ = 1.0V, $V_{DLV\_}$ = -1.0V, $V_{DTV\_}$ = 0		3.2		ns
Prop Delay, Drive to Term	t_{PDDT}	$V_{DHV\_}$ = 3V, $V_{DLV\_}$ = 0, $V_{DTV\_}$ = 1.5V		2.4		ns
Prop Delay, Term to Drive	t_{PDTD}	$V_{DHV\_}$ = 3V, $V_{DLV\_}$ = 0, $V_{DTV\_}$ = 1.5V		2.1		ns
DYNAMIC PERFORMANCE (Z_L = 50Ω)						
Rise and Fall Time	t_R, t_F	$0.2V_{P-P}$, 20% to 80%		0.37		ns
		$1V_{P-P}$, 10% to 90%		0.63		
		$3V_{P-P}$, 10% to 90%	1.0	1.2	1.5	
		$5V_{P-P}$, 10% to 90%		2.0		
Rise- and Fall-Time Match	t_R vs. t_F	$3V_{P-P}$, 10% to 90%		±0.03		ns
SC1 = 0, SC0 = 1 Slew Rate		Percent of full speed (SC0 = SC1 = 0), $3V_{P-P}$, 20% to 80%		75		%
SC1 = 1, SC0 = 0 Slew Rate		Percent of full speed (SC0 = SC1 = 0), $3V_{P-P}$, 20% to 80%		50		%
SC1 = 1, SC0 = 1 Slew Rate		Percent of full speed (SC0 = SC1 = 0), $3V_{P-P}$, 20% to 80%		25		%
Minimum Pulse Width (Note 17)		$0.2V_{P-P}$		0.65		ns
		$1V_{P-P}$		1.0		
		$3V_{P-P}$		2.0		
		$5V_{P-P}$		2.9		
Data Rate (Note 18)		$0.2V_{P-P}$		1700		Mbps
		$1V_{P-P}$		1000		
		$3V_{P-P}$		500		
		$5V_{P-P}$		350		

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +9.75V, V_{EE} = -5.25V, $V_{CCO\_}$ = +2.5V, SC1 = SC0 = 0, $V_{CPHV\_}$ = +7.2V, $V_{CPLV\_}$ = -2.2V, $V_{LDH\_}$ = $V_{LDL\_}$ = 0, V_{GS} = 0, T_J = +85°C, unless otherwise noted. All temperature coefficients are measured at T_J = +70°C to +100°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Dynamic Crosstalk		(Note 19)			10		mV_{P-P}
Rise and Fall Time, Drive to Term	t_{DTR}, t_{DTF}	$V_{DHV\_}$ = 3V, $V_{DLV\_}$ = 0, $V_{DTV\_}$ = 1.5V, 10% to 90%, Figure 1a (Note 20)			1.6		ns
Rise and Fall Time, Term to Drive	t_{TDR}, t_{TDF}	$V_{DHV\_}$ = 3V, $V_{DLV\_}$ = 0, $V_{DTV\_}$ = 1.5V, 10% to 90%, Figure 1b (Note 20)			0.7		ns
COMPARATORS (Note 8)							
DC CHARACTERISTICS							
Input Voltage Range	V_{IN}	(Note 4)		-1.5		+6.5	V
Differential Input Voltage	V_{DIFF}			±8			V
Hysteresis	V_{HYST}				0		mV
Input Offset Voltage	V_{OS}	$V_{DUT\_}$ = 1.5V	MAX996_A			±20	mV
			MAX996_B			±100	
Input-Offset-Voltage Temperature Coefficient					±50		µV/°C
Common-Mode Rejection Ratio (Note 21)	CMRR	$V_{DUT\_}$ = 0, 3V		47	78		dB
		$V_{DUT\_}$ = 0, 6.5V		54	78		
		$V_{DUT\_}$ = -1.5, +6.5V		44	61		
Linearity Error (Note 9)		$V_{DUT\_}$ = 1.5V, 3V				±3	mV
		$V_{DUT\_}$ = 6.5V				±5	
		$V_{DUT\_}$ = -1.5V				±25	
V_{CC} Power-Supply Rejection Ratio (Note 11)	PSRR	$V_{DUT\_}$ = -1.5V, +6.5V		57	80		dB
V_{EE} Power-Supply Rejection Ratio (Note 11)	PSRR	$V_{DUT\_}$ = 0, 6.5V		44	64		dB
		$V_{DUT\_}$ = -1.5V		33	60		
AC CHARACTERISTICS (Note 22)							
Minimum Pulse Width	$t_{PW(MIN)}$	(Note 23)			0.7		ns
Prop Delay	t_{PDL}				2.2		ns
Prop Delay Temperature Coefficient					+6		ps/°C
Prop Delay Match, High/Low vs. Low/High					±25		ps
Prop Delay Match, Comparators Within Package		(Note 16)			35		ps
Prop Delay Dispersion vs. Common-Mode Input (Note 24)		$V_{CHV\_}$ = $V_{CLV\_}$ = 0, 6.4V			±75		ps
		$V_{CHV\_}$ = $V_{CLV\_}$ = -1.4V			±175		
Prop Delay Dispersion vs. Overdrive		100mV to 1V			220		ps

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +9.75V, V_{EE} = -5.25V, $V_{CCO\_}$ = +2.5V, SC1 = SC0 = 0, $V_{CPHV\_}$ = +7.2V, $V_{CPLV\_}$ = -2.2V, $V_{LDH\_}$ = $V_{LDL\_}$ = 0, V_{GS} = 0, T_J = +85°C, unless otherwise noted. All temperature coefficients are measured at T_J = +70°C to +100°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Prop Delay Dispersion vs. Pulse Width		2.5ns to 22.5ns pulse width, relative to 12.5ns pulse width			±40		ps
Prop Delay Dispersion vs. Slew Rate		0.5V/ns to 2V/ns slew rate			100		ps
Waveform Tracking 10% to 90%		$V_{DUT\_}$ = 1.0V_{P-P}, t_R = t_F = 1.0ns, 10% to 90% relative to timing at 50% point	Term mode		250		ps
			High-impedance mode		500		
LOGIC OUTPUTS (CH_, NCH_, CL_, NCL_)							
$V_{CCO\_}$ Voltage Range	$V_{VCCO\_}$			0		3.5	V
Output Low-Voltage Compliance		Set by I_{OL}, R_{TERM}, and $V_{CCO\_}$			-0.5		V
Output High Current	I_{OH}	MAX996_ _DCCQ, MAX996_ _GCCQ		-0.05	0	+0.10	mA
Output Low Current	I_{OL}	MAX996_ _DCCQ, MAX996_ _GCCQ		7.6	8	8.4	mA
Output High Voltage	V_{OH}	$I_{CH\_}$ = $I_{NCH\_}$ = $I_{CL\_}$ = $I_{NCL\_}$ = 0, MAX996_ _LCCQ		V_{CCO} - 0.05	$V_{CCO\_}$ - 0.005		V
Output Low Voltage	V_{OL}	$I_{CH\_}$ = $I_{NCH\_}$ = $I_{CL\_}$ = $I_{NCL\_}$ = 0, MAX996_ _LCCQ			$V_{CCO\_}$ - 0.4		V
Output Voltage Swing		$I_{CH\_}$ = $I_{NCH\_}$ = $I_{CL\_}$ = $I_{NCL\_}$ = 0, MAX996_ _LCCQ		360	390	440	mV
Output Termination Resistor	R_{TERM}	Single-ended measurement from $V_{CCO\_}$ to CH_, NCH_, CL_, NCL_, MAX996_ _LCCQ		48		52	Ω
Differential Rise Time	t_R	20% to 80%	MAX996_ _DCCQ, MAX996_ _GCCQ, R_{TERM} = 50Ω at end of line		280		ps
			MAX996_ _LCCQ		280		
Differential Fall Time	t_F	20% to 80%	MAX996_ _DCCQ, MAX996_ _GCCQ, R_{TERM} = 50Ω at end of line		280		ps
			MAX996_ _LCCQ		280		
CLAMPS							
High-Clamp Input Voltage Range	$V_{CPH\_}$			-0.3		+7.5	V
Low-Clamp Input Voltage Range	$V_{CPL\_}$			-2.5		+5.3	V
Clamp Offset Voltage	V_{OS}	At DUT_ with $I_{DUT\_}$ = 1mA, $V_{CPHV\_}$ = 0				±100	mV
		At DUT_ with $I_{DUT\_}$ = -1mA, $V_{CPLV\_}$ = 0				±100	
Offset-Voltage Temperature Coefficient					±0.5		mV/°C
Clamp Power-Supply Rejection Ratio (Note 11)	PSRR	$I_{DUT\_}$ = 1mA, $V_{CPHV\_}$ = 0			54		dB
		$I_{DUT\_}$ = -1mA, $V_{CPLV\_}$ = 0			54		
Voltage Gain	A_V			0.96		1.00	V/V

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +9.75V, V_{EE} = -5.25V, $V_{CCO\_}$ = +2.5V, SC1 = SC0 = 0, $V_{CPHV\_}$ = +7.2V, $V_{CPLV\_}$ = -2.2V, $V_{LDH\_}$ = $V_{LDL\_}$ = 0, V_{GS} = 0, T_J = +85°C, unless otherwise noted. All temperature coefficients are measured at T_J = +70°C to +100°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Voltage-Gain Temperature Coefficient				-100		ppm/°C
Clamp Linearity		$I_{DUT\_}$ = 1mA, $V_{CPLV\_}$ = -1.5V, $V_{CPHV\_}$ = -0.3V to +6.5V		±10		mV
		$I_{DUT\_}$ = -1mA, $V_{CPHV\_}$ = 6.5V, $V_{CPLV\_}$ = -1.5V to +5.3V		±10		
Short-Circuit Output Current	$I_{SCDUT\_}$	$V_{CPLV\_}$ = -1.5V, $V_{CPHV\_}$ = 0, $V_{DUT\_}$ = 6.5V	50		95	mA
		$V_{CPLV\_}$ = 5V, $V_{CPHV\_}$ = 6.5V, $V_{DUT\_}$ = -1.5V	-95		-50	
Clamp DC Impedance	R_{OUT}	$V_{CPHV\_}$ = 3V, $V_{CPLV\_}$ = 0, $I_{DUT\_}$ = ±5mA and ±15mA	50		55	Ω
ACTIVE LOAD (Driver in high-impedance mode, unless otherwise noted.)						
COMMUTATION AMPLIFIER ($V_{COM\_}$ = +2.5V, I_{SOURCE} = I_{SINK} = 2mA, R_L > 1MΩ)						
COM_ Voltage Range	$V_{COM\_}$		-1.5		+5.7	V
COM_ Offset Voltage	Vos				±100	mV
Offset-Voltage Temperature Coefficient				±100		µV/°C
COM_ Voltage Gain	A_V	$V_{COM\_}$ = 0, 4.5V	0.98		1.00	V/V
Voltage-Gain Temperature Coefficient				-20		ppm/°C
COM_ Linearity Error		$V_{COM\_}$ = -1.5V, +5.7V (Note 9)		±2	±15	mV
COM_ Output Voltage Power-Supply Rejection Ratio	PSRR		40			dB
OUTPUT CHARACTERISTICS (I_{SOURCE} = I_{SINK} = 2mA, R_L > 1MΩ)						
Differential Voltage Range		$V_{DUT\_}$ - $V_{COM\_}$	-7.2		+8.0	V
Output Resistance, Sink or Source	Ro	$V_{DUT\_}$ = 4.5V, 6.5V with $V_{COM\_}$ = -1.5V, and $V_{DUT\_}$ = -1.5V, +0.5V with $V_{COM\_}$ = 5.7V	200	500		kΩ
Output Resistance, Linear Region	Ro	$I_{DUT\_}$ = ±1mA, $V_{COM\_}$ = +2.5V		60		Ω
Deadband		95% I_{SOURCE} to 95% I_{SINK}, $V_{COM\_}$ = +2.5V		310	450	mV
SOURCE CURRENT ($V_{DUT\_}$ = +5V, $V_{COM\_}$ = +2.5V)						
Maximum Source Current		$V_{LDL\_}$ = 5.5V	2.1	2.2	2.3	mA
Source Programming Gain	A_{TC}	$V_{LDL\_}$ = 1.25V, 5V	392	400	408	µA/V
Source Current Offset (Combined Offset of LDL_ and GS)	I_{OS}	$V_{LDL\_}$ = 20mV	-5		+10	µA
Source-Current Temperature Coefficient		$V_{LDL\_}$ = 100mV		-0.02		µA/°C
		$V_{LDL\_}$ = 5V		-0.3		

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +9.75V, V_{EE} = -5.25V, $V_{CCO\_}$ = +2.5V, SC1 = SC0 = 0, $V_{CPHV\_}$ = +7.2V, $V_{CPLV\_}$ = -2.2V, $V_{LDH\_}$ = $V_{LDL\_}$ = 0, V_{GS} = 0, T_J = +85°C, unless otherwise noted. All temperature coefficients are measured at T_J = +70°C to +100°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Source-Current Power-Supply Rejection Ratio	PSRR	$V_{LDL\_}$ = 100mV		±0.7	±4	µA/V
		$V_{LDL\_}$ = 5V		±3	±100	
Source-Current Linearity (Note 25)		$V_{LDL\_}$ = 100mV, 1.25V, 5V		±2	±10	µA
SINK CURRENT ($V_{DUT\_}$ = 0, $V_{COM\_}$ = +2.5V)						
Maximum Sink Current		$V_{LDH\_}$ = 5.5V	-2.3	-2.2	-2.1	mA
Sink Programming Gain	A_{TC}	$V_{LDH\_}$ = 1.25V to 5V	-408	-400	-392	mA/V
Sink Current Offset (Combined Offset of LDH_ and GS)	I_{OS}	$V_{LDH\_}$ = 20mV	-10		+5	µA
Sink-Current Temperature Coefficient		$V_{LDH\_}$ = 100mV		+0.05		µA/°C
		$V_{LDH\_}$ = 5V		+0.4		
Sink-Current Power-Supply Rejection Ratio	PSRR	$V_{LDH\_}$ = 100mV		±1.3	±4	µA/V
		$V_{LDH\_}$ = 5V		±3.7	±100	
Sink-Current Linearity		$V_{LDH\_}$ = 100mV, 1.25V, 5V (Note 25)		±10	±25	µA
GROUND SENSE (GS)						
Voltage Range	V_{GS}	Verified by GS common-mode error test	±250			mV
Common-Mode Error		$V_{DUT\_}$ = 0, $V_{COM\_}$ = +2.5V, V_{GS} = ±250mV, $V_{LDH\_}$ - V_{GS} = 2.5V			±5	µA
		$V_{DUT\_}$ = 5V, $V_{COM\_}$ = +2.5V, V_{GS} = ±250mV, $V_{LDL\_}$ - V_{GS} = 2.5V			±5	
Input Bias Current		V_{GS} = 0			±25	µA
AC CHARACTERISTICS (Z_L = 50Ω to GND)						
Enable Time (Note 26)	t_{EN}	I_{SOURCE} = 2mA, $V_{COM\_}$ = -1.5V		2.5		ns
		I_{SINK} = 2mA, $V_{COM\_}$ = +1.5V		2.2		
Disable Time (Note 26)	t_{DIS}	I_{SOURCE} = 2mA, $V_{COM\_}$ = -1.5V		1.7		ns
		I_{SINK} = 2mA, $V_{COM\_}$ = +1.5V		1.7		
Current Settling Time on Commutation		I_{SOURCE} = I_{SINK} = 500µA (Notes 7 and 27), To 10%		0.4		ns
		I_{SOURCE} = I_{SINK} = 500µA (Notes 7 and 27), To 1%		1.1		
Spike During Enable/Disable Transition		I_{SOURCE} = I_{SINK} = 2mA, $V_{COM\_}$ = 0		30		mV

Note 1: All minimum and maximum limits are 100% production tested. Tests are performed at nominal supply voltages unless otherwise noted.

Note 2: Total for dual device at worst-case setting; driver enabled and load disabled. $R_L \geq 10M\Omega$. The supply currents are measured with typical supply voltages.

Note 3: Does not include internal dissipation of the comparator outputs. For MAX996_ _LCCQ, additional power dissipation is typically (32mA) x (V_{VCCO}).

Note 4: Externally forced voltages can exceed this range provided that the *Absolute Maximum Ratings* are not exceeded.

Note 5: Transition time from LLEAK being asserted to leakage current dropping below specified limits.

Note 6: Transition time from LLEAK being deasserted to output returning to normal operating mode.

Note 7: Based on simulation results only.

Note 8: With the exception of Offset and Gain/CMRR tests, reference input values are calibrated for offset and gain.

Note 9: Relative to straight line between 0 and 4.5V.

Dual, Low-Power, 500Mbps ATE Drivers/Comparators with 2mA Load

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +9.75V, V_{EE} = -5.25V, $V_{CCO\_}$ = +2.5V, SC1 = SC0 = 0, $V_{CPHV\_}$ = +7.2V, $V_{CPLV\_}$ = -2.2V, $V_{LDH\_}$ = $V_{LDL\_}$ = 0, V_{GS} = 0, T_J = +85°C, unless otherwise noted. All temperature coefficients are measured at T_J = +70°C to +100°C, unless otherwise noted.) (Note 1)

Note 10: Specifications measured at the end points of the full range. Full ranges are -1.3V ≤ $V_{DHV\_}$ ≤ +6.5V, -1.5V ≤ $V_{DLV\_}$ ≤ +6.3V, -1.5V ≤ $V_{DTV\_}$ ≤ +6.5V.

Note 11: Change in offset voltage with power supplies independently set to their minimum and maximum values.

Note 12: Nominal target value is 50Ω. Contact factory for alternate trim selections within the 45Ω to 51Ω range.

Note 13: $V_{DTV\_}$ = +1.5V, R_S = 50Ω. External signal driven into T-line is a 0 to +3V edge with 1.2ns rise time (10% to 90%). Measurement is made using the comparator.

Note 14: Measured from the crossing point of DATA_ inputs to the settling of the driver output.

Note 15: Prop delays are measured from the crossing point of the differential input signals to the 50% point of the expected output swing. Rise time of the differential inputs DATA_ and RCV_ is 250ps (10% to 90%).

Note 16: Rising edge to rising edge or falling edge to falling edge.

Note 17: Specified amplitude is programmed. At this pulse width, the output reaches at least 95% of its nominal (DC) amplitude. The pulse width is measured at DATA_.

Note 18: Specified amplitude is programmed. Maximum data rate is specified in transitions per second. A square wave that reaches at least 95% of its programmed amplitude may be generated at one-half this frequency.

Note 19: Crosstalk from either driver to the other. Aggressor channel is driving $3V_{P-P}$ into a 50Ω load. Victim channel is in term mode with $V_{DTV\_}$ = +1.5V.

Note 20: Indicative of switching speed from DHV_ or DLV_ to DTV_ and DTV_ to DHV_ or DLV_ when $V_{DLV\_} < V_{DTV\_} < V_{DHV\_}$. If $V_{DTV\_} < V_{DLV\_}$ or $V_{DTV\_} > V_{DHV\_}$, switching speed is degraded by a factor of approximately 3.

Note 21: Change in offset voltage over the input range.

Note 22: Unless otherwise noted, all propagation delays are measured at 40MHz, $V_{DUT\_}$ = 0 to +2V, $V_{CHV\_}$ = $V_{CLV\_}$ = +1V, slew rate = 2V/ns, Z_S = 50Ω, driver in term mode with $V_{DTV\_}$ = 0. Comparator outputs are terminated with 50Ω to GND at scope input with $V_{CCO\_}$ = 2V. Open-collector outputs are also terminated (internally or externally) with R_{TERM} = 50Ω to $V_{CCO\_}$. Measured from $V_{DUT\_}$ crossing calibrated CHV_ / CLV_ threshold to crossing point of differential outputs.

Note 23: $V_{DUT\_}$ = 0 to +1V, $V_{CHV\_}$ = $V_{CLV\_}$ = +0.5V. At this pulse width, the output reaches at least 90% of its DC voltage swing. The pulse width is measured at the crossing points of the differential outputs.

Note 24: Relative to propagation delay at $V_{CHV\_}$ = $V_{CLV\_}$ = +1.5V. $V_{DUT\_}$ = $200mV_{P-P}$. Overdrive = 100mV.

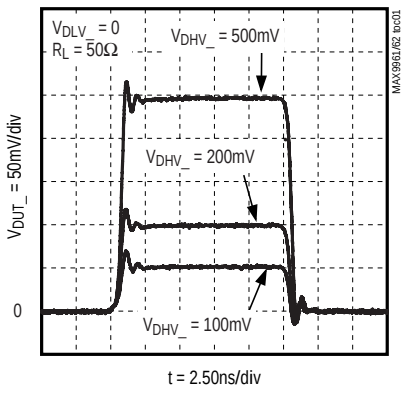
Note 25: Relative to straight line between 0.5V and 2.5V.

Note 26: Measured from crossing of input signals to the 10% point of the output voltage change.

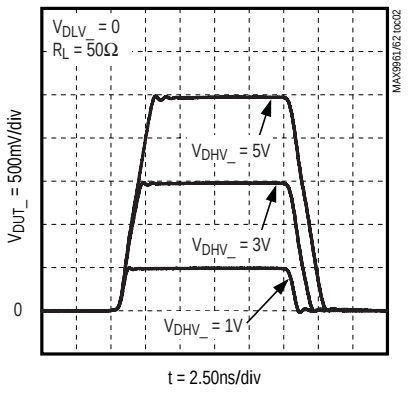
Note 27: $V_{COM\_}$ = 1.5V, Z_S = 50Ω, driving voltage = 3V to 0 transition and 0 to 3V transition. Settling time is measured from $V_{DUT\_}$ = 1.5V to I_{SINK} or I_{SOURCE} settling within specified tolerance.

Typical Operating Characteristics

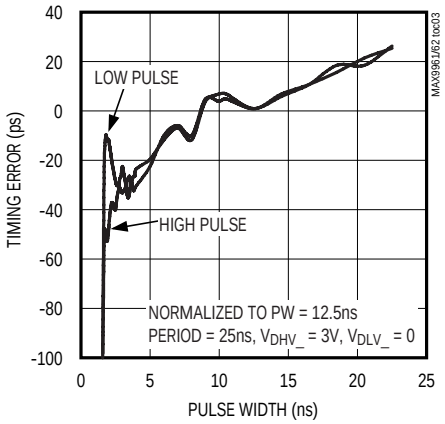
DRIVER SMALL-SIGNAL RESPONSE



DRIVER LARGE-SIGNAL RESPONSE

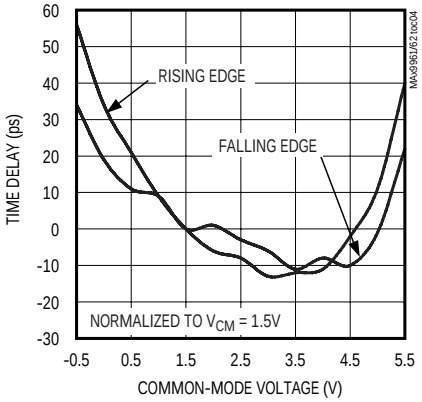


DRIVER TRAILING-EDGE TIMING ERROR vs. PULSE WIDTH

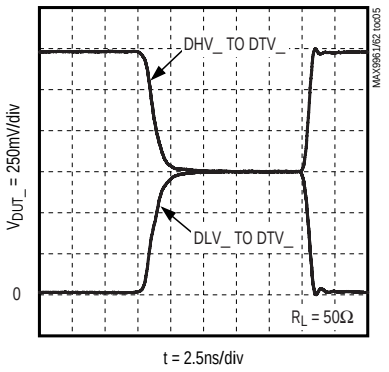


Typical Operating Characteristics (continued)

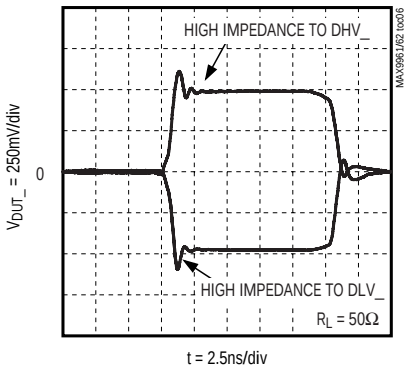
DRIVER TIME DELAY vs. COMMON-MODE VOLTAGE



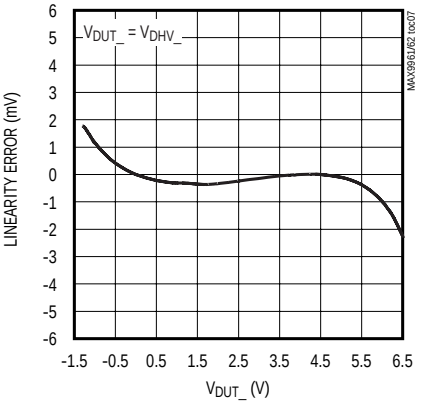
DRIVE-TO-TERM TRANSITION



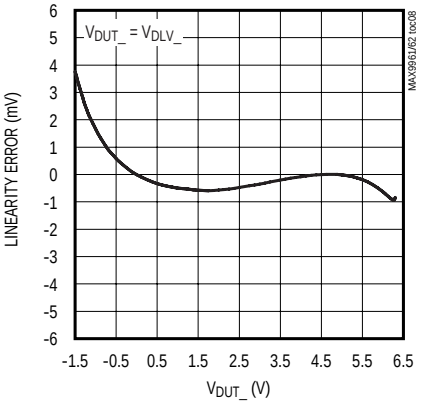
HIGH-IMPEDANCE-TO-DRIVE TRANSITION



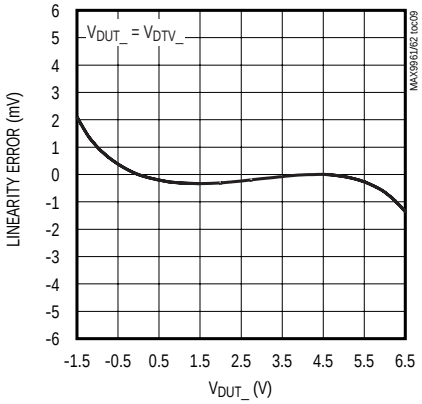
DRIVER LINEARITY ERROR vs. OUTPUT VOLTAGE



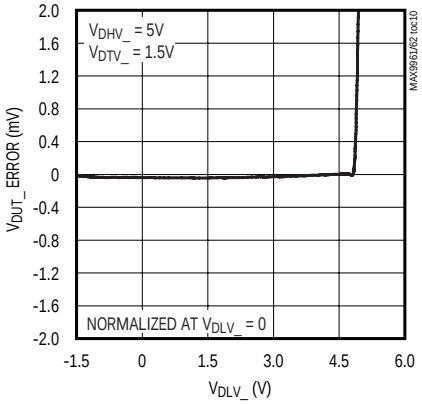
DRIVER LINEARITY ERROR vs. OUTPUT VOLTAGE



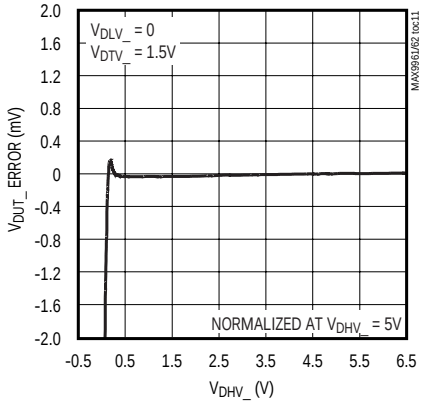
DRIVER LINEARITY ERROR vs. OUTPUT VOLTAGE



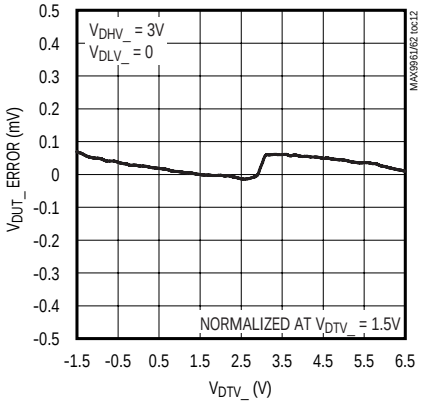
CROSSTALK TO DUT_ FROM DLV_ WITH DUT_ = DHV_



CROSSTALK TO DUT_ FROM DHV_ WITH DUT_ = DLV_



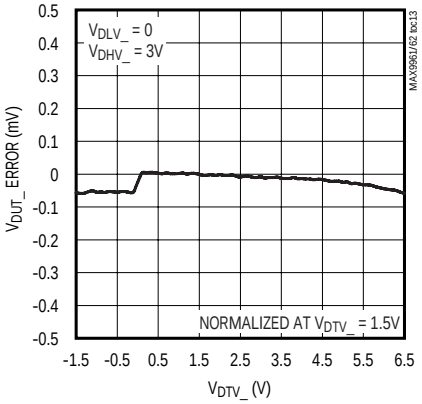
CROSSTALK TO DUT_ FROM DTV_ WITH DUT_ = DHV_



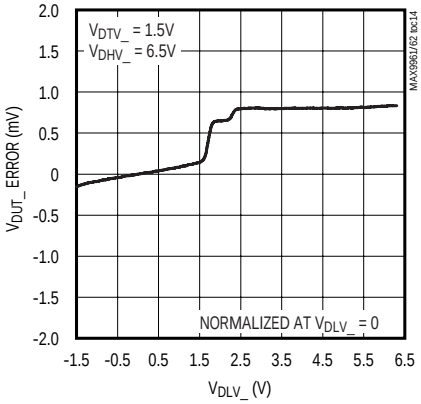
Dual, Low-Power, 500Mbps ATE Drivers/Comparators with 2mA Load

Typical Operating Characteristics (continued)

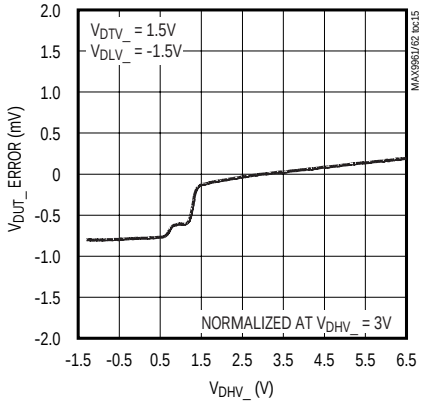
CROSSTALK TO DUT_ FROM DTV_ WITH DUT_ = DLV_



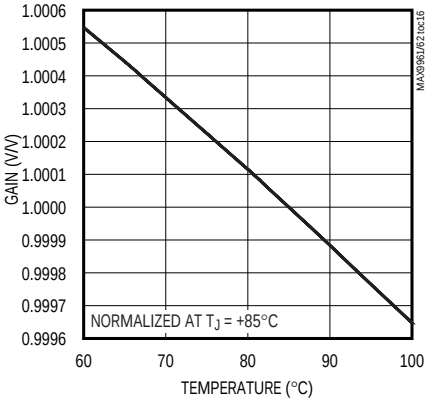
CROSSTALK TO DUT_ FROM DLV_ WITH DUT_ = DTV_



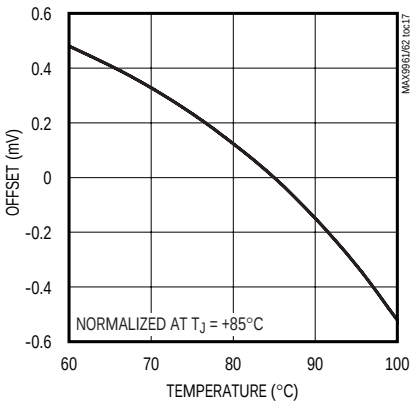
CROSSTALK TO DUT_ FROM DHV_ WITH DUT_ = DTV_



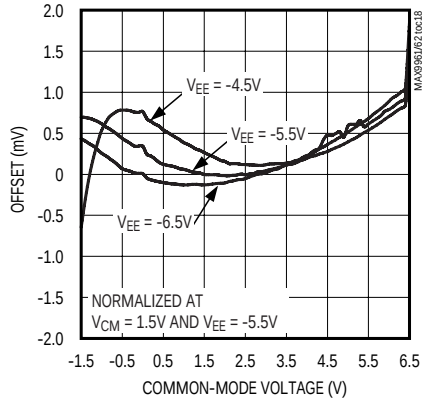
DRIVER GAIN vs. TEMPERATURE



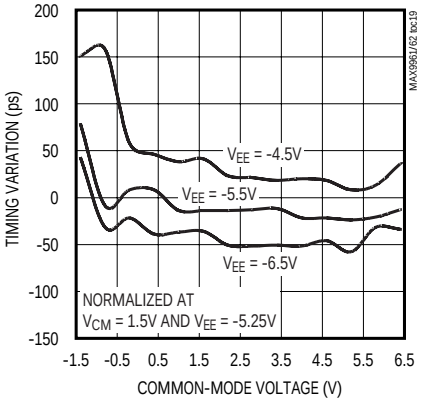
DRIVER OFFSET vs. TEMPERATURE



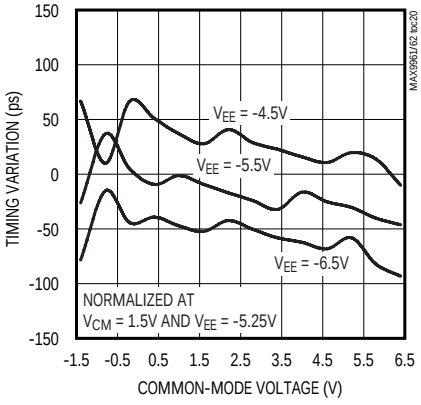
COMPARATOR OFFSET vs. COMMON-MODE VOLTAGE



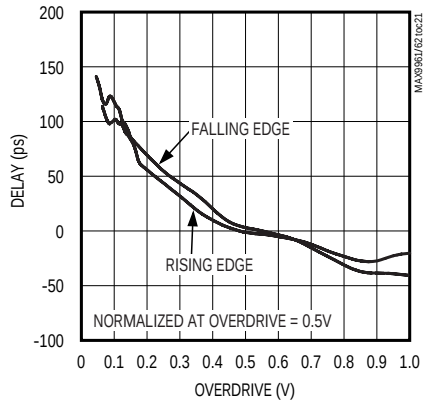
COMPARATOR RISING-EDGE TIMING VARIATION vs. COMMON-MODE VOLTAGE



COMPARATOR FALLING-EDGE TIMING VARIATION vs. COMMON-MODE VOLTAGE

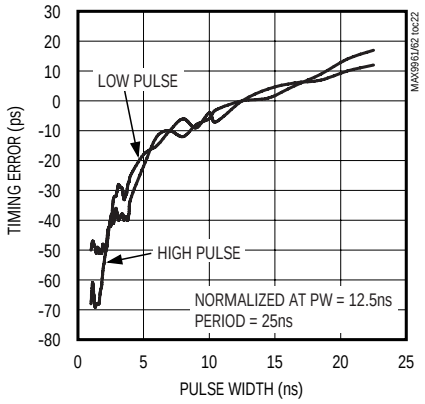


COMPARATOR TIMING VARIATION vs. OVERDRIVE

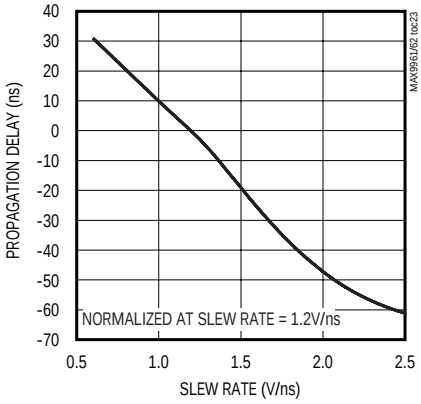


Typical Operating Characteristics (continued)

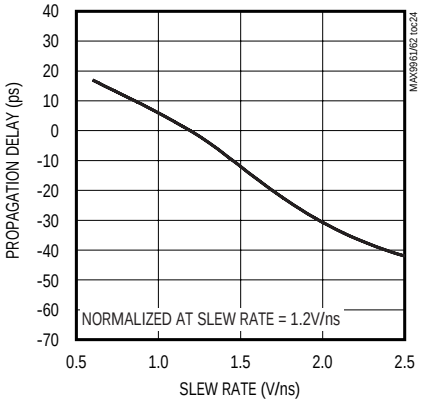
COMPARATOR TRAILING-EDGE TIMING ERROR vs. PULSE WIDTH



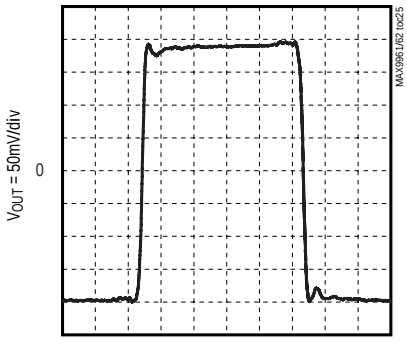
COMPARATOR TIMING VARIATION vs. INPUT SLEW RATE, DUT_ RISING



COMPARATOR TIMING VARIATION vs. INPUT SLEW RATE, DUT_ FALLING

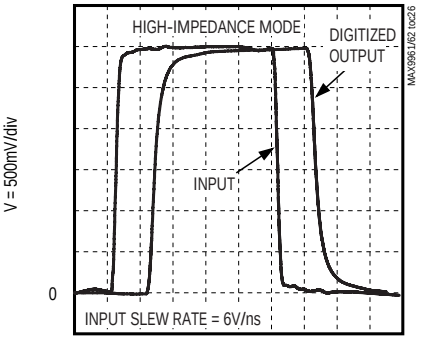


COMPARATOR DIFFERENTIAL OUTPUT RESPONSE

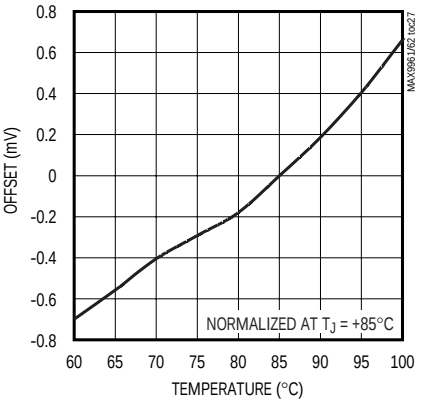


$V_{DUT\_}$ = 0 TO 3V PULSE, $V_{CHV\_}$ = $V_{CLV\_}$ = +1.5V
EXTERNAL LOAD = 50Ω

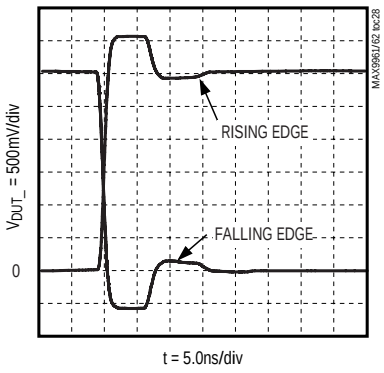
COMPARATOR RESPONSE vs. HIGH SLEW-RATE OVERDRIVE



COMPARATOR OFFSET vs. TEMPERATURE

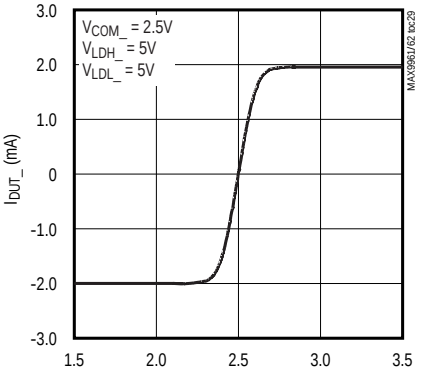


CLAMP RESPONSE

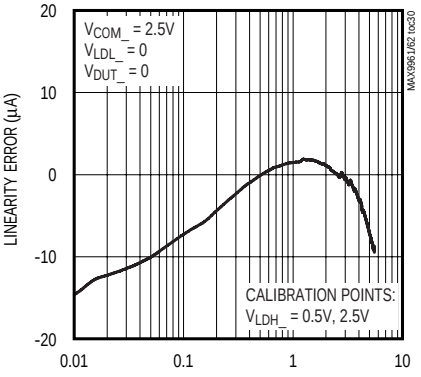


$V_{DUT\_}$ = 0 TO 3V SQUARE WAVE
R_S = 25Ω
$V_{CPLV\_}$ = -0.1V, $V_{CPHV\_}$ = +3.1V

ACTIVE-LOAD VOLTAGE vs. CURRENT



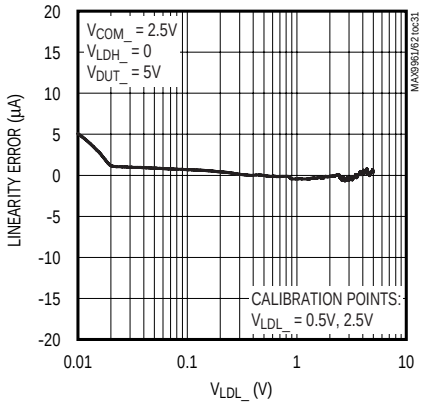
ACTIVE-LOAD LINEARITY ERROR $I_{DUT\_}$ vs. $V_{LDH\_}$



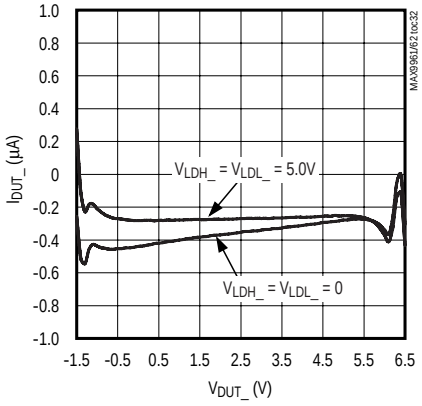
Dual, Low-Power, 500Mbps ATE Drivers/Comparators with 2mA Load

Typical Operating Characteristics (continued)

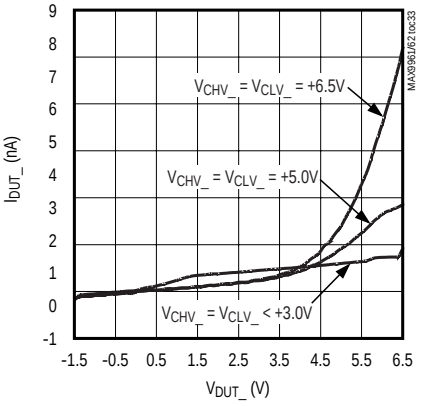
ACTIVE-LOAD LINEARITY ERROR
$I_{DUT\_}$ vs. $V_{LDL\_}$



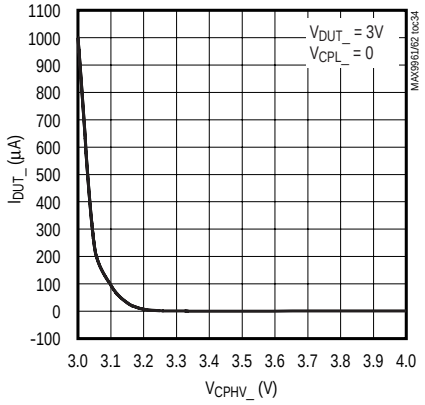
HIGH-IMPEDANCE LEAKAGE CURRENT vs. DUT_ VOLTAGE



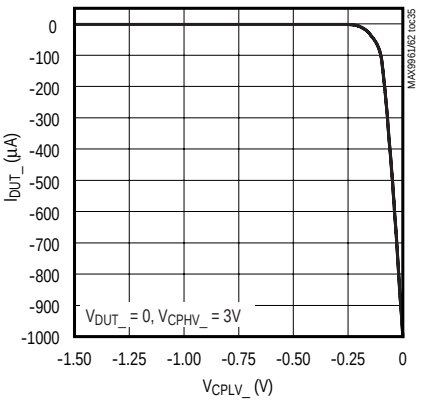
LOW-LEAKAGE CURRENT vs. DUT_ VOLTAGE



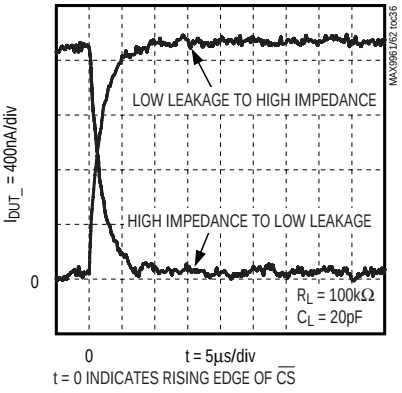
CLAMP CURRENT vs. DIFFERENCE VOLTAGE



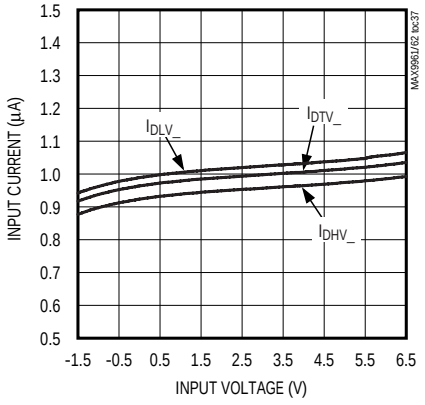
CLAMP CURRENT vs. DIFFERENCE VOLTAGE



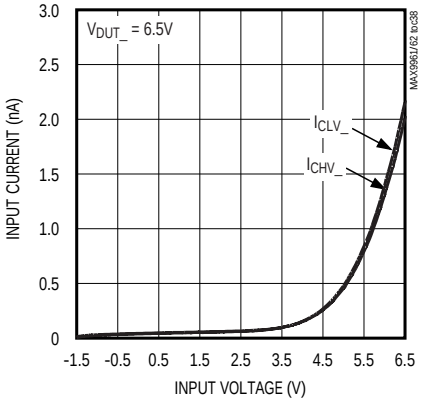
HIGH-IMPEDANCE-TO-LOW-LEAKAGE TRANSITION



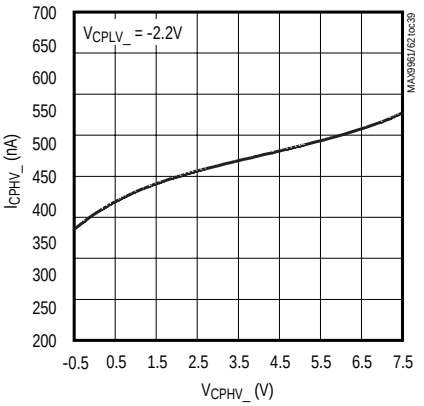
DRIVER REFERENCE INPUT CURRENTS vs. INPUT VOLTAGE



COMPARATOR REFERENCE INPUT CURRENT vs. INPUT VOLTAGE

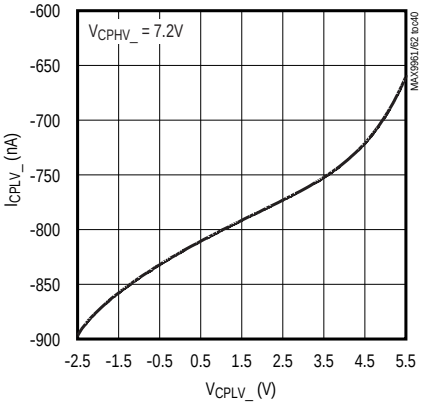


INPUT CURRENT vs. INPUT VOLTAGE, CPHV_

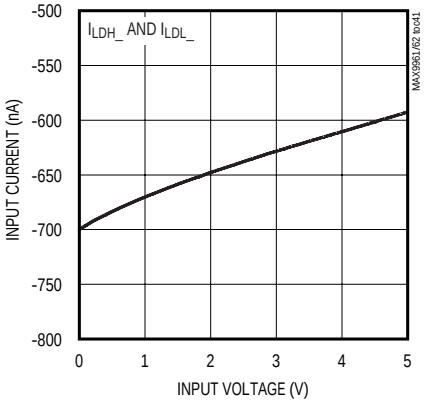


Typical Operating Characteristics (continued)

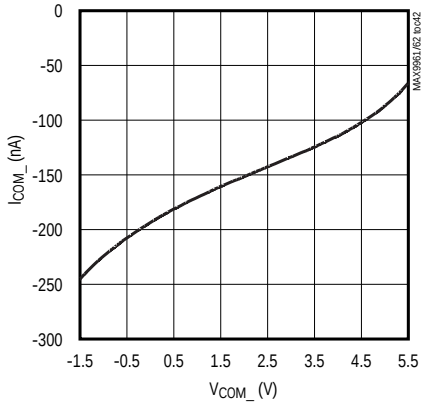
INPUT CURRENT vs. INPUT VOLTAGE, CPLV_



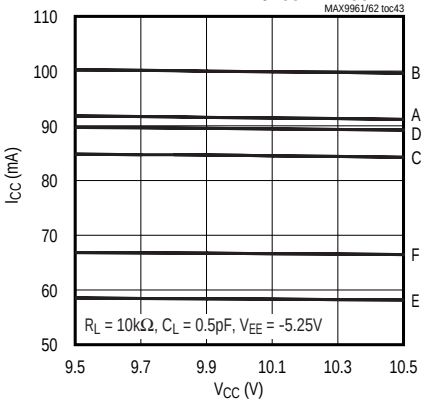
LOAD REFERENCE INPUT CURRENTS vs. INPUT VOLTAGE



INPUT CURRENTS vs. INPUT VOLTAGE, COM_

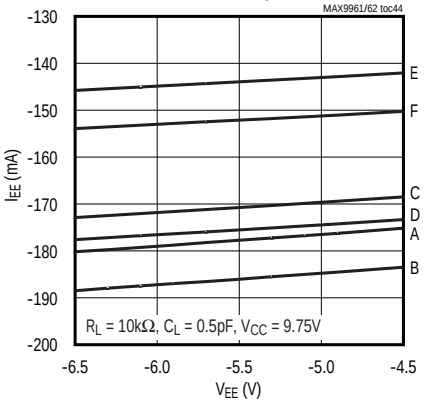


SUPPLY CURRENT, I_{CC} vs. V_{CC}



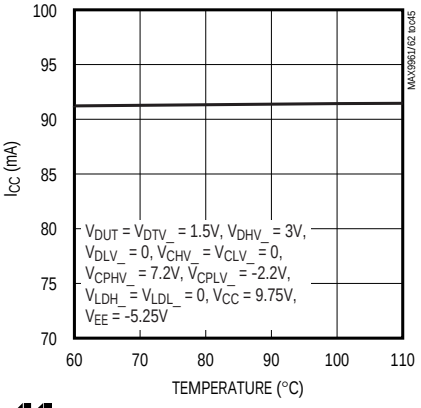
A: $V_{DUT\_} = V_{DTV\_}$ = 1.5V, $V_{DHV\_}$ = 3V, $V_{DLV\_}$ = 0, $V_{CHV\_} = V_{CLV\_}$ = 0, $V_{CPHV\_}$ = 7.2V, $V_{CPLV\_}$ = -2.2V, $V_{LDH\_} = V_{LDL\_}$ = 0
B: SAME AS 'A' EXCEPT $V_{LDH\_} = V_{LDL\_}$ = 5V
C: SAME AS 'A' EXCEPT DRIVER DISABLED HIGH-Z AND LOAD ENABLED
D: SAME AS 'C' EXCEPT $V_{LDH\_} = V_{LDL\_}$ = 5V
E: SAME AS 'A' EXCEPT LOW-LEAKAGE MODE ASSERTED
F: SAME AS 'E' EXCEPT $V_{LDH\_} = V_{LDL\_}$ = 5V

SUPPLY CURRENT, I_{EE} vs. V_{EE}

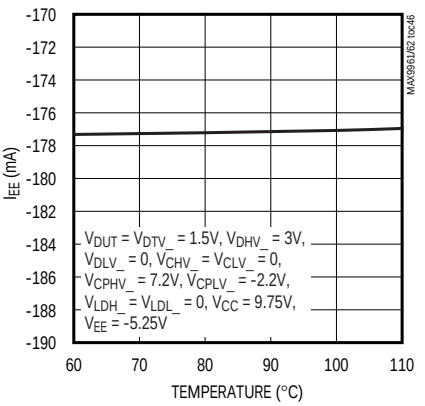


A: $V_{DUT\_} = V_{DTV\_}$ = 1.5V, $V_{DHV\_}$ = 3V, $V_{DLV\_}$ = 0, $V_{CHV\_} = V_{CLV\_}$ = 0, $V_{CPHV\_}$ = 7.2V, $V_{CPLV\_}$ = -2.2V, $V_{LDH\_} = V_{LDL\_}$ = 0
B: SAME AS 'A' EXCEPT $V_{LDH\_} = V_{LDL\_}$ = 5V
C: SAME AS 'A' EXCEPT DRIVER DISABLED HIGH-Z AND LOAD ENABLED
D: SAME AS 'C' EXCEPT $V_{LDH\_} = V_{LDL\_}$ = 5V
E: SAME AS 'A' EXCEPT LOW-LEAKAGE MODE ASSERTED
F: SAME AS 'E' EXCEPT $V_{LDH\_} = V_{LDL\_}$ = 5V

I_{CC} vs. TEMPERATURE



I_{EE} vs. TEMPERATURE



Dual, Low-Power, 500Mbps ATE Drivers/Comparators with 2mA Load

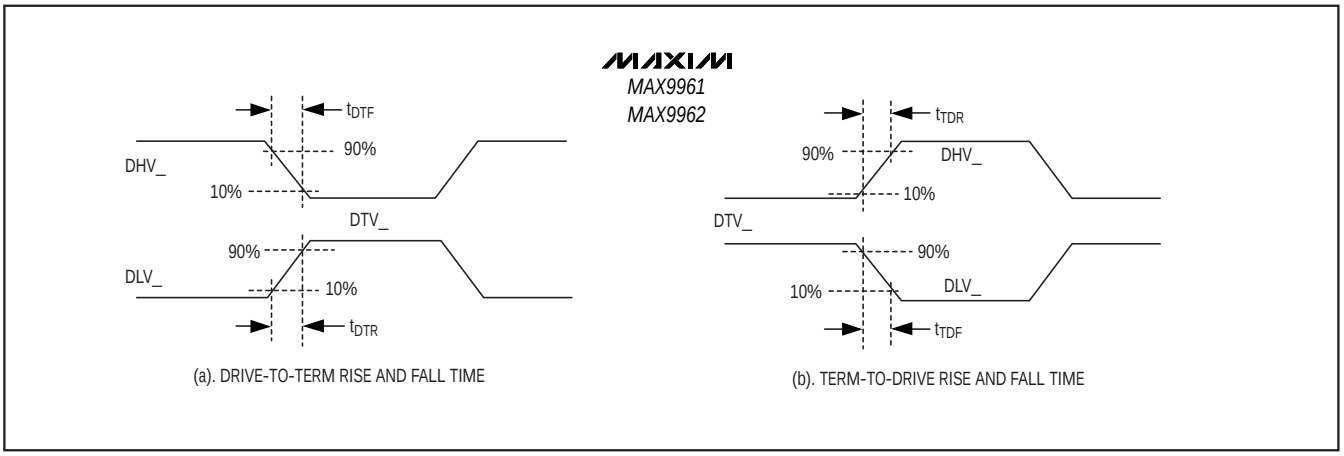


Figure 1. Drive and Term Timing

Pin Description

PIN		NAME	FUNCTION
MAX9961	MAX9962		
1	25	TEMP	Temperature Monitor Output
2, 9, 12, 14, 17, 24, 35, 45, 46, 60, 80, 81, 91	2, 9, 12, 14, 17, 24, 35, 45, 46, 66, 80, 81, 91	V_{EE}	Negative Power-Supply Input
3, 5, 10, 16, 21, 23, 25, 34, 43, 44, 82, 83, 92	1, 3, 5, 10, 16, 21, 23, 34, 43, 44, 82, 83, 92	GND	Ground Connection
4, 11, 15, 22, 33, 41, 42, 66, 84, 85, 93	4, 11, 15, 22, 33, 41, 42, 60, 84, 85, 93	V_{CC}	Positive Power-Supply Input
6	20	FORCE1	Channel 1 Force Input from External PMU
7	19	DUT1	Channel 1 Device-Under-Test Input/Output. Combined I/O for driver, comparator, clamp, and load.
8	18	SENSE1	Channel 1 Sense Output to External PMU
13	13	GS	Ground Sense. GS is the ground reference for LDH_ and LDL_.
18	8	SENSE2	Channel 2 Sense Output to External PMU
19	7	DUT2	Channel 2 Device-Under-Test Input/Output. Combined I/O for driver, comparator, clamp, and load.
20	6	FORCE2	Channel 2 Force Input from External PMU
26	100	CLV2	Channel 2 Low Comparator Reference Input
27	99	CHV2	Channel 2 High Comparator Reference Input
28	98	DLV2	Channel 2 Driver Low Reference Input

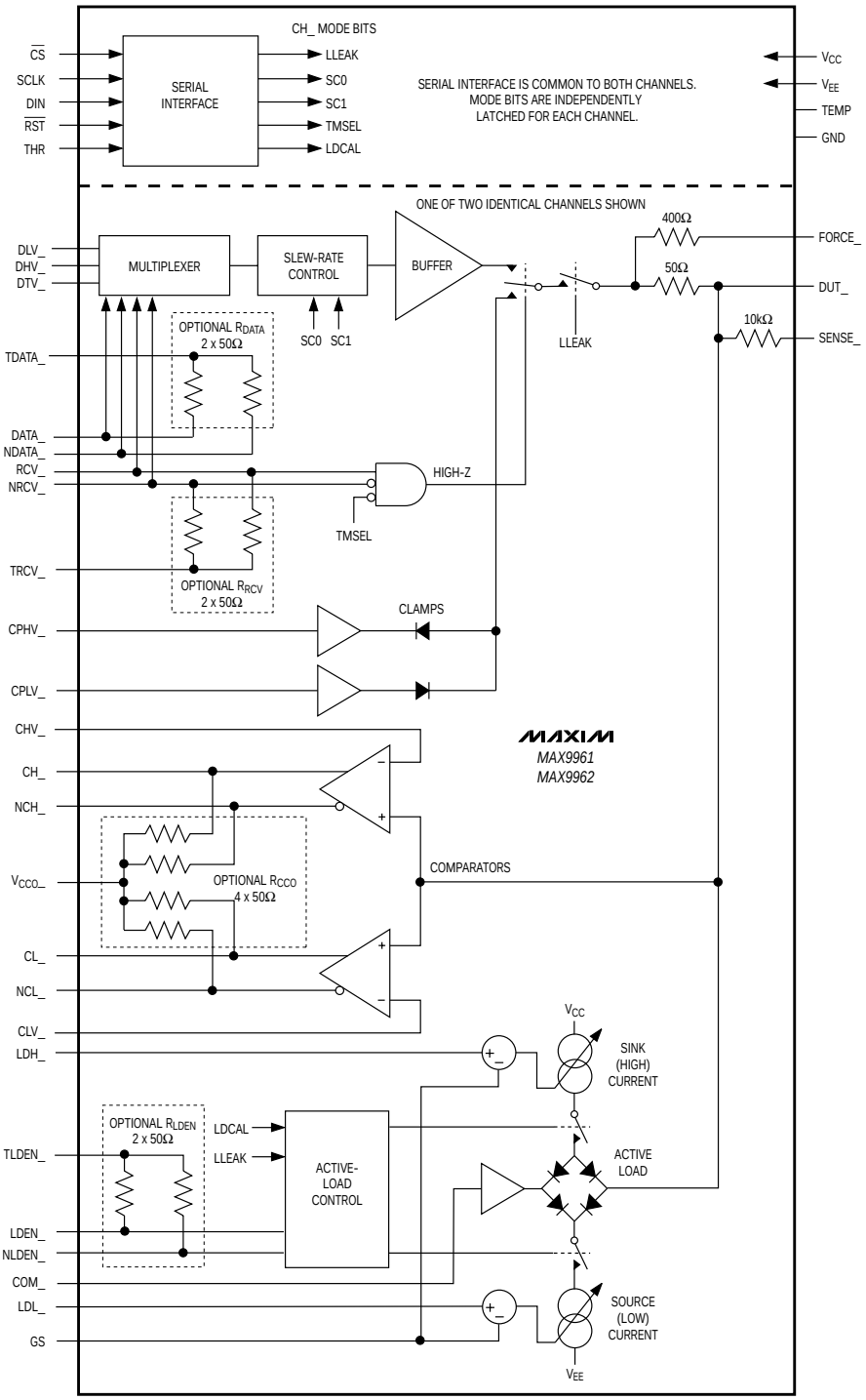
Pin Description (continued)

PIN		NAME	FUNCTION
MAX9961	MAX9962		
29	97	DTV2	Channel 2 Driver Termination Reference Input
30	96	DHV2	Channel 2 Driver High Reference Input
31	95	CPLV2	Channel 2 Low Clamp Reference Input
32	94	CPHV2	Channel 2 High Clamp Reference Input
36	90	NCH2	Channel 2 Comparator High Output. Differential output of channel 2 high comparator.
37	89	CH2	
38	88	V_{CCO2}	Channel 2 Collector Voltage Input. Voltage for channel 2 comparator output pullup resistors. This is the pullup voltage for the internal termination resistors. Not internally connected on versions without internal termination resistors.
39	87	NCL2	Channel 2 Comparator Low Output. Differential output of channel 2 low comparator.
40	86	CL2	
47	79	COM2	Channel 2 Active-Load Commutation-Voltage Reference Input
48	78	LDL2	Channel 2 Active-Load Source-Current Reference Input
49	77	LDH2	Channel 2 Active-Load Sink-Current Reference Input
50, 76	50, 76	N.C.	No Connection. Do not connect.
51	75	TDATA2	Channel 2 Data Termination Voltage Input. Termination voltage input for the DATA2 and NDATA2 differential inputs. Not internally connected on versions without internal termination resistors.
52	74	NDATA2	Channel 2 Multiplexer Control Inputs. Differential controls DATA2 and NDATA2 select driver 2's input from DHV2 or DLV2. Drive DATA2 above NDATA2 to select DHV2. Drive NDATA2 above DATA2 to select DLV2.
53	73	DATA2	
54	72	TRCV2	Channel 2 RCV Termination Voltage Input. Termination voltage input for the RCV2 and NRCV2 differential inputs. Not internally connected on versions without internal termination resistors.
55	71	NRCV2	Channel 2 Multiplexer Control Inputs. Differential controls RCV2 and NRCV2 place channel 2 into receive mode. Drive RCV2 above NRCV2 to place channel 2 into receive mode. Drive NRCV2 above RCV2 to place channel 2 into drive mode.
56	70	RCV2	
57	69	TLDEN2	Channel 2 Load-Enable Termination Voltage Input. Termination voltage input for the LDEN2 and NLDEN2 differential inputs. Not internally connected on versions without internal termination resistors.
58	68	NLDEN2	Channel 2 Multiplexer Control Inputs. Differential controls LDEN2 and NLDEN2 enable/disable the active load. Drive LDEN2 above NLDEN2 to enable the channel 2 active load. Drive NLDEN2 above LDEN2 to disable the channel 2 active load.
59	67	LDEN2	
61	65	$\overline{RST}$	Reset Input. Asynchronous reset input for the serial register. $\overline{RST}$ is active low and asserts low-leakage mode. At power-up, hold $\overline{RST}$ low until V_{CC} and V_{EE} have stabilized.
62	64	$\overline{CS}$	Chip-Select Input. Serial port activation input. $\overline{CS}$ is active low.
63	63	THR	Single-Ended Logic Threshold. Leave THR unconnected to set the threshold to +1.25V or force THR to a desired threshold voltage.
64	62	SCLK	Serial-Clock Input. Clock for serial port.
65	61	DIN	Data Input. Serial port data input.

Pin Description (continued)

PIN		NAME	FUNCTION
MAX9961	MAX9962		
67	59	LDEN1	Channel 1 Multiplexer Control Inputs. Differential controls LDEN1 and NLDEN1 enable/disable the active load. Drive LDEN1 above NLDEN1 to enable the channel 1 active load. Drive NLDEN1 above LDEN1 to disable the channel 1 active load.
68	58	NLDEN1	
69	57	TLDEN1	Channel 1 Load-Enable Termination Voltage Input. Termination voltage input for the LDEN1 and NLDEN1 differential inputs. Not internally connected on versions without internal termination resistors.
70	56	RCV1	Channel 1 Multiplexer Control Inputs. Differential controls RCV1 and NRCV1 place channel 1 into receive mode. Drive RCV1 above NRCV1 to place channel 1 into receive mode. Drive NRCV1 above RCV1 to place channel 1 into drive mode.
71	55	NRCV1	
72	54	TRCV1	Channel 1 RCV Termination Voltage Input. Termination voltage input for the RCV1 and NRCV1 differential inputs. Not internally connected on versions without internal termination resistors.
73	53	DATA1	Channel 1 Multiplexer Control Inputs. Differential controls DATA1 and NDATA1 select driver 1's input from DHV1 or DLV1. Drive DATA1 above NDATA1 to select DHV1. Drive NDATA1 above DATA1 to select DLV1.
74	52	NDATA1	
75	51	TDATA1	Channel 1 Data Termination Voltage Input. Termination voltage input for the DATA1 and NDATA1 differential inputs. Not internally connected on versions without internal termination resistors.
77	49	LDH1	Channel 1 Active-Load Sink-Current Reference Input
78	48	LDL1	Channel 1 Active-Load Source-Current Reference Input
79	47	COM1	Channel 1 Active-Load Commutation-Voltage Reference Input
86	40	CL1	Channel 1 Low Comparator Output. Differential output of channel 1 low comparator.
87	39	NCL1	
88	38	V_{CCO1}	Channel 1 Collector Voltage Input. Voltage for channel 1 comparator output pullup resistors. This is the pullup voltage for the internal termination resistors. Not internally connected on versions without internal termination resistors.
89	37	CH1	Channel 1 High Comparator High Output. Differential output of channel 1 high-side comparator.
90	36	NCH1	
94	32	CPHV1	Channel 1 High Clamp Reference Input
95	31	CPLV1	Channel 1 Low Clamp Reference Input
96	30	DHV1	Channel 1 Driver High Reference Input
97	29	DTV1	Channel 1 Driver Termination Reference Input
98	28	DLV1	Channel 1 Driver Low Reference Input
99	27	CHV1	Channel 1 High Comparator Reference Input
100	26	CLV1	Channel 1 Low Comparator Reference Input
—	—	PAD	Exposed Pad. The exposed pad for heat removal is at V_{EE} potential. Connect to V_{EE} or leave isolated.

Functional Diagram



Dual, Low-Power, 500Mbps ATE Drivers/Comparators with 2mA Load

Detailed Description

The MAX9961/MAX9962 dual, low-power, high-speed, pin electronics DCL ICs include, for each channel, a three-level pin driver, a dual comparator, variable clamps, and an active load. The driver features a -1.5V to +6.5V operating range and high-speed operation, includes high-impedance and active-termination (3rd-level drive) modes, and is highly linear even at low voltage swings. The dual comparator provides low dispersion (timing variation) over a wide variety of input conditions. The clamps provide damping of high-speed DUT_ waveforms when the device is configured as a high-impedance receiver. The programmable load supplies up to 2mA of source and sink current. The load facilitates contact/continuity testing and pullup of high-output-impedance devices.

The MAX9961A/MAX9962A provide tight matching of offset for the drivers and the comparators allowing reference levels to be shared across multiple channels in cost-sensitive systems. Use the MAX9961B/MAX9962B for system designs that incorporate independent reference levels for each channel.

Optional internal resistors at the high-speed inputs provide compatibility with LVPECL, LVDS, and GTL interfaces. Connect the termination voltage inputs (TDATA_, TRCV_, TLDEN_) to the appropriate voltage for terminating LVPECL, GTL, or other logic. Leave the inputs unconnected for 100Ω differential LVDS termination. See the *Selector Guide* for termination options.

The comparators provide open-collector outputs, which must be pulled up to collector voltage V_{CCO}. Optional internal resistors provide 50Ω signal termination and pullup without the need for external components. See the *Selector Guide* for device termination options. See the *Comparators* section for termination details.

A 3-wire, low-voltage, CMOS-compatible serial interface programs the low-leakage, load calibration, slew rate, and tri-state/terminate operational configurations of the MAX9961/MAX9962.

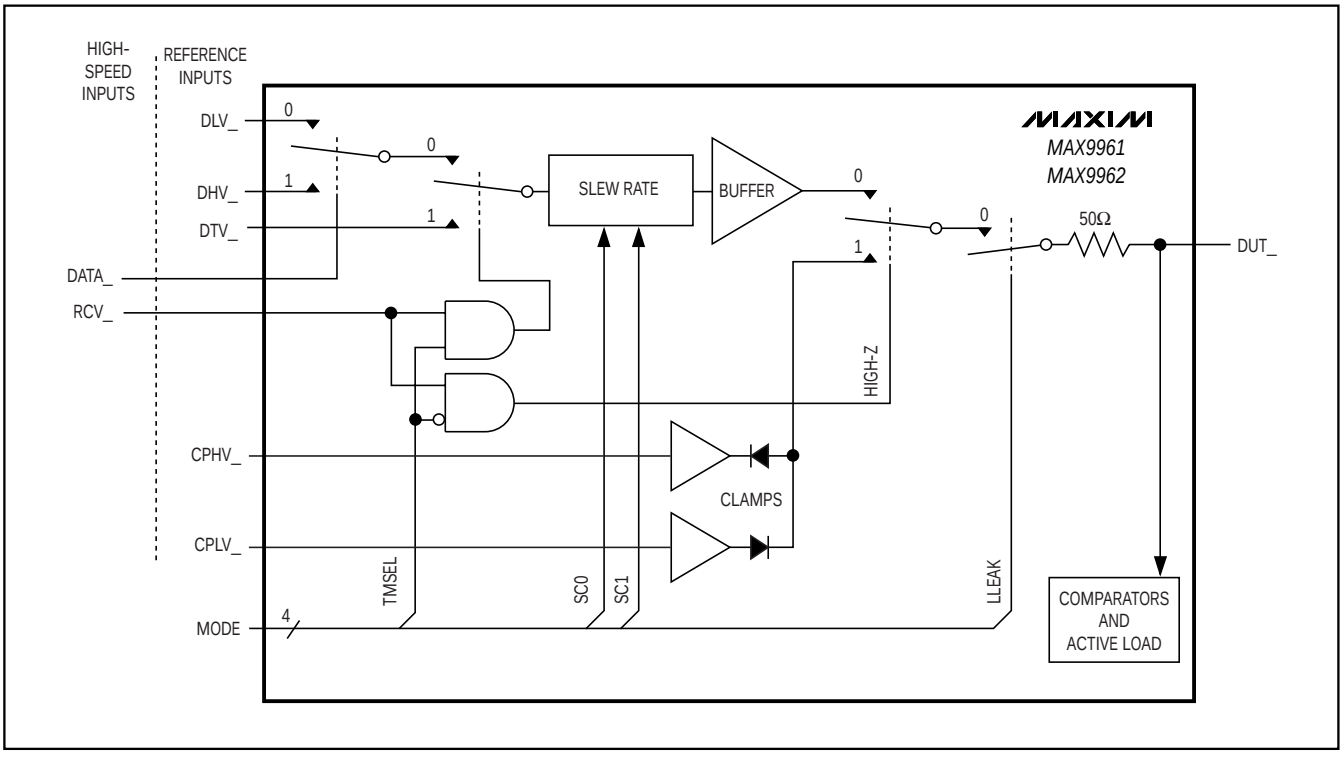


Figure 2. Simplified Driver Channel

Output Driver

The driver input is a high-speed multiplexer that selects one of three voltage inputs: DHV_, DLV_, or DTV_. This switching is controlled by high-speed inputs DATA_ and RCV_, and mode-control bit TMSEL (Table 1). A slew-rate circuit controls the slew rate of the buffer input. Select to one of four possible slew rates according to Table 2. The speed of the internal multiplexer sets the 100% driver slew rate (see the Driver Large-Signal Response graph in the *Typical Operating Characteristics*).

DUT_ can be toggled at high speed between the buffer output and high-impedance mode, or it can be placed into low-leakage mode (Figure 2, Table 1). In high-impedance mode the clamps are connected. High-speed input RCV_ and mode control bits TMSEL and LLEAK control the switching. In high-impedance mode, the bias current at DUT_ is less than 1.5µA over the 0 to 3V range, while the node maintains its ability to track high-speed signals. In low-leakage mode, the bias current at DUT_ is further reduced to less than 15nA, and signal tracking slows. See the *Low-Leakage Mode* section for more details.

The nominal driver output resistance is 50Ω. Contact the factory for different resistance values within the 45Ω to 51Ω range.

Clamps

Configure the voltage clamps (high and low) to limit the voltage at DUT_ and to suppress reflections when the channel is configured as a high-impedance receiver. The clamps behave as diodes connected to the outputs of high-current buffers. Internal circuitry compensates for the diode drop at 1mA clamp current. Set the clamp voltages using the external connections CPHV_ and CPLV_. The clamps are enabled only when the driver is in the high-impedance mode (Figure 2). For transient suppression, set the clamp voltages to approximately the minimum and maximum expected DUT_ voltage range. The optimal clamp voltages are application specific and must be empirically determined. If clamping is not desired, set the clamp voltages at least 0.7V outside the expected DUT_ voltage range; overvoltage protection remains active without loading DUT_.

Comparators

The MAX9961/MAX9962 provide two independent high-speed comparators for each channel. Each comparator has one input connected internally to DUT_ and the other input connected to either CHV_ or CLV_ (see the *Functional Diagram*). Comparator outputs are a logical result of the input conditions, as indicated in Table 3.

Table 1. Driver Logic

EXTERNAL CONNECTIONS		INTERNAL CONTROL REGISTER		DRIVER OUTPUT
DATA_	RCV_	TMSEL	LLEAK	
1	0	X	0	Drive to DHV_
0	0	X	0	Drive to DLV_
X	1	1	0	Drive to DTV_ (term mode)
X	1	0	0	High-impedance mode (high-z)
X	X	X	1	Low-leakage mode

Table 2. Slew Rate Logic

SC1	SC0	DRIVER SLEW RATE (%)
0	0	100
0	1	75
1	0	50
1	1	25

Table 3. Comparator Logic

DUT_ > CHV_	DUT_ > CLV_	CH_	CL_
0	0	0	0
0	1	0	1
1	0	1	0
1	1	1	1

The comparator differential outputs are open collector. This configuration switches an 8mA current source between the two outputs, and is available with and without internal termination resistors connected to $V_{CCO\_}$ (Figure 3). For external termination, leave $V_{CCO\_}$ unconnected and add the required external resistors. These resistors are typically 50Ω to the pullup voltage at the receiving end of the output trace. Alternate configurations to terminate different path impedances can be used provided that the *Absolute Maximum Ratings* are not exceeded. Note that the resistor value also sets the voltage swing. For internal termination, connect $V_{CCO\_}$ to the desired V_{OH} voltage. The output provides a nominal 400mV_{P-P} swing and 50Ω source termination.

Dual, Low-Power, 500Mbps ATE Drivers/Comparators with 2mA Load

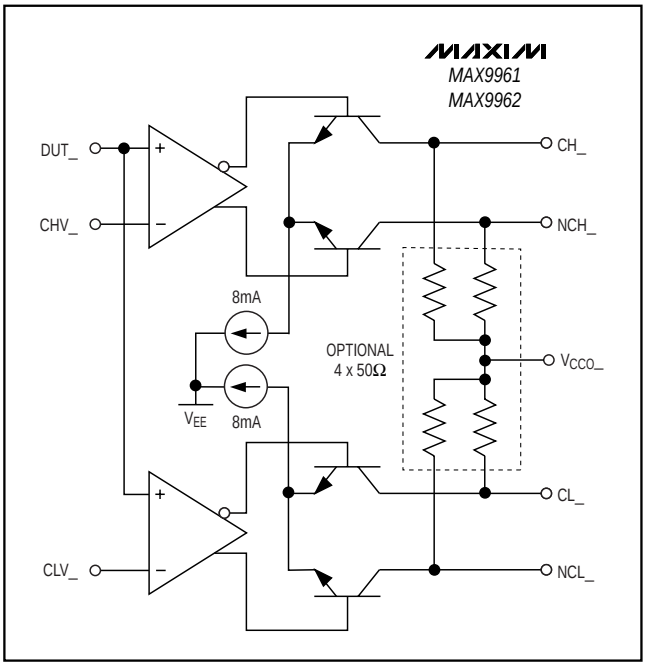


Figure 3. Open-Collector Comparator Outputs

Active Load

The active load consists of linearly programmable source and sink current sources, a commutation buffer, and a diode bridge (see the *Functional Diagram*). Analog control inputs LDH_ and LDL_ program the sink and source currents, respectively, within the 0 to 2mA range. Analog reference input COM_ sets the commutation buffer output voltage. The source and sink naming convention is referenced to the device under test. Current out of the MAX9961/MAX9962 constitutes sink current while current into the MAX9961/MAX9962 constitutes source current.

The programmed source (low) current loads the device under test when $V_{DUT\_} > V_{COM\_}$. The programmed sink (high) current loads the device under test when $V_{DUT\_} < V_{COM\_}$.

The GS input allows a single level-setting DAC, such as the MAX5631 or MAX5734, to program the MAX9961/MAX9962s' active load, driver, comparator, and clamps. Although all the DAC levels typically are offset by V_{GS}, the operation of the MAX9961/MAX9962s' ground-sense input nullifies this offset with respect to the active-load currents. Connect GS to the ground reference used by the DAC. ($V_{LDL\_}$ - V_{GS}) sets the source current by +400µA/V. ($V_{LDH\_}$ - V_{GS}) sets the sink current by -400µA/V.

Table 4. Active Load Programming

EXTERNAL CONNECTIONS	INTERNAL CONTROL REGISTER		MODE
LDEN_	LDCAL	LLEAK	
0	0	0	Normal operating mode, load disabled
1	0	0	Normal operating mode, load enabled
X	1	0	Load enabled for diagnostics
X	X	1	Low-leakage mode

The high-speed differential input LDEN_ and 2 bits of the control word, LDCAL and LLEAK, control the load (Table 4). When the load is enabled, the internal source and sink current sources connect to the diode bridge. When the load is disabled, the internal current sources shunt to ground and the top and bottom of the bridge float (see the *Functional Diagram*). LLEAK places the load into low-leakage mode. LLEAK overrides LDEN_ and LDCAL. See the *Low-Leakage Mode* section for more detailed information.

Load Calibration Enable, LDCAL

The LDCAL signal enables the load independently of the state of LDEN_. In some tester configurations, the load enable is driven with the complement of the driver high-impedance signal (RCV_), so disabling the driver enables the load and vice versa. LDCAL allows the load and driver to be simultaneously enabled for diagnostic purposes in this tester configuration (Table 4).

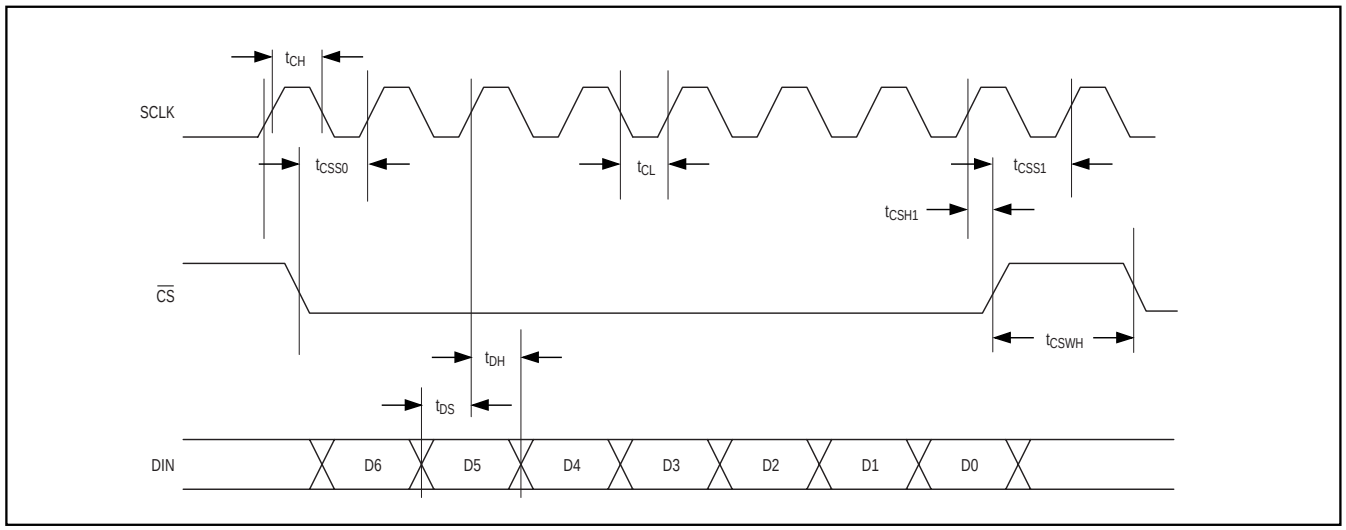


Figure 4. Serial Interface Timing

Low-Leakage Mode, LLEAK

Asserting LLEAK through the serial port or with $\overline{RST}$ places the MAX9961/MAX9962 into a very-low-leakage state (see *Electrical Characteristics*). The comparators function at full speed, but the driver, clamps, and active load are disabled. This mode is convenient for making IDDQ and PMU measurements without the need for an output disconnect relay. LLEAK is independent for each channel.

When DUT_ is driven with a high-speed signal while LLEAK is asserted, the leakage current momentarily increases beyond the limits specified for normal operation. The low-leakage recovery specification in the *Electrical Characteristics* table indicates device behavior under this condition.

Serial Interface and Device Control

A CMOS-compatible serial interface controls the MAX9961/MAX9962 modes (Figure 5). Control data flow into a 7-bit shift register (MSB first) and are latched when $\overline{CS}$ is taken high, as shown in Figure 4. Data from the shift register are then loaded to either or both of the latches as determined by bits D5 and D6, and indicated in Figure 5 and Table 5. The latches contain the 5 mode bits for each channel of the dual-pin driver. The mode bits, in conjunction with external inputs DATA_ and RCV_, manage the features of each channel, as shown in Figure 2 and Tables 1 and 2. $\overline{RST}$ sets LLEAK = 1 for both channels, forcing them into low-leakage mode. At power-up, hold $\overline{RST}$ low until V_{CC} and V_{EE} have stabilized.

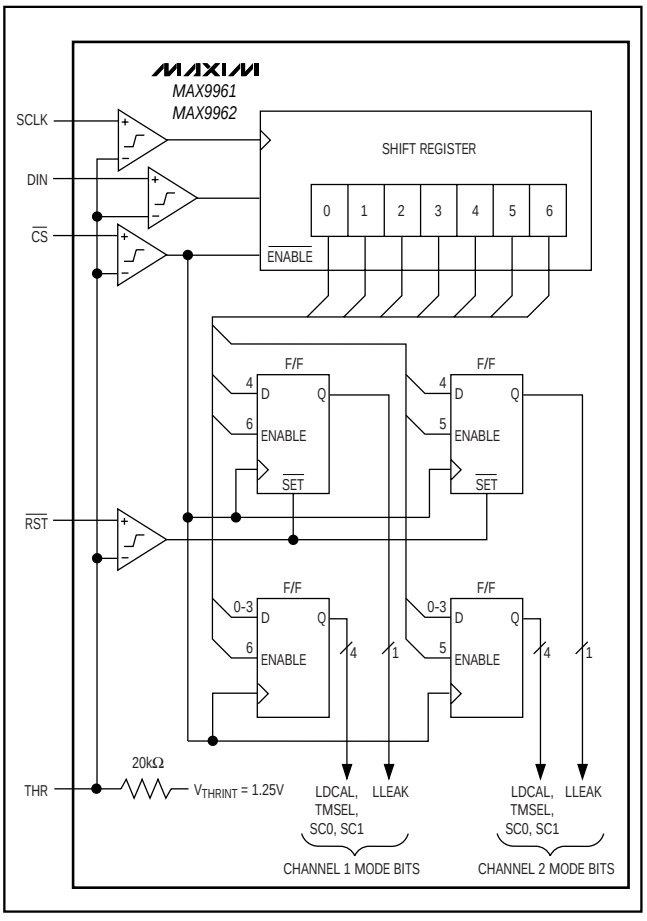


Figure 5. Serial Interface

Table 5. Shift Register Functions

BIT	NAME	DESCRIPTION
D6	CH1	Channel 1 Write Enable. Set to 1 to update the control byte for channel 1. Set to 0 to make no changes to channel 1.
D5	CH2	Channel 2 Write Enable. Set to 1 to update the control byte for channel 2. Set to 0 to make no changes to channel 2.
D4	LLEAK	Low-Leakage Select. Set to 1 to put driver, load, and clamps into low-leakage mode. Comparators remain active in low-leakage mode. Set to 0 for normal operation.
D3	TMSEL	Termination Select. Driver termination select bit. Set to 1 to force the driver output to the DTV_ voltage (term mode) when RCV_ = 1. Set to 0 to place the driver into high-impedance mode (high-Z) when RCV_ = 1. See Table 1.
D2	SC1	Driver Slew Rate Select. SC1 and SC0 set the driver slew rate. See Table 2.
D1	SC0	
D0	LDCAL	Load Calibrate. Overrides LDEN to enable load. Set LDCAL to 1 to enable load. Set LDCAL to 0 for normal operation. See Table 4.

Analog control input THR sets the threshold for the input logic, allowing operation with CMOS logic as low as 0.9V. Leaving THR unconnected results in a nominal threshold of 1.25V from an internal reference, providing compatibility with 2.5V to 3.3V logic.

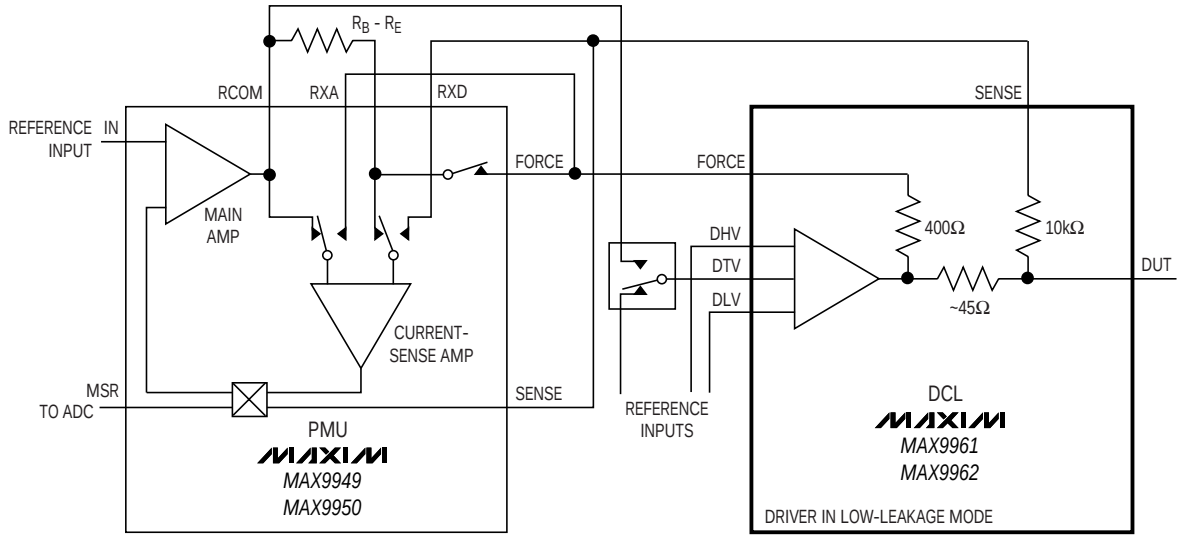
Temperature Monitor

The MAX9961/MAX9962 supply a temperature output signal, TEMP, that asserts a nominal output voltage of 3.43V at a die temperature of +70°C (343K). The output voltage increases with temperature at 10mV/°C.

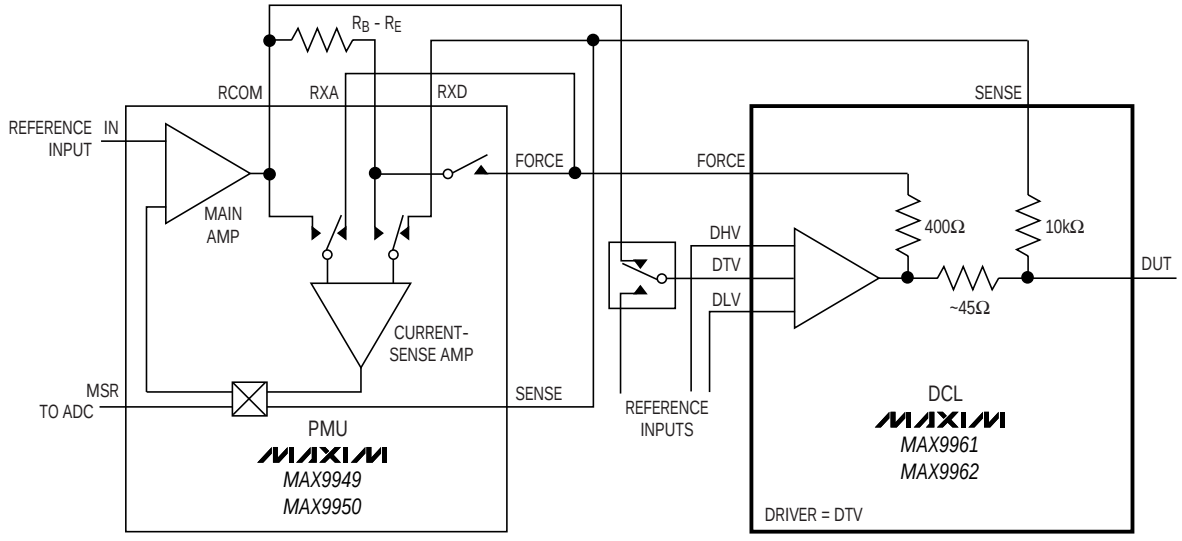
Heat Removal

Under normal circumstances, the MAX9961/MAX9962 require heat removal through the exposed pad by use of an external heat sink. The exposed pad is electrically at V_{EE} potential, and must be either connected to V_{EE} or isolated. The pad is located on the top of the MAX9961, and on the bottom of the MAX9962.

Typical Application Circuits (Simplified)



INTERFACING TO PMU WITHOUT EXTERNAL RELAYS. PMU SOURCING 2mA OR LESS.



INTERFACING TO PMU WITHOUT EXTERNAL RELAYS. DCL SOURCING UP TO 60mA.

Dual, Low-Power, 500Mbps ATE Drivers/Comparators with 2mA Load

Selector Guide

PART	ACCURACY GRADE	COMPARATOR OUTPUT TERMINATION	HIGH-SPEED DIGITAL INPUT TERMINATION	HEAT EXTRACTION
MAX9961ADCCQ	A	None	None	Top
MAX9961AGCCQ	A	None	100Ω with center tap	Top
MAX9961ALCCQ	A	50Ω to $V_{CCO\_}$	100Ω with center tap	Top
MAX9961BDCCQ	B	None	None	Top
MAX9961BGCCQ	B	None	100Ω with center tap	Top
MAX9961BLCCQ	B	50Ω to $V_{CCO\_}$	100Ω with center tap	Top
MAX9962ADCCQ	A	None	None	Bottom
MAX9962AGCCQ	A	None	100Ω with center tap	Bottom
MAX9962ALCCQ	A	50Ω to $V_{CCO\_}$	100Ω with center tap	Bottom
MAX9962BDCCQ	B	None	None	Bottom
MAX9962BGCCQ	B	None	100Ω with center tap	Bottom
MAX9962BLCCQ	B	50Ω to $V_{CCO\_}$	100Ω with center tap	Bottom

Chip Information

TRANSISTOR COUNT: 5130

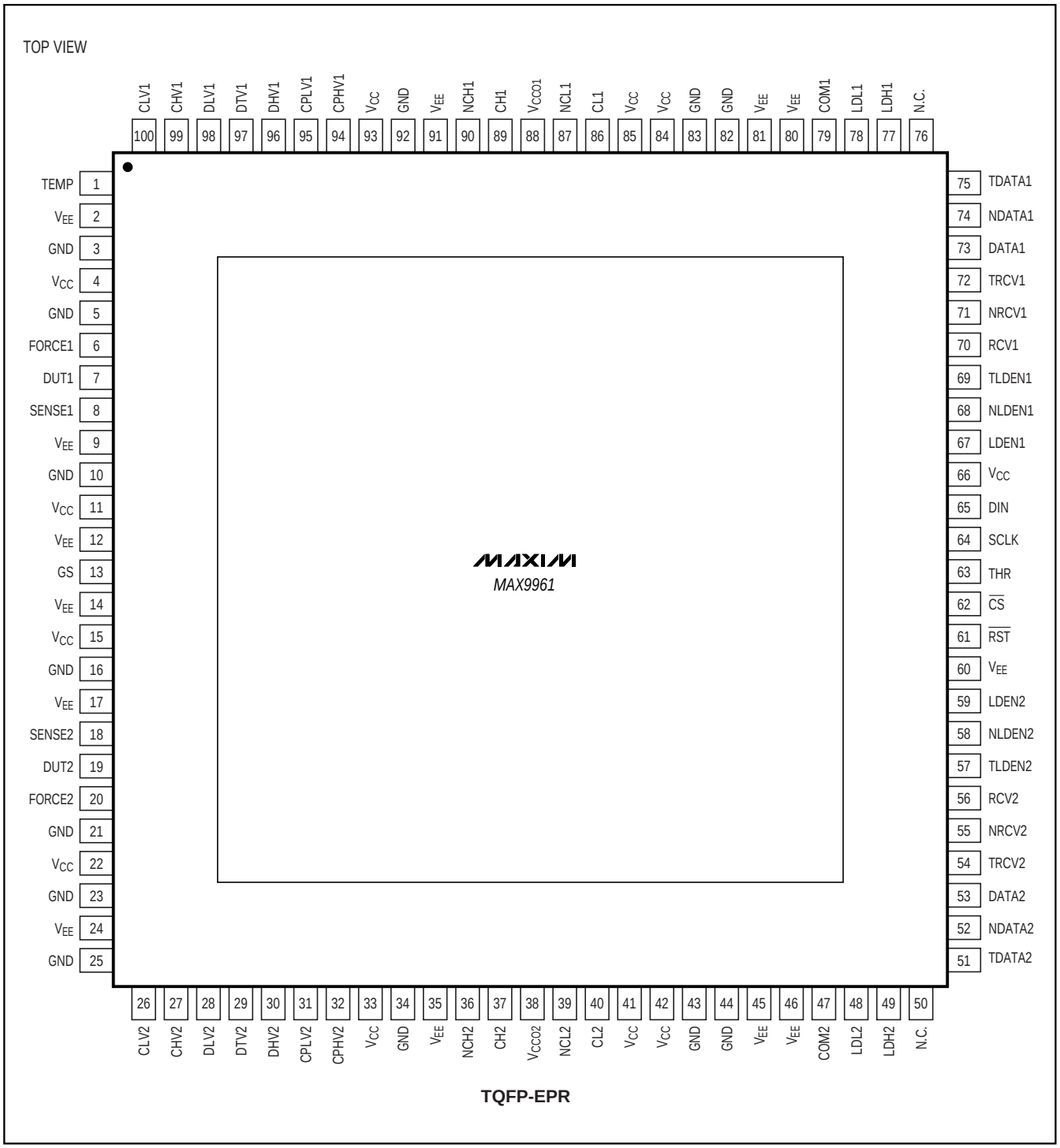
PROCESS: Bipolar

EXPOSED PAD: At V_{EE} potential; connect to V_{EE} or leave isolated.

Package Information

For the latest package outline information, go to **www.maxim-ic.com/packages**.

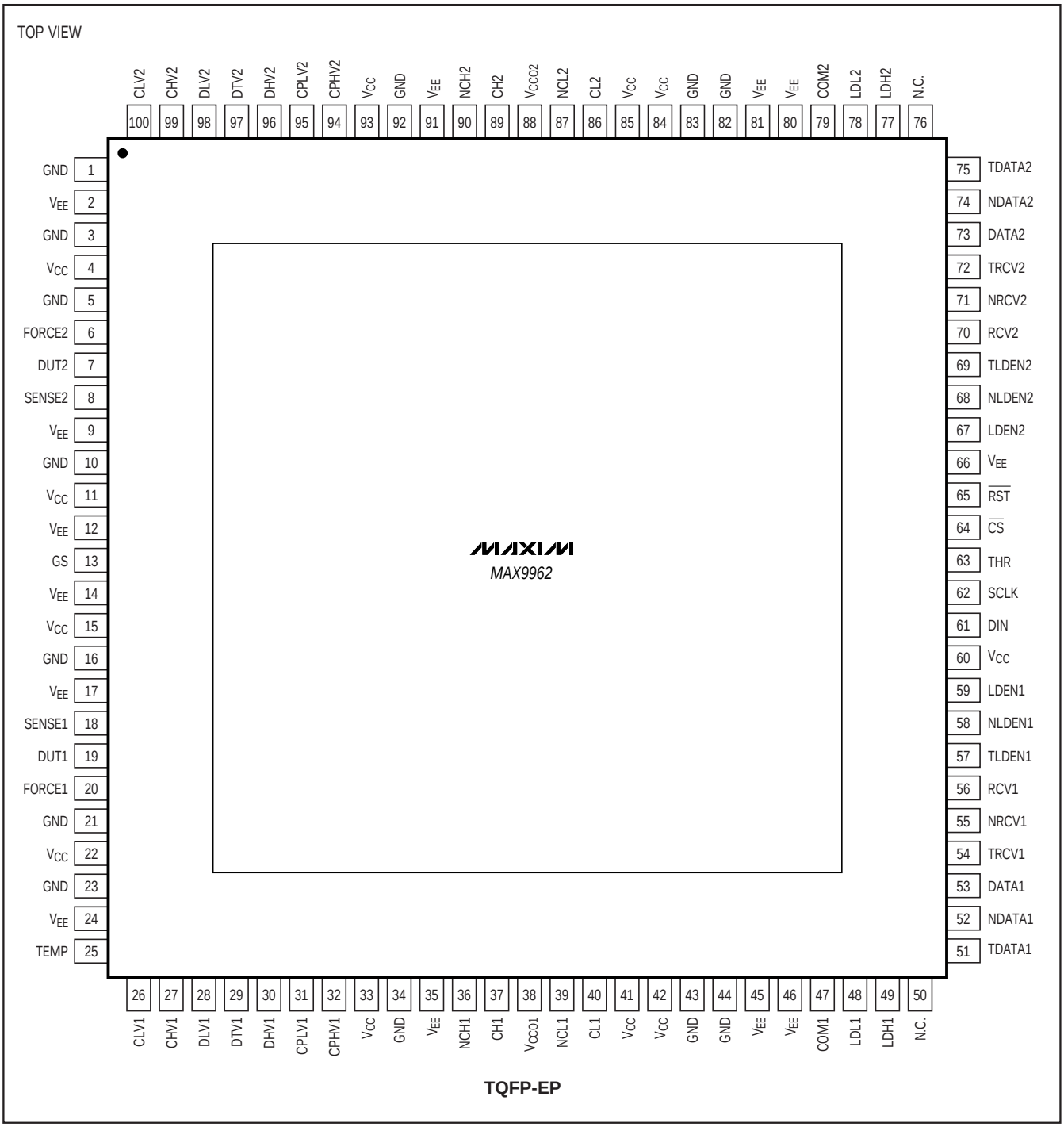
Pin Configurations



TQFP-EPR

Dual, Low-Power, 500Mbps ATE Drivers/Comparators with 2mA Load

Pin Configurations (continued)



TQFP-EP

MAX9961

Part Number Table

Notes:

1. See the MAX9961 QuickView Data Sheet for further information on this product family or download the MAX9961 full data sheet (PDF, 440kB).
2. Other options and links for purchasing parts are listed at: http://www.maxim-ic.com/sales.
3. Didn't Find What You Need? Ask our applications engineers. Expert assistance in finding parts, usually within one business day.
4. Part number suffixes: T or T&R = tape and reel; + = RoHS/lead-free; # = RoHS/lead-exempt. More: See full data sheet or Part Naming Conventions.
5. * Some packages have variations, listed on the drawing. "PkgCode/Variation" tells which variation the product uses.

Part Number	Free Sample	Buy Direct	Package: TYPE PINS SIZE DRAWING CODE/VAR *	Temp	RoHS/Lead-Free? Materials Analysis
MAX9961BLEVKIT					RoHS/Lead-Free: No
MAX9961BLCCQ+D				0C to +70C	RoHS/Lead-Free: Yes
MAX9961BDCCQ+TD				0C to +70C	RoHS/Lead-Free: Yes
MAX9961BDCCQ+D				0C to +70C	RoHS/Lead-Free: Yes
MAX9961ALCCQ+TD				0C to +70C	RoHS/Lead-Free: Yes
MAX9961ALCCQ+D				0C to +70C	RoHS/Lead-Free: Yes
MAX9961ADCCQ+TD				0C to +70C	RoHS/Lead-Free: Yes

MAX9961ADCCQ+D				0C to +70C	RoHS/Lead-Free: Yes
MAX9961BLCCQ-TD				0C to +70C	RoHS/Lead-Free: No
MAX9961BDCCQ-TD				0C to +70C	RoHS/Lead-Free: No
MAX9961ALCCQ-TD				0C to +70C	RoHS/Lead-Free: No
MAX9961ADCCQ-TD				0C to +70C	RoHS/Lead-Free: No
MAX9961BLCCQ+TD				0C to +70C	RoHS/Lead-Free: Yes
MAX9961BLCCQ-D			TQFP;100 pin;14x14x1mm Dwg: 21-0148A (PDF) Use pkgcode/variation: C100E-8R*	0C to +70C	RoHS/Lead-Free: No Materials Analysis
MAX9961BDCCQ-D			TQFP;100 pin;14x14x1mm Dwg: 21-0148A (PDF) Use pkgcode/variation: C100E-8R*	0C to +70C	RoHS/Lead-Free: No Materials Analysis
MAX9961ALCCQ-D			TQFP;100 pin;14x14x1mm Dwg: 21-0148A (PDF) Use pkgcode/variation: C100E-8R*	0C to +70C	RoHS/Lead-Free: No Materials Analysis
MAX9961ADCCQ-D			TQFP;100 pin;14x14x1mm Dwg: 21-0148A (PDF) Use pkgcode/variation: C100E-8R*	0C to +70C	RoHS/Lead-Free: No Materials Analysis

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