TOSHIBA Field-Effect Transistor Silicon P-Channel MOS Type (U-MOSVI)

# SSM6J503NU

### **Power Management Switch Applications**

1.5V drive

Low ON-resistance:  $R_{DS(ON)}$ = 89.6 m $\Omega$  (max) (@V<sub>GS</sub> = -1.5 V)

 $R_{DS(ON)} = 57.9 \text{ m}\Omega \text{ (max) (@V_{GS} = -1.8 V)}$ 

 $R_{DS(ON)} = 41.7 \text{ m}\Omega \text{ (max) (@V_{GS} = -2.5 V)}$ 

 $R_{DS(ON)} = 32.4 \text{ m}\Omega \text{ (max) (@V_{GS} = -4.5 V)}$ 

## Absolute Maximum Ratings (Ta = 25°C)

Charac	teristics	Symbol	Rating	Unit	
Drain-Source voltage		$V_{DSS}$	-20	V	
Gate-Source voltage		$V_{GSS}$	±8	V	
Drain current	DC	ID	-6.0	А	
	Pulse	I <sub>DP</sub> (Note 1)	-24.0		
Power Dissipation		P <sub>D</sub> (Note 2)	1	W	
		t ≦10s	2		
Channel temperature		T <sub>ch</sub>	150	°C	
Storage temperature		T <sub>stg</sub>	−55 to 150	°C	

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

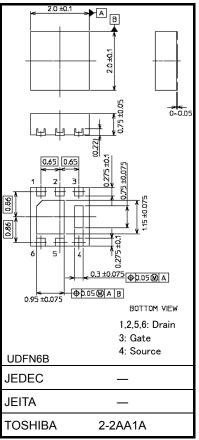
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling

Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1: The pulse width limited by max channel temperature.

Note 2: Mounted on an FR4 board.  $(25.4 \text{ mm} \times 25.4 \text{ mm} \times 1.6 \text{ mm}, \text{ Cu Pad: } 645 \text{ mm}^2)$ 

#### Unit: mm

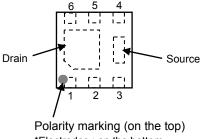


Weight: 8.5 mg (typ.)

## Marking(Top View)

# **Equivalent Circuit(Top View)**

# Pin Condition(Top View)



\*Electrodes: on the bottom

Polarity marking

# **Electrical Characteristics (Ta = 25°C)**

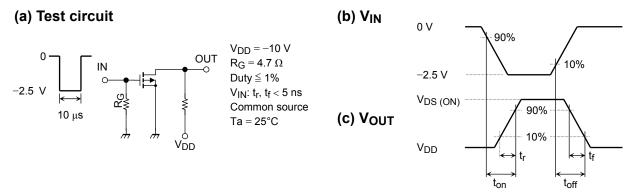
Chara	cteristic	Symbol	Test Conditions		Min	Тур.	Max	Unit
Drain-Source breakdown voltage		V (BR) DSS	$I_D = -1 \text{ mA}, V_{GS} = 0 \text{ V}$		-20	_	_	V
		V (BR) DSX	I <sub>D</sub> = -1 mA, V <sub>GS</sub> = 5 V	(Note 4)	-15	_	_	v
Drain cut-off current		I <sub>DSS</sub>	V <sub>DS</sub> = -20 V, V <sub>GS</sub> = 0 V		_	_	-1	μА
Gate leakage current		I <sub>GSS</sub>	$V_{GS} = \pm 8 \text{ V}, V_{DS} = 0 \text{ V}$		_	_	±1	μΑ
Gate threshold voltage		V <sub>th</sub>	$V_{DS} = -3 \text{ V}, I_{D} = -1 \text{ mA}$		-0.3	_	-1.0	V
Forward transfer admittance		Y <sub>fs</sub>	$V_{DS} = -3 \text{ V}, I_{D} = -1.0 \text{ A}$	(Note 3)	4.5	9.1	_	S
Drain-source ON-resistance			$I_D = -3.0 \text{ A}, V_{GS} = -4.5 \text{ V}$	(Note 3)	_	27.7	32.4	mΩ
		D	I <sub>D</sub> = -2.5 A, V <sub>GS</sub> = -2.5 V	(Note 3)	_	33.1	41.7	
		R <sub>DS</sub> (ON)	I <sub>D</sub> = -1.5 A, V <sub>GS</sub> = -1.8 V	(Note 3)	_	40.6	57.9	
			I <sub>D</sub> = -0.5 A, V <sub>GS</sub> = -1.5 V	(Note 3)	_	48.6	89.6	
Input capacitance		C <sub>iss</sub>			_	840	_	
Output capacitance		Coss	V <sub>DS</sub> = -10 V, V <sub>GS</sub> = 0 V, f = 1	_	118	_	pF	
Reverse transfer capacitance		C <sub>rss</sub>		_	99	_		
Total Gate Charge		Qg	$V_{DD} = -10 \text{ V}, I_D = -4.0 \text{ A}$ $V_{GS} = -4.5 \text{ V}$		_	12.8	_	nC
Gate-Source Charge		Q <sub>gs1</sub>			_	1.4	_	
Gate-Drain Charge		Q <sub>gd</sub>			_	3.0	_	
Switching time	Turn-on time	t <sub>on</sub>	V <sub>DD</sub> = -10 V, I <sub>D</sub> = -2.0 A,	_	32	_	no	
	Turn-off time	t <sub>off</sub>	$V_{GS} = 0$ to -2.5 V, $R_{G} = 4.7 \Omega$	!	_	107	_	ns
Drain-Source forward voltage		V <sub>DSF</sub>	I <sub>D</sub> = 4.0 A, V <sub>GS</sub> = 0 V	(Note 3)	_	0.78	1.2	٧

Note 3: Pulse test

Note 4: If a forward bias is applied between gate and source, this device enters  $V(BR)DSX \ mode$ .

Note that the drain-source breakdown voltage is lowered in this mode

## **Switching Time Test Circuit**



#### **Precaution**

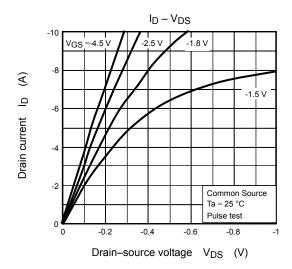
 $V_{th}$  can be expressed as voltage between gate and source when low operating current value is  $I_D$  = -1mA for this product. For normal switching operation,  $V_{GS}$  (on) requires higher voltage than  $V_{th}$  and  $V_{GS}$  (off) requires lower voltage than  $V_{th}$ .(Relationship can be established as follows:  $V_{GS}$  (off) <  $V_{th}$  <  $V_{GS}$  (on))

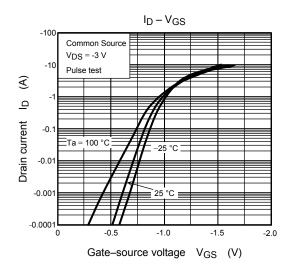
#### **Handling Precaution**

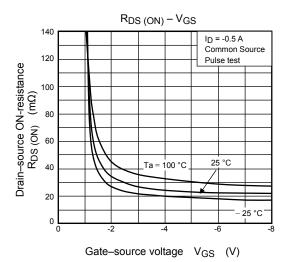
Please take this into consideration for using the device.

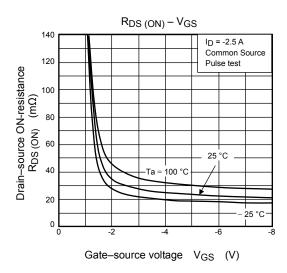
When handling individual devices that are not yet mounted on a circuit board, make sure that the environment is protected against electrostatic discharge. Operators should wear antistatic clothing, and containers and other objects that come into direct contact with devices should be made of antistatic materials.

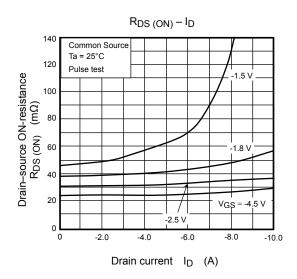
Thermal resistance  $R_{th\ (ch-a)}$  and power dissipation  $P_D$  vary depending on board material, board area, board thickness and pad area. When using this device, please take heat dissipation into consideration

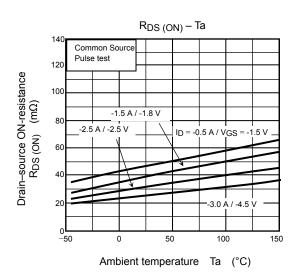


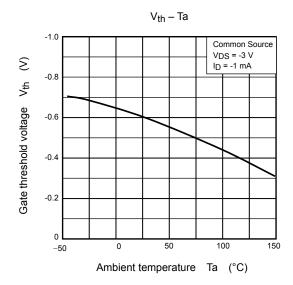


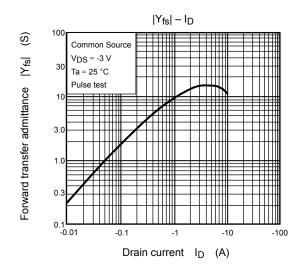


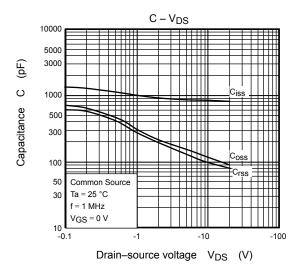


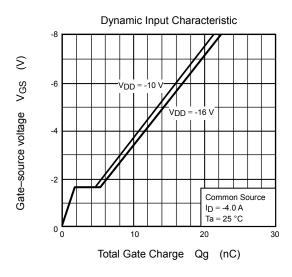


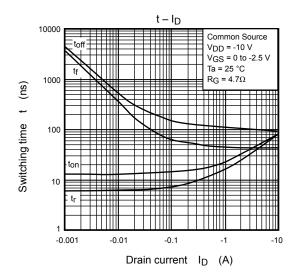


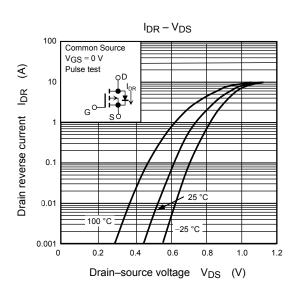


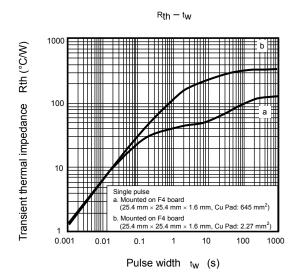


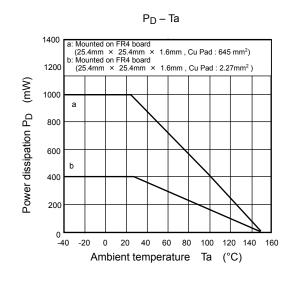












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