

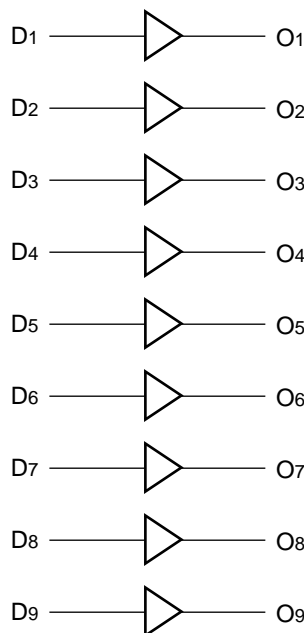
## FEATURES

- Max. propagation delay of 700ps
- IEE min. of -55mA
- Extended supply voltage option:  
VEE = -4.2V to -5.5V
- Voltage and temperature compensation for improved noise immunity
- Internal 75kΩ input pull-down resistors
- 70% faster than Fairchild 300K at lower power
- Function and pinout compatible with Fairchild F100K
- Available in 28-pin PLCC package

## DESCRIPTION

The SY100S322 is an ultra-fast buffer designed for use in high-performance ECL systems. The device provides nine non-inverting buffers with single-ended outputs. The inputs on the device have 75kΩ pull-down resistors.

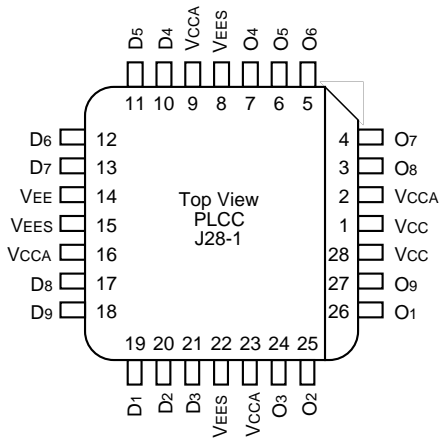
## BLOCK DIAGRAM



## PIN NAMES

Pin	Function
D1 – D9	Data Inputs
O1 – O9	Data Outputs
VEES	VEE Substrate
VCCA	Vcco for ECL Outputs

**PACKAGE/ORDERING INFORMATION**



**28-Pin PLCC (J28-1)**

**Ordering Information**

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY100S322JC	J28-1	Commercial	SY100S322JC	Sn-Pb
SY100S322JCTR <sup>(1)</sup>	J28-1	Commercial	SY100S322JC	Sn-Pb
SY100S322JZ <sup>(2)</sup>	J28-1	Commercial	SY100S322JZ with Pb-Free bar-line indicator	Matte-Sn
SY100S322JZTR <sup>(1, 2)</sup>	J28-1	Commercial	SY100S322JZ with Pb-Free bar-line indicator	Matte-Sn

**Notes:**

1. Tape and Reel.
2. Pb-Free package is recommended for new designs.

**LOGIC EQUATION**

$O_n = D_n, n = 1 \text{ to } 9$

**DC ELECTRICAL CHARACTERISTICS**

$V_{EE} = -4.2V \text{ to } -5.5V$  unless otherwise specified,  $V_{CC} = V_{CCA} = GND$

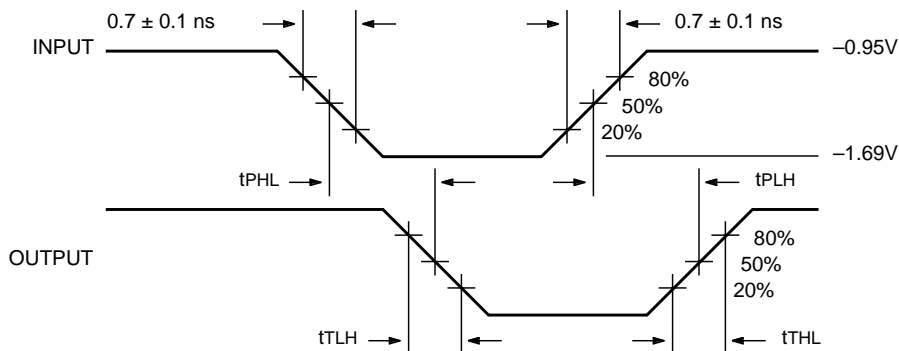
Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
$I_{IH}$	Input HIGH Current	—	—	200	$\mu A$	$V_{IN} = V_{IH} \text{ (Max.)}$
$I_{EE}$	Power Supply Current	-55	-41	-25	mA	Inputs Open

**AC ELECTRICAL CHARACTERISTICS**

$V_{EE} = -4.2V \text{ to } -5.5V$  unless otherwise specified,  $V_{CC} = V_{CCA} = GND$

Symbol	Parameter	$T_A = 0^\circ C$		$T_A = +25^\circ C$		$T_A = +85^\circ C$		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
$t_{PLH}$ $t_{PHL}$	Propagation Delay Data to Output	300	700	300	700	300	700	ps	
$t_{TLH}$ $t_{THL}$	Transition Time 20% to 80%, 80% to 20%	300	900	300	900	300	900	ps	

**TIMING DIAGRAM**

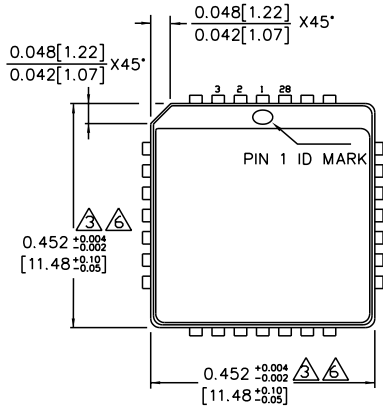


Propagation Delay and Transition Times

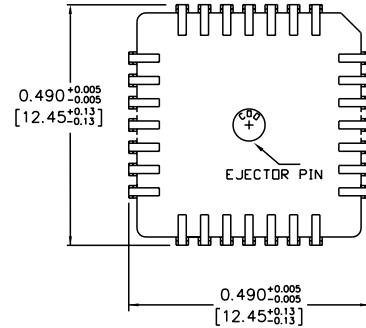
**Note:**

$V_{EE} = -4.2V \text{ to } -5.5V$  unless otherwise specified,  $V_{CC} = V_{CCA} = GND$

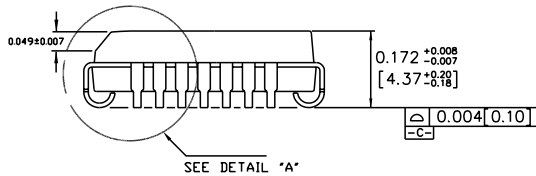
**28-PIN PLCC (J28-1)**



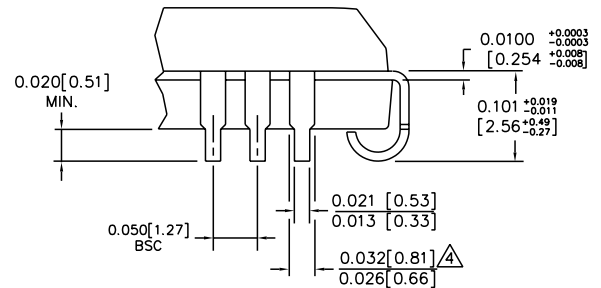
TOP VIEW



BOTTOM VIEW



SIDE VIEW



DETAIL "A"

NOTES:

1. DIMENSIONS ARE IN INCHES [MM].
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, EITHER OF WHICH SHALL NOT EXCEED 0.008 [0.203].
4. LEAD DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION.
5. MAXIMUM AND MINIMUM SPECIFICATIONS ARE INDICATED AS FOLLOWS: MAX/MIN
6. PACKAGE TOP DIMENSION MAY BE SLIGHTLY SMALLER THAN BOTTOM DIMENSION.

Rev. A

**MICREL, INC. 2180 FORTUNE DRIVE SAN JOSE, CA 95131 USA**

TEL + 1 (408) 944-0800 FAX + 1 (408) 474-1000 WEB <http://www.micrel.com>

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