0.5 Ω CMOS Dual 2:1 MUX/SPDT Audio Switch

ADG884

FEATURES

1.8 V to 5.5 V operation
Ultralow on resistance:
- **0.34 Ω typical**
- **0.38 Ω max at 5 V supply**

Excellent audio performance, ultralow distortion:
- **0.1 Ω typical**
- **0.15 Ω max R_{ON} flatness**

High current-carrying capability:
- **400 mA continuous**
- **600 mA peak current at 5 V supply**

Rail-to-rail switching operation
Typical power consumption (<0.1 μW)

APPLICATIONS

Cellular phones
PDAs
MP3 players
Power routing
Battery-powered systems
PCMCIA cards
Modems
Audio and video signal routing
Communications systems

FUNCTIONAL BLOCK DIAGRAM

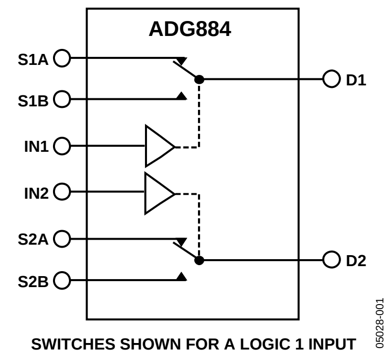

Figure 1.

GENERAL DESCRIPTION

The ADG884 is a low voltage CMOS device containing two independently selectable single-pole, double-throw (SPDT) switches. This device offers ultralow on resistance of less than 0.4 Ω over the full temperature range, making the part an ideal solution for applications that require minimal distortion through the switch. The ADG884 also has the capability of carrying large amounts of current, typically 600 mA at 5 V operation.

The ADG884 is available in a 10 bump, 2.0 mm × 1.50 mm WLCSP package, a 10-lead LFCSP package, and a 10-lead MSOP package. These tiny packages make the ADG884 the ideal solution for space-constrained applications.

When on, each switch conducts equally well in both directions and has an input signal range that extends to the supplies. The ADG884 exhibits break-before-make switching action.

PRODUCT HIGHLIGHTS

1. Single 1.8 V to 5.5 V operation.
2. High current handling capability (400 mA continuous current at 3.3 V).
3. 1.8 V logic-compatible.
4. Low THD + N (0.01% typ).
5. Tiny 2 mm × 1.5 mm WLCSP package and 3 mm × 3 mm 10-lead LFCSP package.

Table 1. ADG884 Truth Table

Logic (IN1/IN2)	Switch 1A/2A	Switch 1B/2B
0	Off	On
1	On	Off

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REVISION HISTORY

10/04—Revision 0: Initial Version

SPECIFICATIONS

V_{DD} = 5 V ± 10%, GND = 0 V, unless otherwise noted.[1]

Table 2.

Parameter	25°C	−40°C to +85°C	Unit	Test Conditions/Comments
ANALOG SWITCH				
Analog Signal Range		0 V to V_{DD}	V	
On Resistance, R_{ON}	0.28		Ω typ	V_{DD} = 4.5 V, V_S = 0 V to V_{DD}, I_S = 100 mA
	0.34	0.38	Ω max	See Figure 18
On Resistance Match Between	0.01		Ω typ	V_{DD} = 4.5 V, V_S = 2 V, I_S = 100 mA
Channels, ΔR_{ON}	0.035	0.05	Ω max	
On Resistance Flatness, R_{FLAT} (ON)	0.1		Ω typ	V_{DD} = 4.5 V, V_S = 0 V to V_{DD}
	0.13	0.15	Ω max	I_S = 100 mA
LEAKAGE CURRENTS				V_{DD} = 5.5 V
Source Off Leakage, I_S (OFF)	±0.2		nA typ	V_S = 0.6 V/4.5 V, V_D = 4.5 V/0.6 V; Figure 19
Channel On Leakage, I_D, I_S (ON)	±0.2		nA typ	V_S = V_D = 0.6 V or 4.5 V; Figure 20
DIGITAL INPUTS				
Input High Voltage, V_{INH}		2.0	V min	
Input Low Voltage, V_{INL}		0.8	V max	
Input Current, I_{INL} or I_{INH}	0.005		μA typ	V_{IN} = V_{INL} or V_{INH}
		±0.1	μA max	
Digital Input Capacitance, C_{IN}	2		pF typ	
DYNAMIC CHARACTERISTICS[2]				
t_{ON}	42		ns typ	R_L = 50 Ω, C_L = 35 pF
	50	53	ns max	V_S = 3 V/0 V; Figure 21
t_{OFF}	15		ns typ	R_L = 50 Ω, C_L = 35 pF
	20	21	ns max	V_S = 3 V; Figure 21
Break-Before-Make Time Delay, t_{BBM}	16		ns typ	R_L = 50 Ω, C_L = 35 pF
		10	ns min	V_{S1} = V_{S2} = 1.5 V; Figure 22
Charge Injection	125		pC typ	V_S = 1.5 V, R_S = 0 Ω, C_L = 1 nF; Figure 23
Off Isolation	−60		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 100 kHz; Figure 24
Channel-to-Channel Crosstalk	−120		dB typ	S1A−S2A/S1B−S2B; R_L = 50 Ω, C_L = 5 pF, f = 100 kHz; Figure 27
	−60		dB typ	S1A−S1B/S2A−S2B; R_L = 50 Ω, C_L = 5 pF, f = 100 kHz; Figure 26
Total Harmonic Distortion, THD + N	0.017		%	R_L = 32 Ω, f = 20 Hz to 20 kHz, V_S = 3.5 V p-p
Insertion Loss	−0.03		dB typ	R_L = 50 Ω, C_L = 5 pF; Figure 25
−3 dB Bandwidth	18		MHz typ	R_L = 50 Ω, C_L = 5 pF; Figure 25
C_S (OFF)	103		pF typ	
C_D, C_S (ON)	295		pF typ	
POWER REQUIREMENTS				V_{DD} = 5.5 V
I_{DD}	0.003		μA typ	Digital Inputs = 0 V or 5.5 V
		1	μA max	

[1] Temperature range of the B version is −40°C to +85°C.
[2] Guaranteed by design, not subject to production test.

V_{DD} = 3.4 V to 4.2 V; GND = 0 V, unless otherwise noted.[1]

Table 3.

Parameter	25°C	−40°C to +85°C	Unit	Test Conditions/Comments
ANALOG SWITCH				
Analog Signal Range		0 V to V_{DD}	V	
On Resistance, R_{ON}	0.33		Ω typ	V_{DD} = 3.4 V, V_S = 0 V to V_{DD}, I_S = 100 mA
	0.38	0.45	Ω max	See Figure 18
On Resistance Match Between	0.013		Ω typ	V_{DD} = 3.4 V, V_S = 2 V, I_S = 100 mA
Channels, ΔR_{ON}	0.042	0.065	Ω max	
On Resistance Flatness, R_{FLAT} (ON)	0.13		Ω typ	V_{DD} = 3.4 V, V_S = 0 V to V_{DD}
	0.155	0.175	Ω max	I_S = 100 mA
LEAKAGE CURRENTS				V_{DD} = 4.2 V
Source Off Leakage, I_S (OFF)	±0.2		nA typ	V_S = 0.6 V/3.9 V, V_D = 3.9 V/0.6 V; Figure 19
Channel On Leakage, I_D, I_S (ON)	±0.2		nA typ	V_S = V_D = 0.6 V or 3.9 V; Figure 20
DIGITAL INPUTS				
Input High Voltage, V_{INH}		2.0	V min	
Input Low Voltage, V_{INL}		0.8	V max	
Input Current, I_{INL} or I_{INH}	0.005		µA typ	V_{IN} = V_{INL} or V_{INH}
		±0.1	µA max	
Digital Input Capacitance, C_{IN}	2		pF typ	
DYNAMIC CHARACTERISTICS[2]				
t_{ON}	42		ns typ	R_L = 50 Ω, C_L = 35 pF
	50	54	ns max	V_S = 1.5 V/0 V; Figure 21
t_{OFF}	15		ns typ	R_L = 50 Ω, C_L = 35 pF
	21	24	ns max	V_S = 1.5 V; Figure 21
Break-Before-Make Time Delay, t_{BBM}	17		ns typ	R_L = 50 Ω, C_L = 35 pF
		10	ns min	V_{S1} = V_{S2} = 1.5 V; Figure 22
Charge Injection	100		pC typ	V_S = 1.5 V, R_S = 0 Ω, C_L = 1 nF; Figure 23
Off Isolation	−60		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 100 kHz; Figure 24
Channel-to-Channel Crosstalk	−120		dB typ	S1A–S2A/S1B–S2B; R_L = 50 Ω, C_L = 5 pF, f = 100 kHz; Figure 27
	−60		dB typ	S1A–S1B/S2A–S2B; R_L = 50 Ω, C_L = 5 pF, f = 100 kHz; Figure 26
Total Harmonic Distortion, THD + N	0.01		%	R_L = 32 Ω, f = 20 Hz to 20 kHz, V_S = 2 V p-p
Insertion Loss	−0.03		dB typ	R_L = 50 Ω, C_L = 5 pF; Figure 25
−3 dB Bandwidth	18		MHz typ	R_L = 50 Ω, C_L = 5 pF; Figure 25
C_S (OFF)	110		pF typ	
C_D, C_S (ON)	300		pF typ	
POWER REQUIREMENTS				V_{DD} = 4.2 V
I_{DD}	0.003		µA typ	Digital Inputs = 0 V or 4.2 V
		1	µA max	

[1] Temperature range of the B version is −40°C to +85°C.
[2] Guaranteed by design, not subject to production test.

V_{DD} = 2.7 V to 3.6 V, GND = 0 V, unless otherwise noted.[1]

Table 4.

Parameter	25°C	−40°C to +85°C	Unit	Test Conditions/Comments
ANALOG SWITCH				
Analog Signal Range		0 V to V_{DD}	V	
On Resistance, R_{ON}	0.4		Ω typ	V_{DD} = 2.7 V, V_S = 0 V to V_{DD}
	0.5	0.6	Ω max	I_S = 100 mA; Figure 18
On Resistance Match Between	0.02		Ω typ	V_{DD} = 2.7 V, V_S = 0.6 V
Channels, ΔR_{ON}	0.07	0.1	Ω max	I_S = 100 mA
On Resistance Flatness, R_{FLAT} (ON)	0.18		Ω typ	V_{DD} = 2.7 V, V_S = 0 V to V_{DD}
		0.25	Ω max	I_S = 100 mA
LEAKAGE CURRENTS				V_{DD} = 3.6 V
Source Off Leakage, I_S (OFF)	±0.2		nA typ	V_S = 0.6 V/3.3 V, V_D = 3.3 V/0.6 V, Figure 19
Channel On Leakage, I_D, I_S (ON)	±0.2		nA typ	V_S = V_D = 0.6 V or 3.3 V; Figure 20
DIGITAL INPUTS				
Input High Voltage, V_{INH}		1.3	V min	
Input Low Voltage, V_{INL}		0.8	V max	
Input Current, I_{INL} or I_{INH}	0.005		μA typ	V_{IN} = V_{INL} or V_{INH}
		±0.1	μA max	
Digital Input Capacitance, C_{IN}	2		pF typ	
DYNAMIC CHARACTERISTICS[2]				
t_{ON}	42		ns typ	R_L = 50 Ω, C_L = 35 pF
	56	62	ns max	V_S = 1.5 V/0 V; Figure 21
t_{OFF}	14		ns typ	R_L = 50 Ω, C_L = 35 pF
	19	21	ns max	V_S = 1.5 V; Figure 21
Break-Before-Make Time Delay, t_{BBM}	24		ns typ	R_L = 50 Ω, C_L = 35 pF
		10	ns min	V_{S1} = V_{S2} = 1.5 V; Figure 22
Charge Injection	85		pC typ	V_S = 1.25 V, R_S = 0 Ω, C_L = 1 nF; Figure 23
Off Isolation	−60		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 100 kHz; Figure 24
Channel-to-Channel Crosstalk	−120		dB typ	S1A–S2A/S1B–S2B; R_L = 50 V, C_L = 5 pF, f = 100 kHz; Figure 27
	−60		dB typ	S1A–S1B/S2A–S2B; R_L = 50 Ω, C_L = 5 pF, f = 100 kHz; Figure 25
Total Harmonic Distortion, THD + N	0.03		%	R_L = 32 Ω, f = 20 Hz to 20 kHz, V_S = 1.5 V p-p
Insertion Loss	−0.03		dB typ	R_L = 50 Ω, C_L = 5 pF; Figure 25
−3 dB Bandwidth	18		MHz typ	R_L = 50 Ω, C_L = 5 pF; Figure 25
C_S (OFF)	110		pF typ	
C_D, C_S (ON)	300		pF typ	
POWER REQUIREMENTS				V_{DD} = 3.6 V
I_{DD}	0.003		μA typ	Digital Inputs = 0 V or 3.6 V
		1	μA max	

[1] Temperature range of the B version is −40°C to +85°C.
[2] Guaranteed by design, not subject to production test.

ABSOLUTE MAXIMUM RATINGS

TA = 25°C, unless otherwise noted.

Table 5.

Parameter	Rating
V_{DD} to GND	−0.3 V to +6 V
Analog Inputs[1]	−0.3 V to V_{DD} + 0.3 V
Digital Inputs[1]	−0.3 V to 6 V or 10 mA (whichever occurs first)
Peak Current, S or D	
5 V Operation	600 mA mA (pulsed at 1 ms, 10% duty cycle max)
Continuous Current, S or D	
5 V Operation	400 mA
Operating Temperature Range	
Industrial (B Version)	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
10-Lead MSOP Package	
θ_{JA} Thermal Impedance	206°C/W
θ_{JC} Thermal Impedance	44°C/W
10-Lead WLCSP Package (4-Layer Board)	
θ_{JA} Thermal Impedance	120 °C/W
10-Lead LFCSP Package (4-Layer Board)	
θ_{JA} Thermal Impedance	76 °C/W
θ_{JC} Thermal Impedance	13.5 °C/W
IR Reflow, Peak Temperature <20 s	235°C

[1] Overvoltages at IN, S, or D are clamped by internal diodes. Current should be limited to the maximum ratings given.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Only one absolute maximum rating may be applied at any one time.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

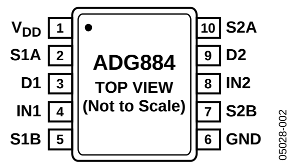

Figure 2. LFCSP and MSOP Pin Configuration

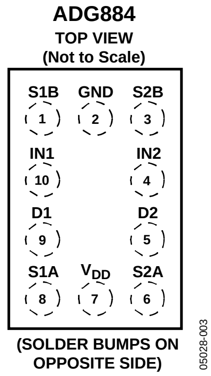

Figure 3. WLCSP Pin Configuration

Table 6. Pin Function Descriptions

Pin No.			
LFCSP, MSOP	**WLCSP**	**Mnemonic**	**Description**
1	7	V_{DD}	Most Positive Power Supply Potential.
2, 5, 10, 7	6, 3, 8, 1	S1A, S1B, S2A, S2B	Source Terminal. May be an input or output.
3, 9	5, 9	D1, D2	Drain Terminal. May be an input or output.
4, 8	4, 10	IN1, IN2	Logic Control Input.
6	2	GND	Ground (0 V) Reference.

TYPICAL PERFORMANCE CHARACTERISTICS

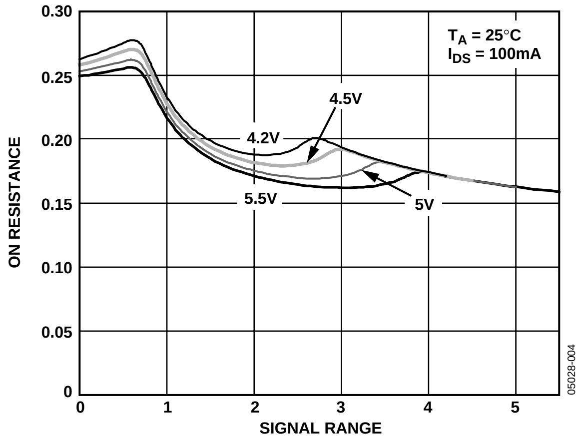

Figure 4. On Resistance vs. V_D (V_S), V_{DD} = 4.2 V to 5.5 V

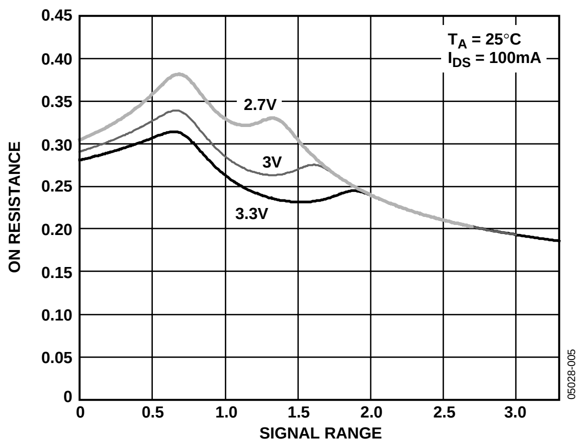

Figure 5. On Resistance vs. V_D (V_S), V_{DD} = 2.7 V to 3.3 V

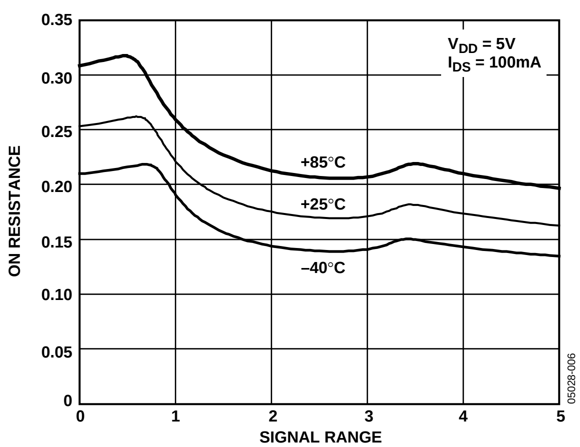

Figure 6. On Resistance vs. V_D (V_S) for Different Temperature, V_{DD} = 5 V

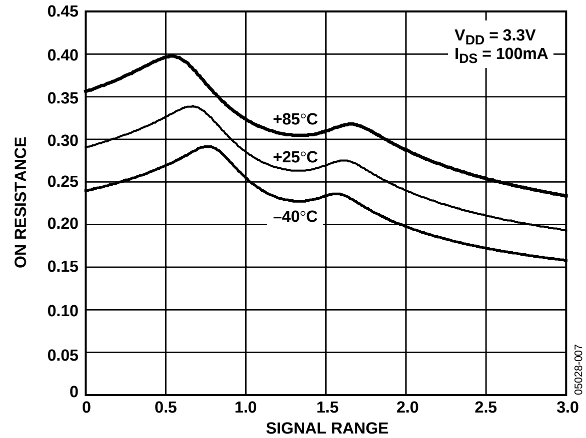

Figure 7. On Resistance vs. V_D (V_S) for Different Temperature, V_{DD} = 3.3 V

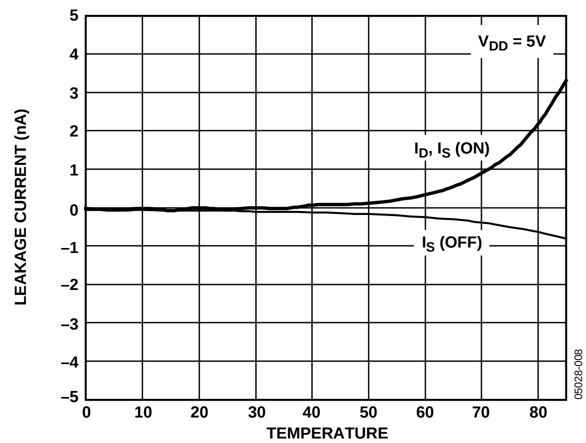

Figure 8. Leakage Current vs. Temperature, V_{DD} = 5 V

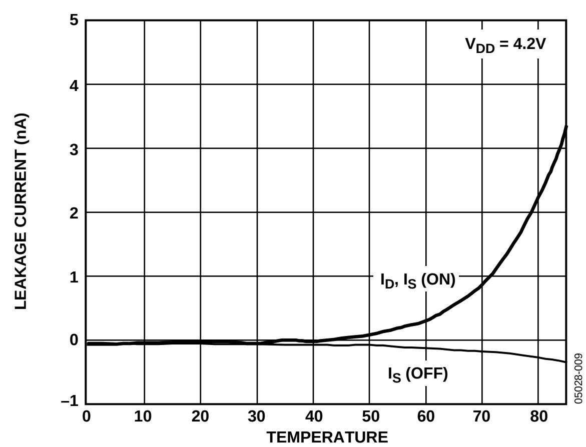

Figure 9. Leakage Current vs. Temperature, V_{DD} = 4.2 V

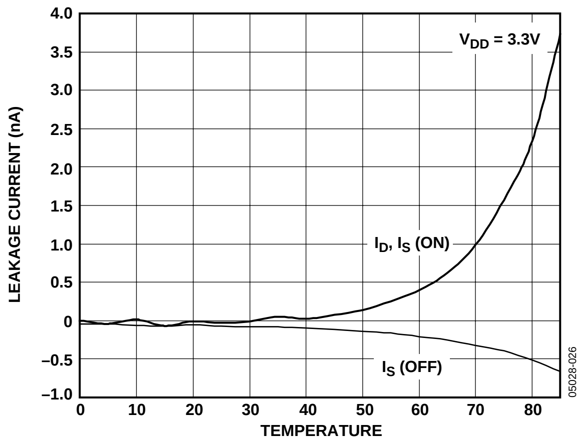

Figure 10. Leakage Current vs. Temperature, V_{DD} = 3.3 V

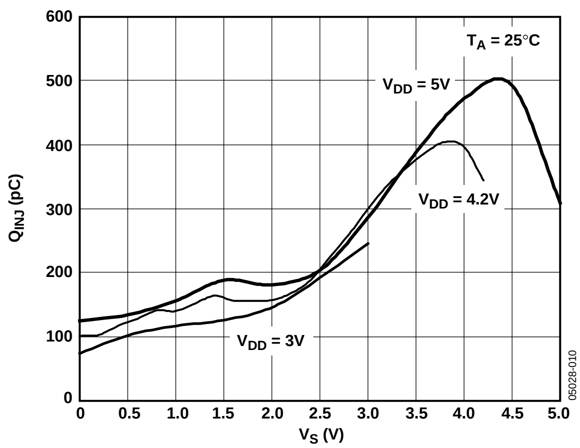

Figure 11. Charge Injection vs. Source Voltage

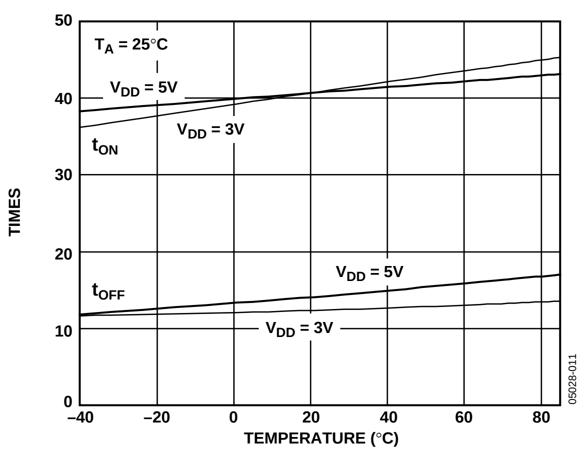

Figure 12. t_{ON}/t_{OFF} Times vs. Temperature

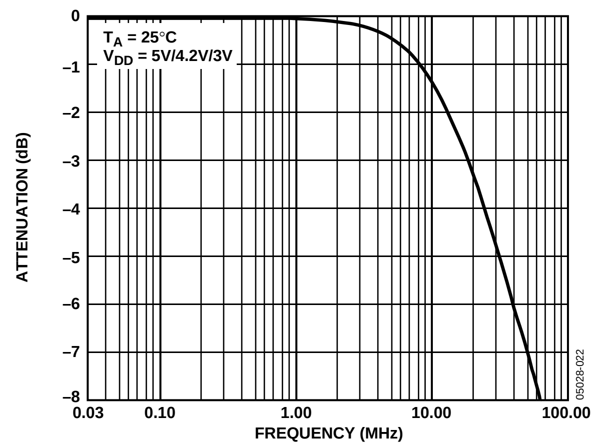

Figure 13. Bandwidth

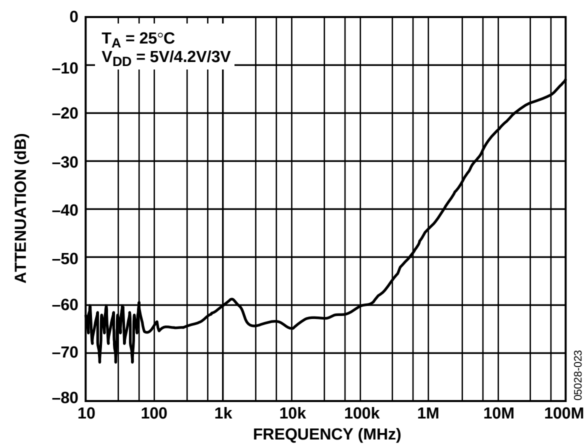

Figure 14. Off Isolation vs. Frequency

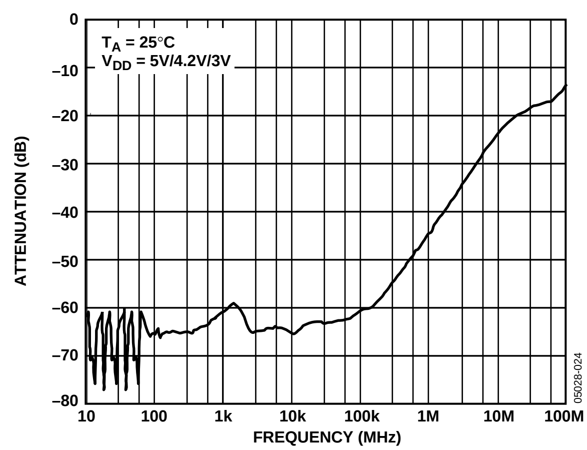

Figure 15. Crosstalk vs. Frequency

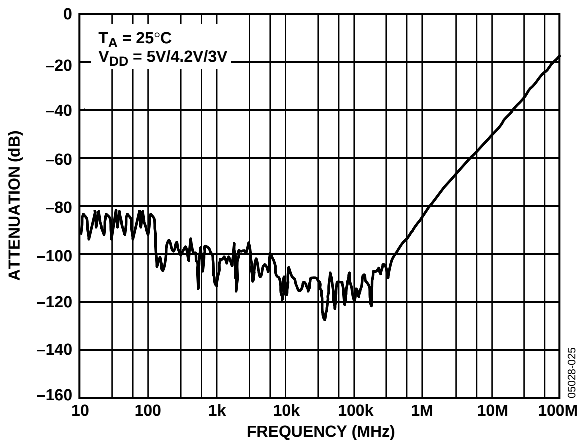

Figure 16. AC PSRR

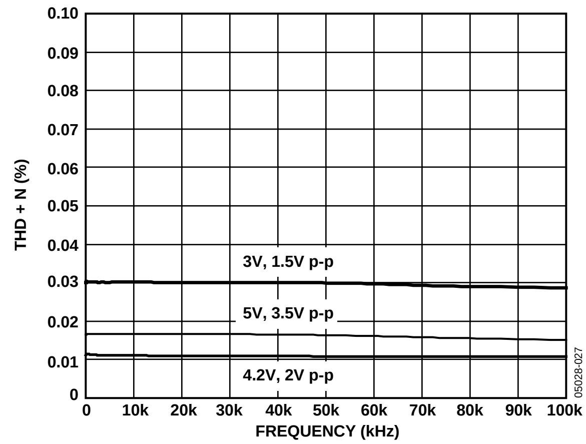

Figure 17. THD + N

TERMINOLOGY

I_{DD}
Positive supply current.

V_D (V_S)
Analog voltage on Terminals D, S.

R_{ON}
Ohmic resistance between D and S.

R_{FLAT} (ON)
The difference between the maximum and minimum values of on resistance as measured on the switch.

ΔR_{ON}
On resistance match between any two channels.

I_S (OFF)
Source leakage current with the switch off.

I_D (OFF)
Drain leakage current with the switch off.

I_D, I_S (ON)
Channel leakage current with the switch on.

V_{INL}
Maximum input voltage for Logic 0.

V_{INH}
Minimum input voltage for Logic 1.

I_{INL} (I_{INH})
Input current of the digital input.

C_S (OFF)
Off switch source capacitance. Measured with reference to ground.

C_D (OFF)
Off switch drain capacitance. Measured with reference to ground.

C_D, C_S (ON)
On switch capacitance. Measured with reference to ground.

C_{IN}
Digital input capacitance.

t_{ON}
Delay time between the 50% and 90% points of the digital input and switch on condition.

t_{OFF}
Delay time between the 50% and 90% points of the digital input and switch off condition.

t_{BBM}
On or off time measured between the 80% points of both switches when switching from one to another.

Charge Injection
Measure of the glitch impulse transferred from the digital input to the analog output during on-off switching.

Off Isolation
Measure of unwanted signal coupling through an off switch.

Crosstalk
Measure of unwanted signal that is coupled through from one channel to another as a result of parasitic capacitance.

−3 dB Bandwidth
Frequency at which the output is attenuated by 3 dB.

On Response
Frequency response of the on switch.

Insertion Loss
The loss due to the on resistance of the switch.

THD + N
Ratio of the harmonics amplitude plus noise of a signal to the fundamental.

TEST CIRCUITS

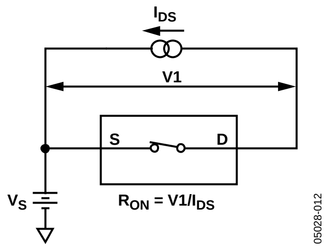

Figure 18. On Resistance

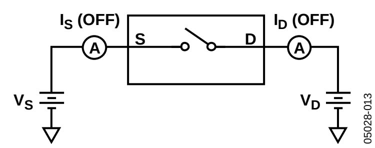

Figure 19. Off Leakage

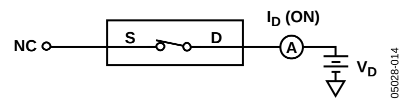

Figure 20. On Leakage

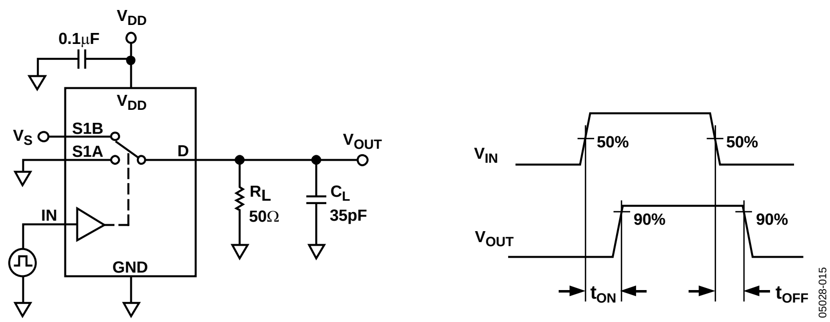

Figure 21. Switching Times, t_{ON}, t_{OFF}

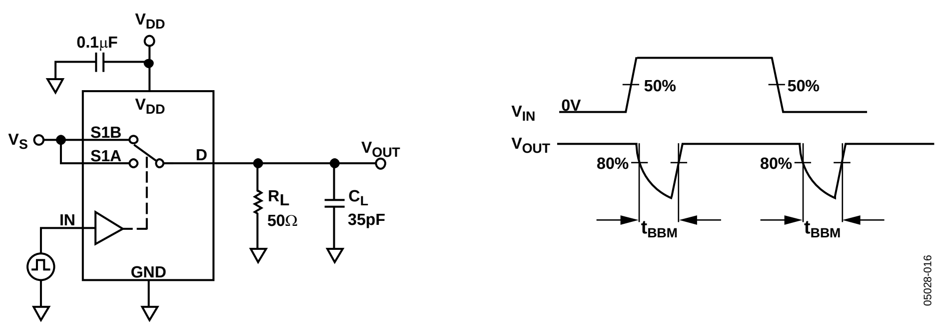

Figure 22. Break-Before-Make Time Delay, t_{BBM}

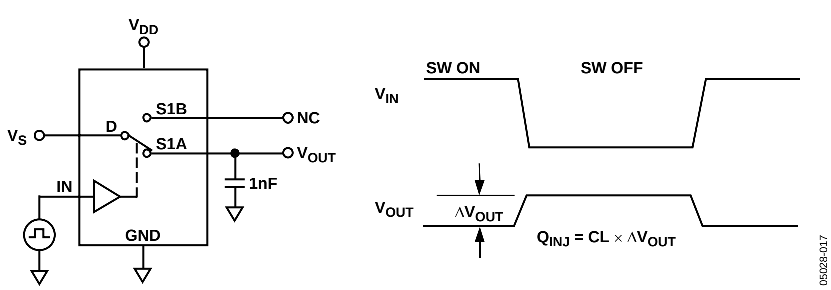

Figure 23. Charge Injection

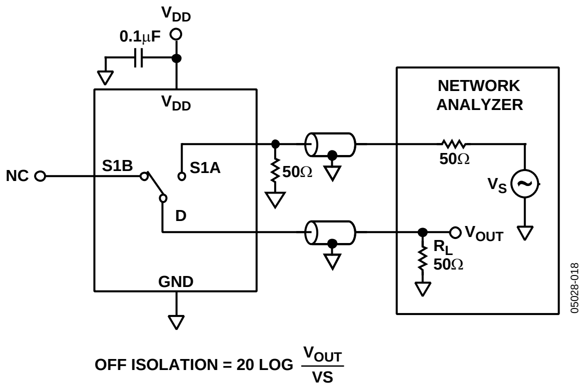

Figure 24. Off Isolation

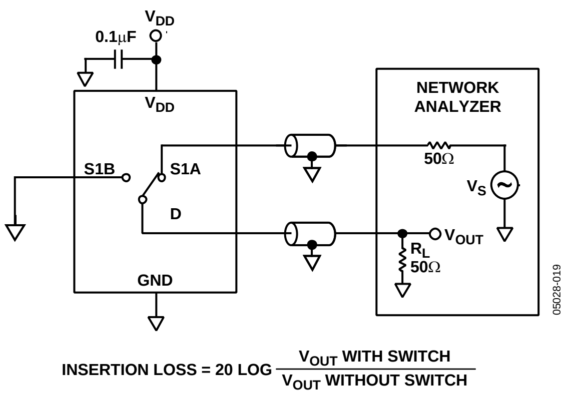

Figure 25. Channel-to-Channel Crosstalk (S1A–S1B)

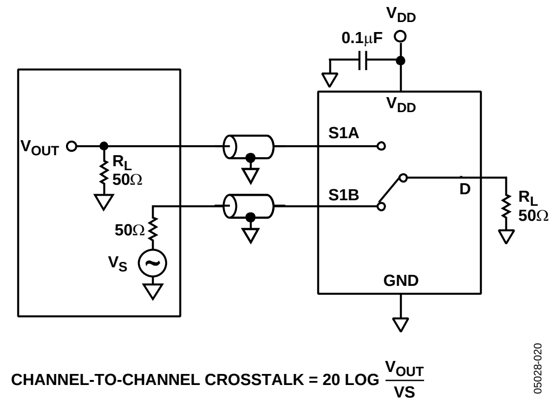

Figure 26. Bandwidth

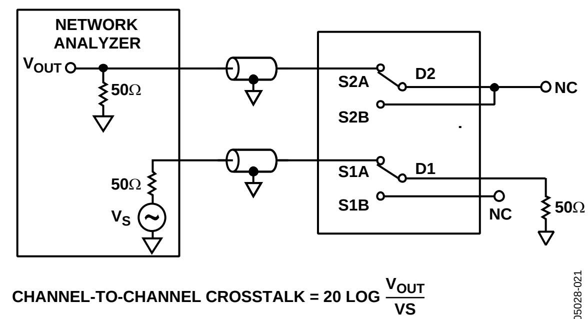

Figure 27. Channel-to-Channel Crosstalk (S1A–S2A)

OUTLINE DIMENSIONS

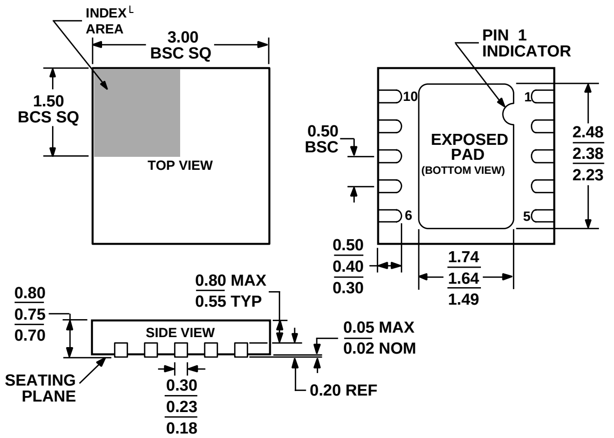

Figure 28. 10-Lead Lead Frame Chip Scale Package [LFCSP]
3 mm × 3 mm Body
(CP-10-9)
Dimensions shown in millimeters

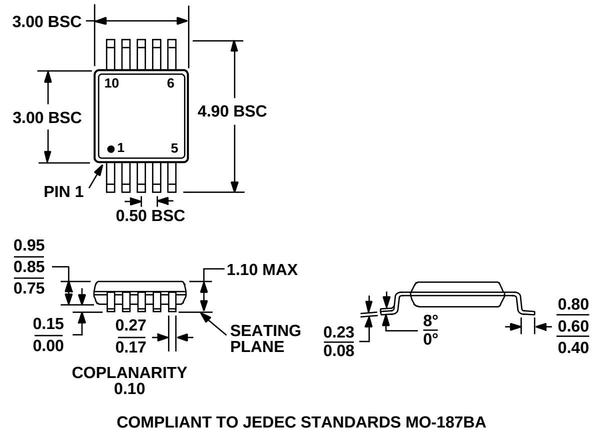

Figure 29. 10-Lead Mini Small Outline Package [MSOP]
(RM-10)
Dimensions shown in millimeters

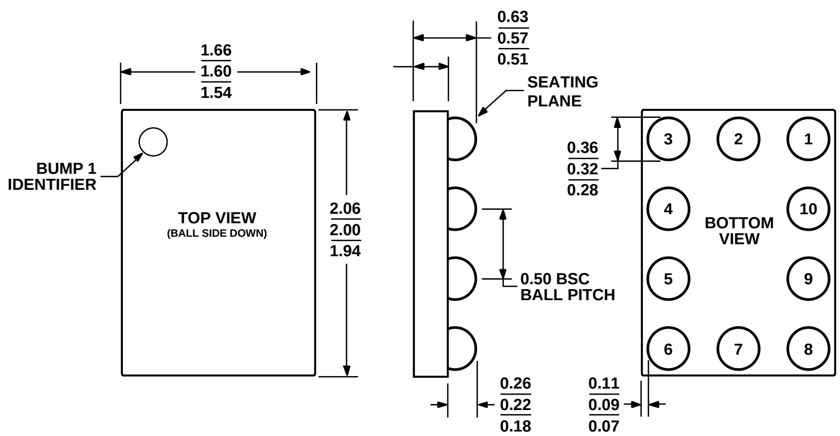

Figure 30. 10-Ball Wafer Level Chip Scale Package [WLCSP]
(CB-10)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option	Branding[1]
ADG884BRMZ[2]	−40°C to +85°C	Mini Small Outline Package (MSOP)	RM-10	S9C
ADG884BRMZ-REEL[2]	−40°C to +85°C	Mini Small Outline Package (MSOP)	RM-10	S9C
ADG884BRMZ-REEL7[2]	−40°C to +85°C	Mini Small Outline Package (MSOP)	RM-10	S9C
ADG884BCPZ-REEL[2]	−40°C to +85°C	Lead Frame Chip Scale Package (LFCSP)	CP-10-9	S9C
ADG884BCPZ-REEL7[2]	−40°C to +85°C	Lead Frame Chip Scale Package (LFCSP)	CP-10-9	S9C
ADG884BCB-500RL7	−40°C to +85°C	Micro Chip Scale Package (WLCSP)	CB-10	S9C
ADG884BCB-REEL	−40°C to +85°C	Micro Chip Scale Package (WLCSP)	CB-10	S9C
ADG884BCB-REEL7	−40°C to +85°C	Micro Chip Scale Package (WLCSP)	CB-10	S9C
ADG884BCBZ[2]	−40°C to +85°C	Micro Chip Scale Package (WLCSP)	CB-10	S9C

[1] Branding on this package is limited to three characters due to space constraints.
[2] Z = Pb-free package.

NOTES

D05028-0-10/04(0)