Pb Free Plating Product

# GTM CORPORATION

ISSUED DATE :2006/04/24
REVISED DATE :

# GSS6982

**DUAL N-CHANNEL ENHANCEMENT MODE POWER MOSFET**

| | | |
|---|---|---|
| CH1 | $BV_{DSS}$ | 30V |
| | $R_{DS(ON)}$ | 18mΩ |
| | $I_D$ | 8.5A |
| CH2 | $BV_{DSS}$ | 30V |
| | $R_{DS(ON)}$ | 26mΩ |
| | $I_D$ | 7.3A |

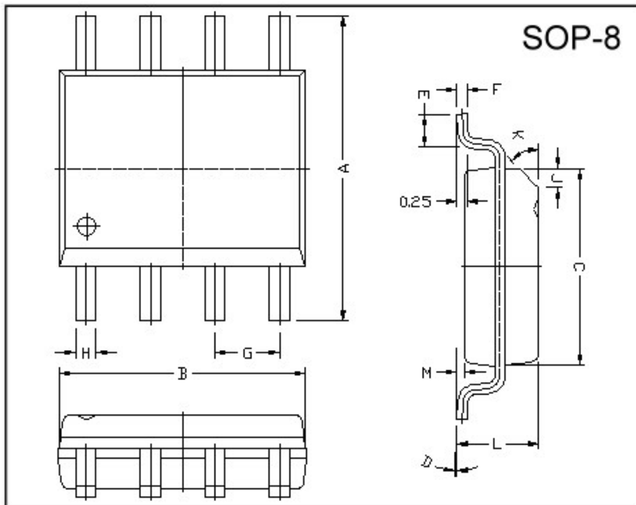
## Description

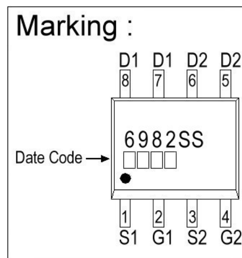
The GSS6982 provide the designer with the best combination of fast switching, ruggedized device design, ultra low on-resistance and cost-effectiveness.

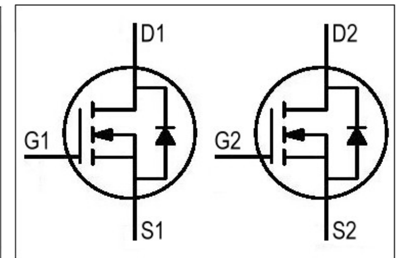
## Features

*Low On-resistance
*Fast Switching

## Package Dimensions




| REF. | Millimeter Min. | Millimeter Max. | REF. | Millimeter Min. | Millimeter Max. |
|---|---|---|---|---|---|
| A | 5.80 | 6.20 | M | 0.10 | 0.25 |
| B | 4.80 | 5.00 | H | 0.35 | 0.49 |
| C | 3.80 | 4.00 | L | 1.35 | 1.75 |
| D | 0° | 8° | J | 0.375 REF. | |
| E | 0.40 | 0.90 | K | 45° | |
| F | 0.19 | 0.25 | G | 1.27 TYP. | |

## Absolute Maximum Ratings

| Parameter | Symbol | Ratings CH-1 | Ratings CH-2 | Unit |
|---|---|---|---|---|
| Drain-Source Voltage | $V_{DS}$ | 30 | 30 | V |
| Gate-Source Voltage | $V_{GS}$ | ±25 | ±25 | V |
| Continuous Drain Current[3] | $I_D$ @TA=25℃ | 8.5 | 7.3 | A |
| Continuous Drain Current[3] | $I_D$ @TA=70℃ | 6.8 | 5.8 | A |
| Pulsed Drain Current[1] | $I_{DM}$ | 30 | 30 | A |
| Total Power Dissipation | $P_D$ @TA=25℃ | 2.0 | | W |
| Linear Derating Factor | | 0.016 | | W/℃ |
| Operating Junction and Storage Temperature Range | Tj, Tstg | -55 ~ +150 | | ℃ |

## Thermal Data

| Parameter | | Symbol | Value | Unit |
|---|---|---|---|---|
| Thermal Resistance Junction-ambient[3] | Max. | Rthj-a | 62.5 | ℃/W |

## CH-1 Electrical Characteristics (Tj = 25℃ unless otherwise specified)

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| Drain-Source Breakdown Voltage | $BV_{DSS}$ | 30 | - | - | V | $V_{GS}$=0, $I_D$=250uA |
| Breakdown Voltage Temperature Coefficient | $\triangle BV_{DSS}/\triangle Tj$ | - | 0.03 | - | V/℃ | Reference to 25℃, $I_D$=1mA |
| Gate Threshold Voltage | $V_{GS(th)}$ | 1.0 | - | 3.0 | V | $V_{DS}$=$V_{GS}$, $I_D$=250uA |
| Forward Transconductance | $g_{fs}$ | - | 12 | - | S | $V_{DS}$=10V, $I_D$=8A |
| Gate-Source Leakage Current | $I_{GSS}$ | - | - | ±100 | nA | $V_{GS}$= ±25V |
| Drain-Source Leakage Current(Tj=25℃) | $I_{DSS}$ | - | - | 1 | uA | $V_{DS}$=30V, $V_{GS}$=0 |
| Drain-Source Leakage Current(Tj=70℃) | | - | - | 25 | uA | $V_{DS}$=24V, $V_{GS}$=0 |
| Static Drain-Source On-Resistance[2] | $R_{DS(ON)}$ | - | 15 | 18 | mΩ | $V_{GS}$=10V, $I_D$=8A |
| | | | 23 | 30 | | $V_{GS}$=4.5V, $I_D$=6A |
| Total Gate Charge[2] | $Q_g$ | - | 14 | 22 | nC | $I_D$=8A<br>$V_{DS}$=24V<br>$V_{GS}$=4.5V |
| Gate-Source Charge | $Q_{gs}$ | - | 4 | - | | |
| Gate-Drain ("Miller") Change | $Q_{gd}$ | - | 8 | - | | |
| Turn-on Delay Time[2] | $T_{d(on)}$ | - | 12 | - | ns | $V_{DS}$=15V<br>$I_D$=1A<br>$V_{GS}$=10<br>$R_G$=3.3Ω<br>$R_D$=15Ω |
| Rise Time | $T_r$ | - | 7 | - | | |
| Turn-off Delay Time | $T_{d(off)}$ | - | 25 | - | | |
| Fall Time | $T_f$ | - | 9 | - | | |
| Input Capacitance | $C_{iss}$ | - | 1050 | 1680 | pF | $V_{GS}$=0V<br>$V_{DS}$=25V<br>f=1.0MHz |
| Output Capacitance | $C_{oss}$ | - | 240 | - | | |
| Reverse Transfer Capacitance | $C_{rss}$ | - | 165 | - | | |
| Gate Resistance | $R_g$ | - | 1.6 | 2.4 | Ω | f=1.0MHz |

## Source-Drain Diode

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| Forward On Voltage[2] | $V_{SD}$ | - | - | 1.2 | V | $I_S$=1.7A, $V_{GS}$=0V |
| Reverse Recovery Time[2] | $T_{rr}$ | - | 23 | - | ns | $I_S$=8A, $V_{GS}$=0V<br>dI/dt=100A/µs |
| Reverse Recovery Charge | $Q_{rr}$ | - | 15 | - | nC | |

Notes: 1. Pulse width limited by Max. junction temperature.

2. Pulse width≦300us, duty cycle≦2%.

3. Surface mounted on 1 $in^2$ copper pad of FR4 board, t≦10sec; 135℃/W when mounted on Min. copper pad.

## CH-2 Electrical Characteristics (Tj = 25℃ unless otherwise specified)

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| Drain-Source Breakdown Voltage | $BV_{DSS}$ | 30 | - | - | V | $V_{GS}$=0, $I_D$=250uA |
| Breakdown Voltage Temperature Coefficient | $\triangle BV_{DSS}/\triangle Tj$ | - | 0.03 | - | V/℃ | Reference to 25℃, $I_D$=1mA |
| Gate Threshold Voltage | $V_{GS(th)}$ | 1.0 | - | 3.0 | V | $V_{DS}=V_{GS}$, $I_D$=250uA |
| Forward Transconductance | $g_{fs}$ | - | 10 | - | S | $V_{DS}$=10V, $I_D$=7A |
| Gate-Source Leakage Current | $I_{GSS}$ | - | - | ±100 | nA | $V_{GS}$= ±25V |
| Drain-Source Leakage Current(Tj=25℃) | $I_{DSS}$ | - | - | 1 | uA | $V_{DS}$=30V, $V_{GS}$=0 |
| Drain-Source Leakage Current(Tj=70℃) | | - | - | 25 | uA | $V_{DS}$=24V, $V_{GS}$=0 |
| Static Drain-Source On-Resistance[2] | $R_{DS(ON)}$ | - | 22 | 26 | mΩ | $V_{GS}$=10V, $I_D$=7A |
| | | | 36 | 45 | | $V_{GS}$=4.5V, $I_D$=5A |
| Total Gate Charge[2] | $Q_g$ | - | 9 | 15 | nC | $I_D$=7A<br>$V_{DS}$=24V<br>$V_{GS}$=4.5V |
| Gate-Source Charge | $Q_{gs}$ | - | 3 | - | | |
| Gate-Drain (“Miller”) Change | $Q_{gd}$ | - | 5 | - | | |
| Turn-on Delay Time[2] | $T_{d(on)}$ | - | 9 | - | ns | $V_{DS}$=15V<br>$I_D$=1A<br>$V_{GS}$=10<br>$R_G$=3.3Ω<br>$R_D$=15Ω |
| Rise Time | $T_r$ | - | 6 | - | | |
| Turn-off Delay Time | $T_{d(off)}$ | - | 19 | - | | |
| Fall Time | $T_f$ | - | 6 | - | | |
| Input Capacitance | $C_{iss}$ | - | 640 | 1030 | pF | $V_{GS}$=0V<br>$V_{DS}$=25V<br>f=1.0MHz |
| Output Capacitance | $C_{oss}$ | - | 150 | - | | |
| Reverse Transfer Capacitance | $C_{rss}$ | - | 105 | - | | |
| Gate Resistance | $R_g$ | - | 1.7 | 2.5 | Ω | f=1.0MHz |

## Source-Drain Diode

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| Forward On Voltage[2] | $V_{SD}$ | - | - | 1.2 | V | $I_S$=1.7A, $V_{GS}$=0V |
| Reverse Recovery Time[2] | $T_{rr}$ | - | 18 | - | ns | $I_S$=7A, $V_{GS}$=0V<br>dI/dt=100A/μs |
| Reverse Recovery Charge | $Q_{rr}$ | - | 8 | - | nC | |

Notes: 1. Pulse width limited by Max. junction temperature.

2. Pulse width≦300us, duty cycle≦2%.

3. Surface mounted on 1 $in^2$ copper pad of FR4 board, t≦10sec; 135℃/W when mounted on Min. copper pad.

## Characteristics Curve CH-1

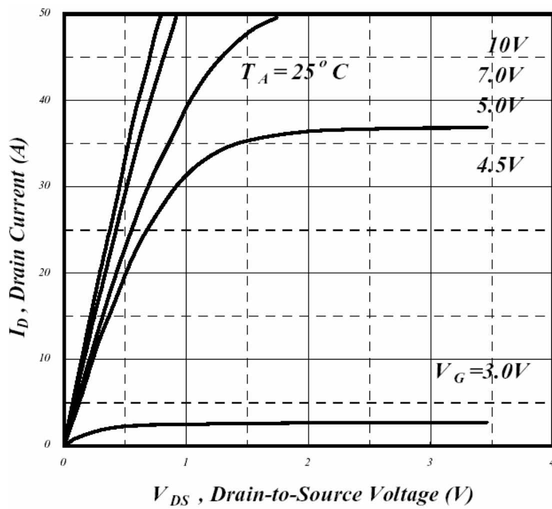



Fig 1. Typical Output Characteristics

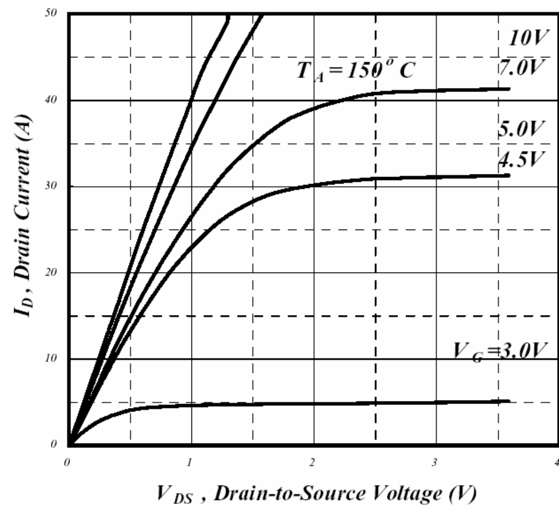



Fig 2. Typical Output Characteristics

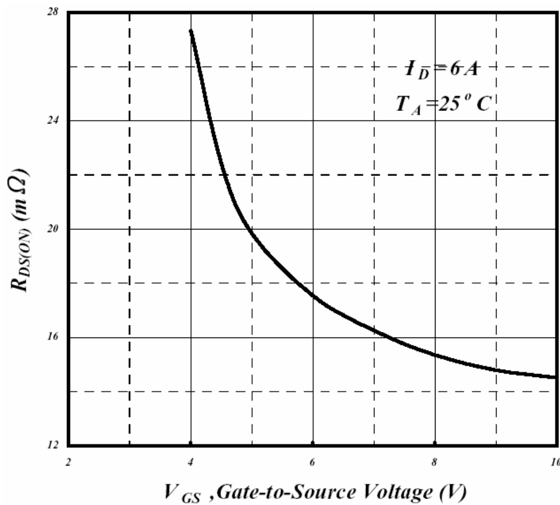



Fig 3. On-Resistance v.s. Gate Voltage

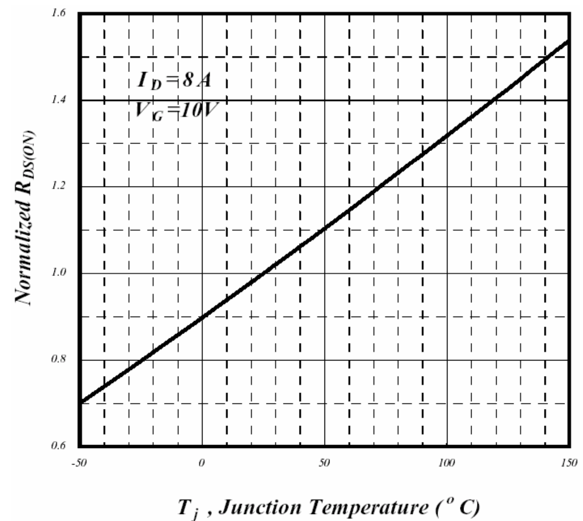



Fig 4. Normalized On-Resistance v.s. Junction Temperature

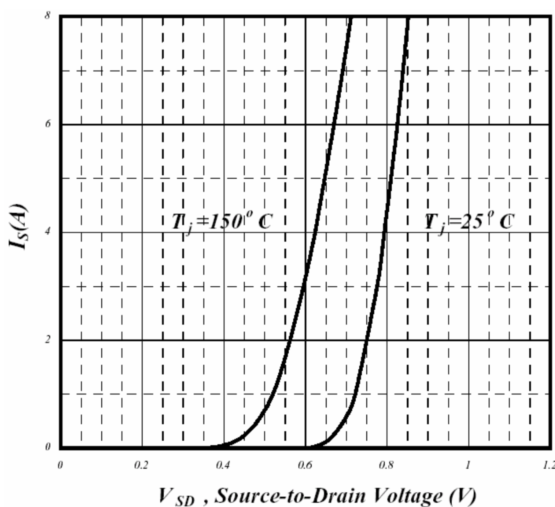



Fig 5. Forward Characteristics of Reverse Diode

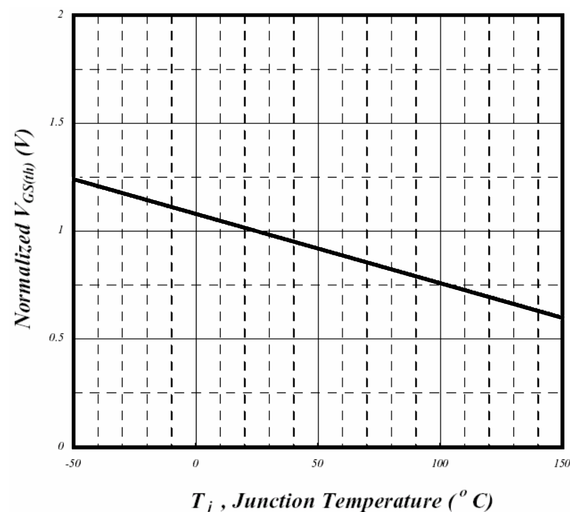



Fig 6. Gate Threshold Voltage v.s. Junction Temperature

**CH-1**

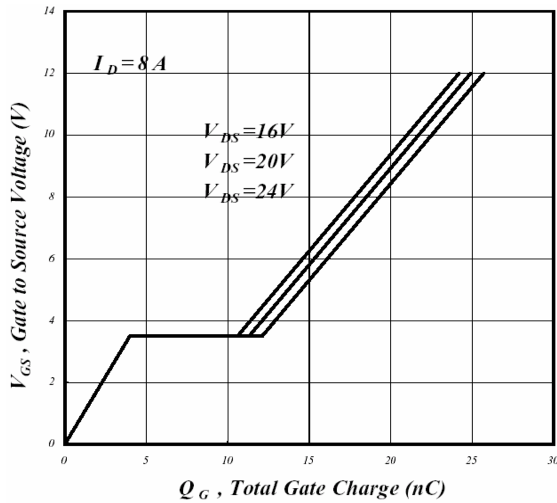



Fig 7. Gate Charge Characteristics

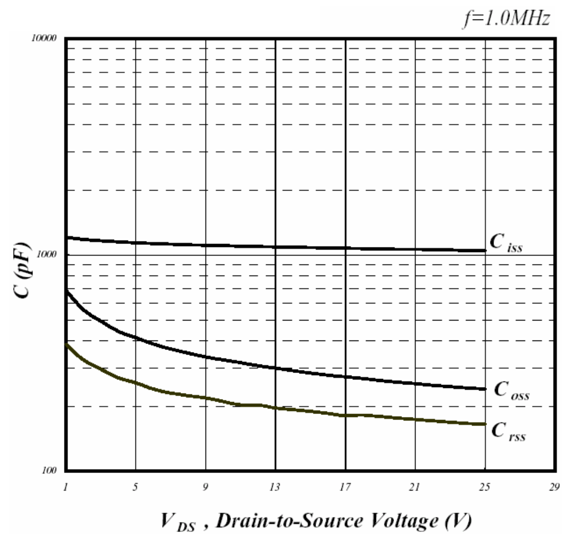



Fig 8. Typical Capacitance Characteristics

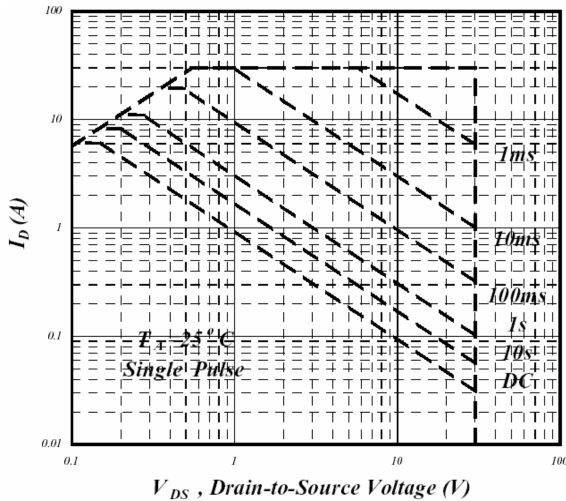



Fig 9. Maximum Safe Operating Area

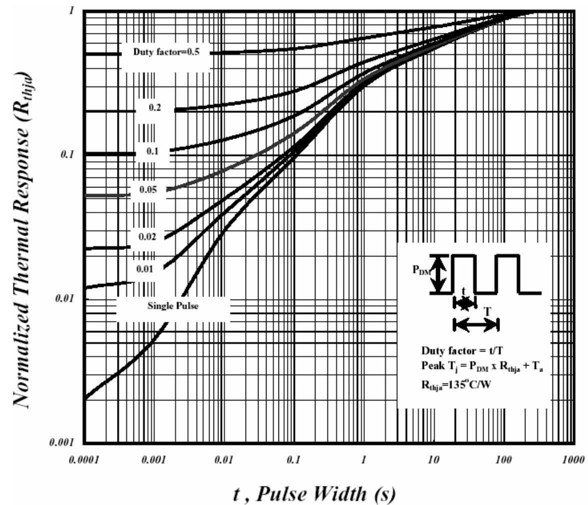



Fig 10. Effective Transient Thermal Impedance

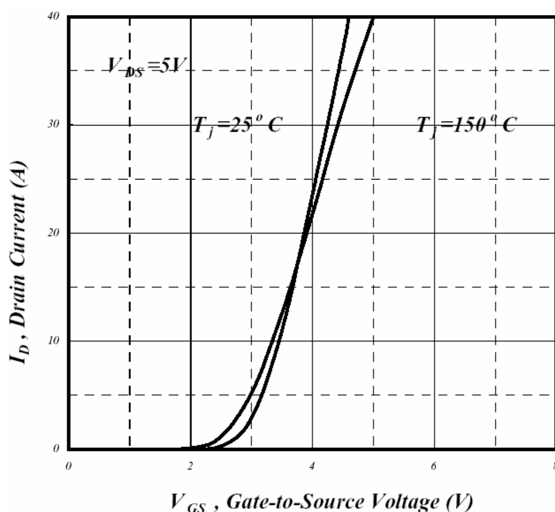



Fig 11. Transfer Characteristics

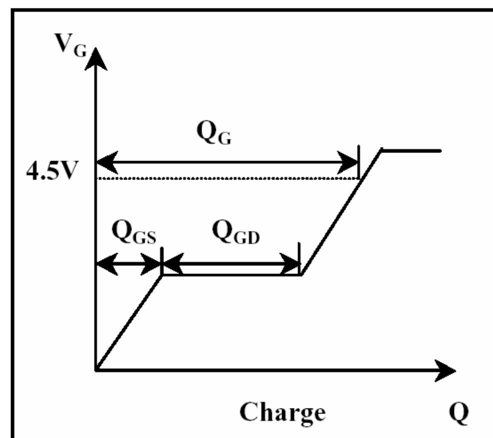



Fig 12. Gate Charge Waveform

**CH-2**

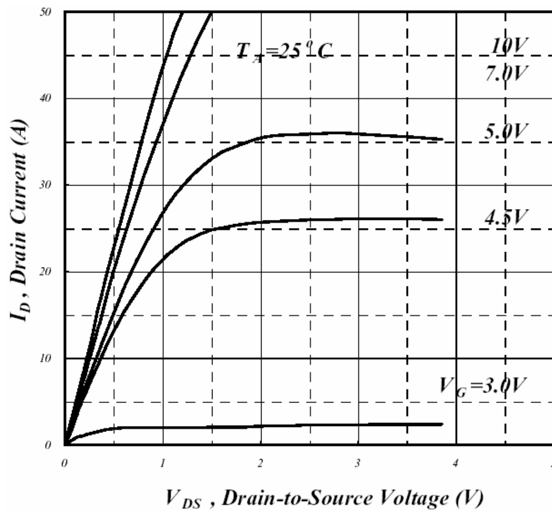



**Fig 1. Typical Output Characteristics**

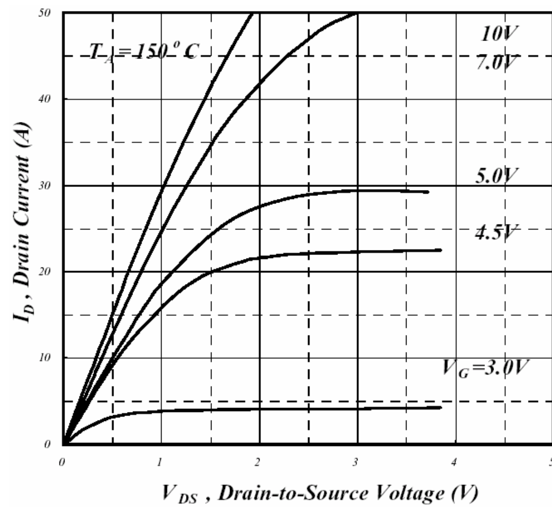



**Fig 2. Typical Output Characteristics**

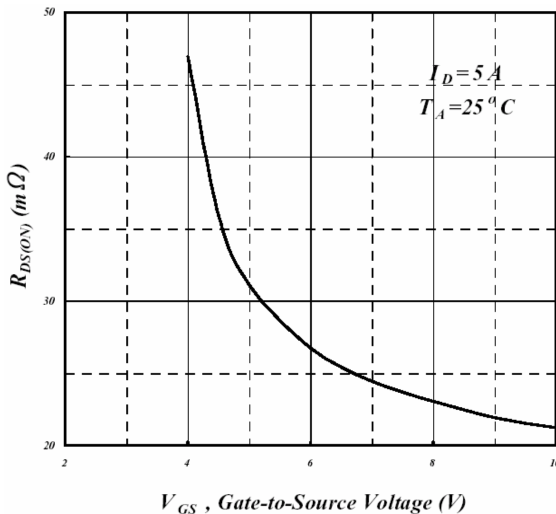



**Fig 3. On-Resistance v.s. Gate Voltage**

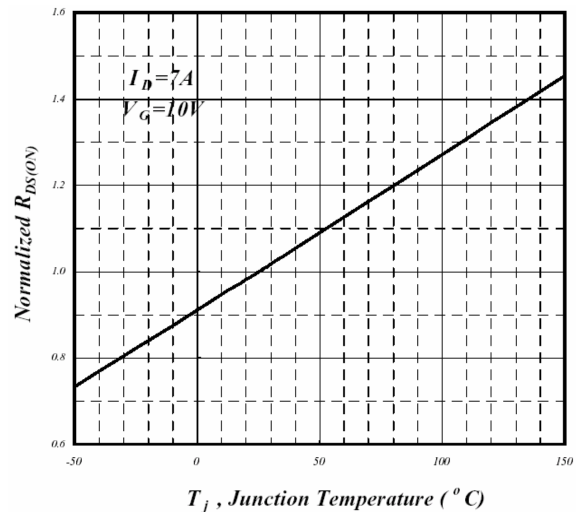



**Fig 4. Normalized On-Resistance v.s. Junction Temperature**

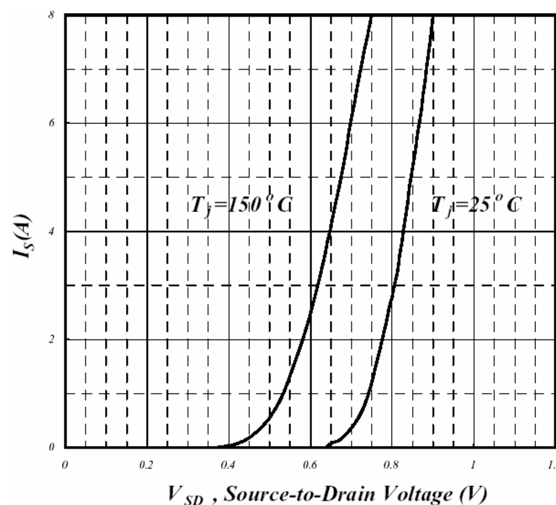



**Fig 5. Forward Characteristics of Reverse Diode**

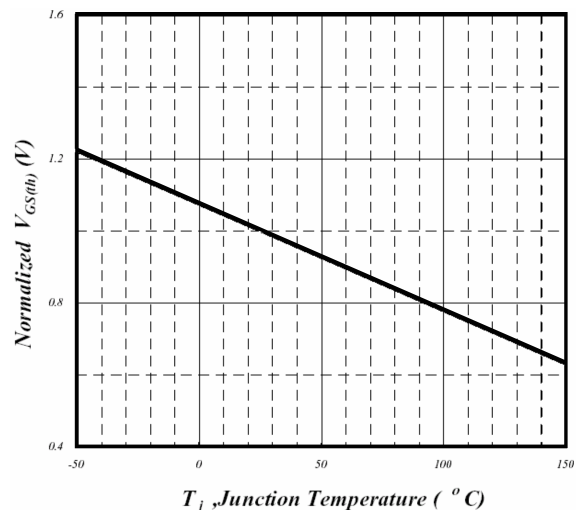



**Fig 6. Gate Threshold Voltage v.s. Junction Temperature**

**CH-2**

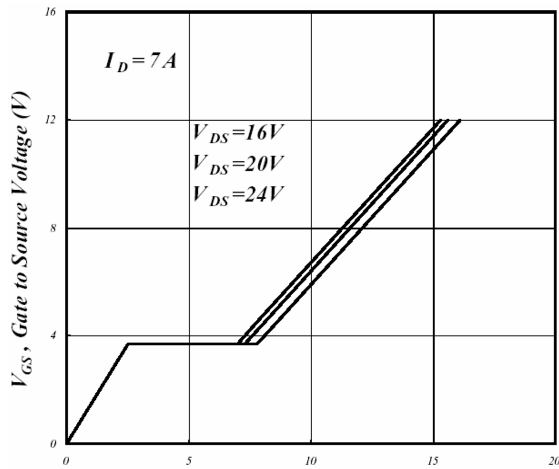



**Fig 7. Gate Charge Characteristics**

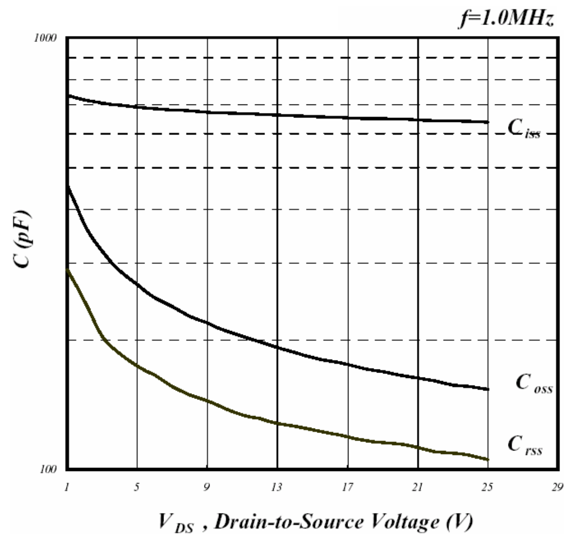



**Fig 8. Typical Capacitance Characteristics**

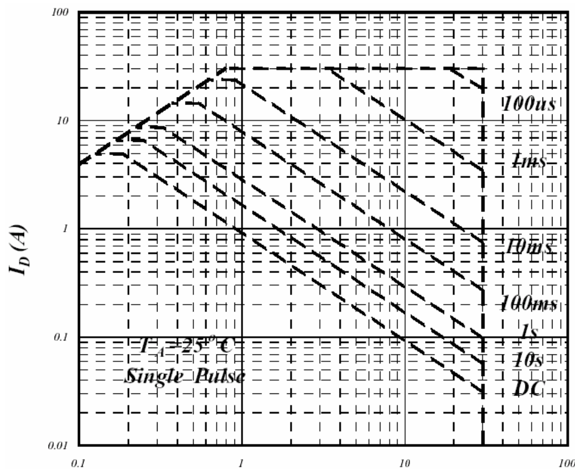



**Fig 9. Maximum Safe Operating Area**

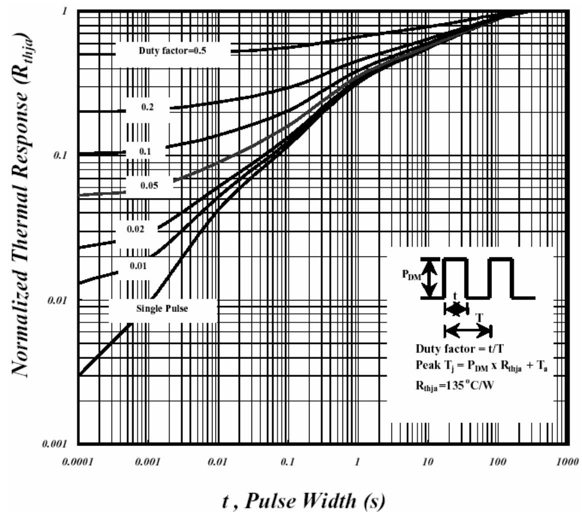



**Fig 10. Effective Transient Thermal Impedance**

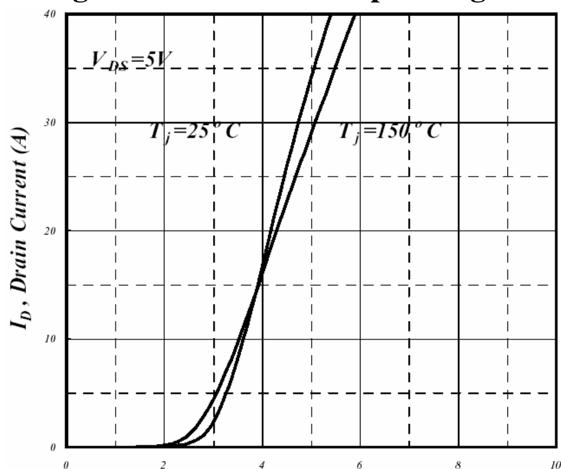



**Fig 11. Transfer Characteristics**

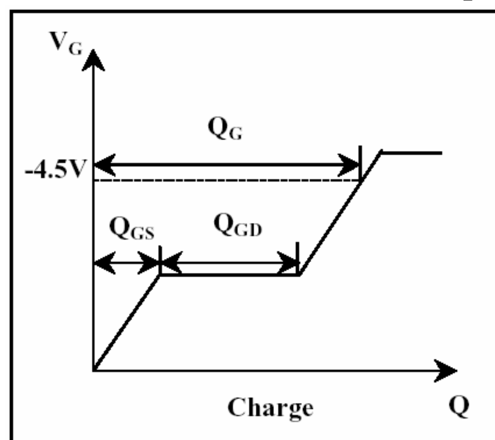



**Fig 12. Gate Charge Waveform**

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