HI-3596, HI-3597, HI-3598, HI-3599

Octal ARINC 429 Receivers with Label Recognition and SPI Interface

November, 2009

GENERAL DESCRIPTION

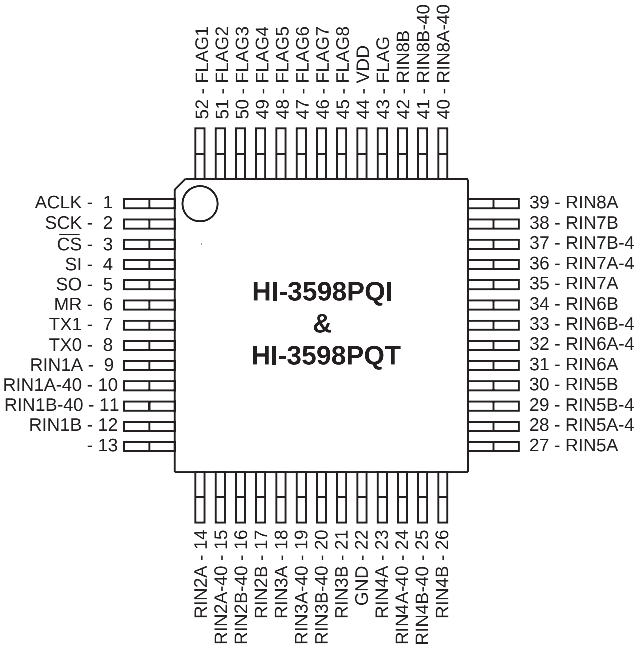
The HI-359x family from Holt Integrated Circuits are silicon gate CMOS ICs for interfacing up to eight ARINC 429 receive buses to a high-speed Serial Peripheral Interface (SPI) enabled microcontroller. Each receiver has user-programmable label recognition for up to 16 labels, a four-word data buffer (FIFO), and an on-chip analog line receiver. Receive FIFO status can be monitored using the programmable external interrupt pins, or by polling the status register. Other features include the ability to switch the bit-signifiance of the ARINC 429 label and to recognize the 32nd received ARINC bit as either data or a parity flag. Some versions provide a digital transmit channel which can be utilized with an external line driver such as HI-8570 to relay information from multiple sources, for example sensors, to a single collection point such as a flight computer and can also be configured as a loopback test register for each receive channel. Versions are also available with different input resistance values to provide flexibility when using external lightning protection circuitry. The SPI and all control signals are CMOS and TTL compatible and support 3.3V or 5V operation.

The HI-3596 and HI-3598 are full featured parts. The HI-3597 and HI-3599 give the user the option of utilizing a smaller 24-pin SOIC package with very little trade off in features. In this case, a global interrupt flag is provided instead of individual external FIFO interrupt pins. The HI-3597 is identical to the HI-3599 except that it offers the digital transmit feature and seven receive channels.

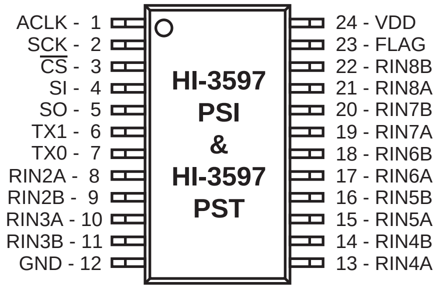
FEATURES

- ARINC 429 compliant
- Up to 8 independent receive channels
- Digital transmit channel (except HI-3599)
- 3.3V or 5.0V logic supply operation
- On-chip analog line receivers connect directly to ARINC 429 bus
- Programmable label recognition for 16 labels per channel
- Independent data rate selection for each receiver
- Four-wire SPI interface
- Label bit-order control
- 32nd bit can be data or parity
- Low Power
- Industrial & extended temperature ranges

PIN CONFIGURATION (TOP VIEW)


52 - FLAG1
51 - FLAG2
50 - FLAG3
49 - FLAG4
48 - FLAG5
47 - FLAG6
46 - FLAG7
45 - FLAG8
44 - VDD
43 - FLAG
42 - RIN8B
41 - RIN8B-40
40 - RIN8A-40
ACLK - 1
SCK - 2
$\overline{CS}$ - 3
SI - 4
SO - 5
MR - 6
TX1 - 7
TX0 - 8
RIN1A - 9
RIN1A-40 - 10
RIN1B-40 - 11
RIN1B - 12
- 13
HI-3598PQI
&
HI-3598PQT
39 - RIN8A
38 - RIN7B
37 - RIN7B-40
36 - RIN7A-40
35 - RIN7A
34 - RIN6B
33 - RIN6B-40
32 - RIN6A-40
31 - RIN6A
30 - RIN5B
29 - RIN5B-40
28 - RIN5A-40
27 - RIN5A
RIN2A - 14
RIN2A-40 - 15
RIN2B-40 - 16
RIN2B - 17
RIN3A - 18
RIN3A-40 - 19
RIN3B-40 - 20
RIN3B - 21
GND - 22
RIN4A - 23
RIN4A-40 - 24
RIN4B-40 - 25
RIN4B - 26

HI-3598 Full function, full pin-out version
52 - Pin Plastic Quad Flat Pack (PQFP)

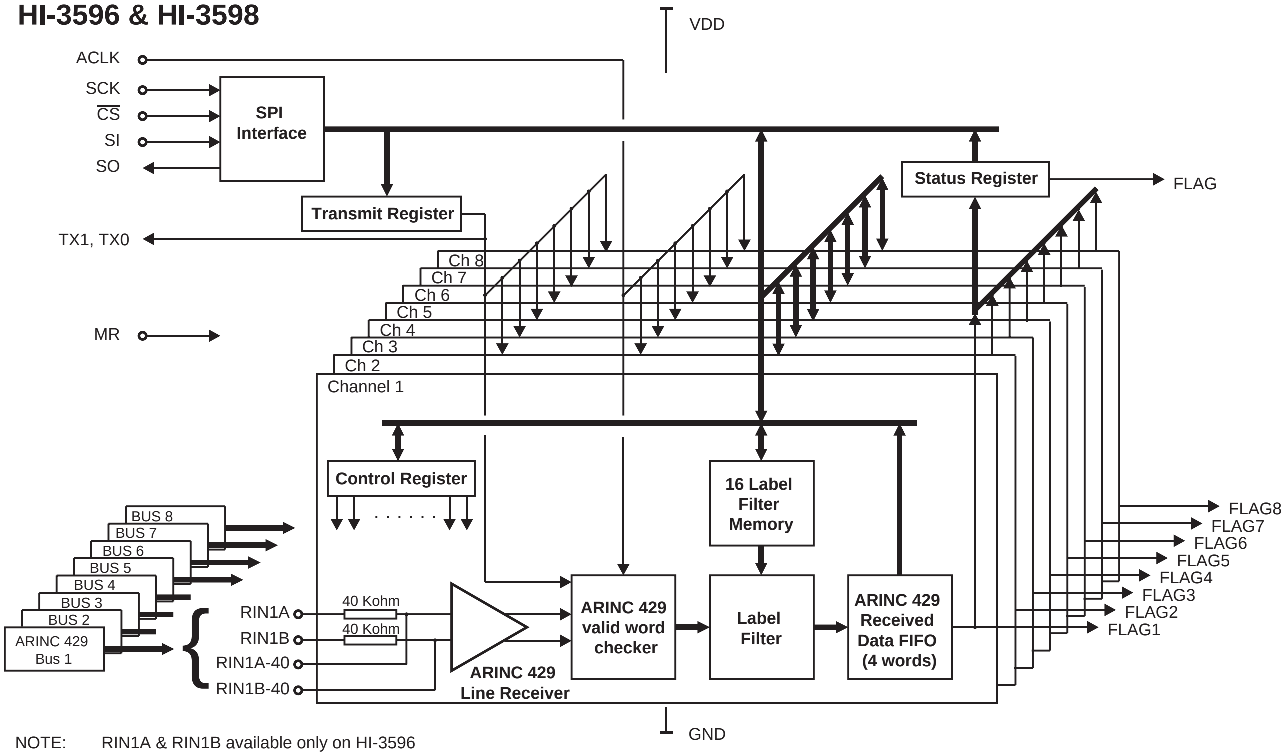

ACLK - 1
SCK - 2
$\overline{CS}$ - 3
SI - 4
SO - 5
TX1 - 6
TX0 - 7
RIN2A - 8
RIN2B - 9
RIN3A - 10
RIN3B - 11
GND - 12
HI-3597
PSI
&
HI-3597
PST
24 - VDD
23 - FLAG
22 - RIN8B
21 - RIN8A
20 - RIN7B
19 - RIN7A
18 - RIN6B
17 - RIN6A
16 - RIN5B
15 - RIN5A
14 - RIN4B
13 - RIN4A

HI-3597 minimum footprint, reduced pin-out version
24 - Pin Plastic Small Outline package (SOIC)

(*See page 13 for additional package pin configurations*)

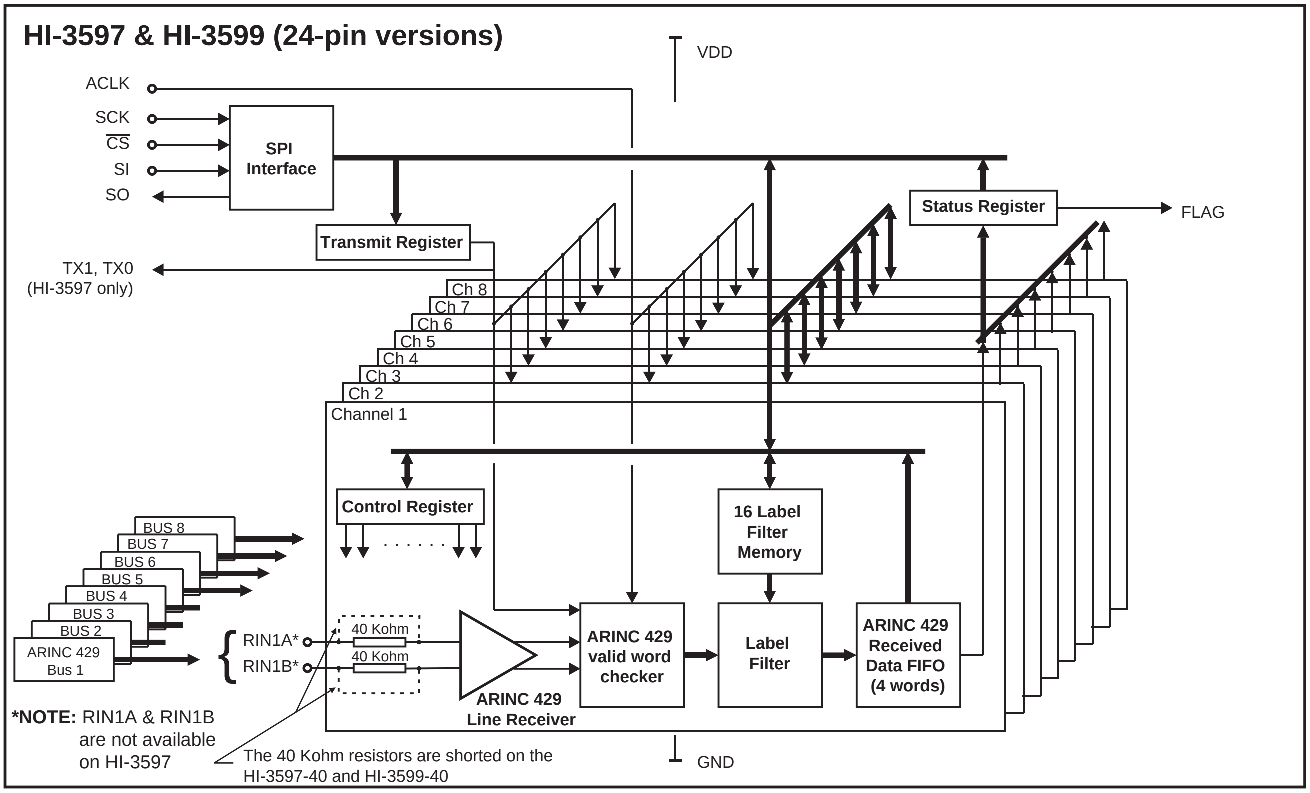
BLOCK DIAGRAMS

HI-3596 & HI-3598


VDD
ACLK
SCK
CS
SI
SO
SPI Interface
Transmit Register
TX1, TX0
MR
Status Register
FLAG
Ch 8
Ch 7
Ch 6
Ch 5
Ch 4
Ch 3
Ch 2
Channel 1
Control Register
16 Label Filter Memory
BUS 8
BUS 7
BUS 6
BUS 5
BUS 4
BUS 3
BUS 2
ARINC 429 Bus 1
RIN1A
RIN1B
RIN1A-40
RIN1B-40
40 Kohm
40 Kohm
ARINC 429 Line Receiver
ARINC 429 valid word checker
Label Filter
ARINC 429 Received Data FIFO (4 words)
FLAG8
FLAG7
FLAG6
FLAG5
FLAG4
FLAG3
FLAG2
FLAG1
GND

NOTE: RIN1A & RIN1B available only on HI-3596
RIN1A-40 & RIN1B-40 available only on HI-3596-40

HI-3597 & HI-3599 (24-pin versions)


VDD
ACLK
SCK
CS
SI
SO
SPI Interface
Transmit Register
TX1, TX0
(HI-3597 only)
Status Register
FLAG
Ch 8
Ch 7
Ch 6
Ch 5
Ch 4
Ch 3
Ch 2
Channel 1
Control Register
16 Label Filter Memory
BUS 8
BUS 7
BUS 6
BUS 5
BUS 4
BUS 3
BUS 2
ARINC 429 Bus 1
RIN1A*
RIN1B*
40 Kohm
40 Kohm
ARINC 429 Line Receiver
ARINC 429 valid word checker
Label Filter
ARINC 429 Received Data FIFO (4 words)
GND

***NOTE:** RIN1A & RIN1B are not available on HI-3597

The 40 Kohm resistors are shorted on the HI-3597-40 and HI-3599-40

Figure 1. Block Diagrams

PIN DESCRIPTIONS

Table 1. Pin Descriptions

Pin	Function	Description	3596	3597	3598	3599
VDD	POWER	3.3V or 5.0V power supply	X	X	X	X
GND	POWER	Chip 0V supply	X	X	X	X
$\overline{CS}$	INPUT	Chip select. Data is shifted into SI and out of SO when $\overline{CS}$ is low	X	X	X	X
SCK	INPUT	SPI Clock. Data is shifted into or out of the SPI interface using SCK	X	X	X	X
SI	INPUT	SPI interface serial data input	X	X	X	X
SO	OUTPUT	SPI interface serial data output	X	X	X	X
ACLK	INPUT	Master 1 MHz timing reference for the ARINC 429 receiver and transmitter	X	X	X	X
RIN1A* - RIN8A	ARINC INPUT	ARINC receiver positive input. Direct connection to ARINC 429 bus	Std	Std	X	Std
RIN1B* - RIN8B	ARINC INPUT	ARINC receiver negative input. Direct connection to ARINC 429 bus	Std	Std	X	Std
RIN1A-40* - RIN8A-40	ARINC INPUT	Alternate ARINC receiver positive input. Requires external 40KΩ resistor	-40	-40	X	-40
RIN1B-40* - RIN8B-40	ARINC INPUT	Alternate ARINC receiver negative input. Requires external 40KΩ resistor	-40	-40	X	-40
FLAG1 - FLAG8	OUTPUT	Goes high when ARINC 429 receiver FIFO is not empty (CR1=0), or full (CR1=1)	X	-	X	-
FLAG	OUTPUT	Logical OR of FLAG1 through FLAG8	X	X	X	X
TX1	OUTPUT	ARINC 429 test word ONE state serial output pin	X	X	X	-
TX0	OUTPUT	ARINC 429 test word ZERO state serial output pin	X	X	X	-
MR	INPUT	Hardware active high Master Reset. Clears all receivers and FIFOs. Does not affect Control Register contents.	X	-	X	-

* **NOTE:** RIN1A & RIN1B are not available on HI-3597

INSTRUCTIONS

Instruction op codes are used to read, write and configure the HI-359x devices. The instruction format is illustrated in Figure 2. When $\overline{CS}$ goes low, the next 8 clocks at the SCK pin shift an instruction op code into the decoder, starting with the first rising edge. The op code is fed into the SI pin, most significant bit first.

For write instructions, the most significant bit of the data word must immediately follow the instruction op code and is clocked into its register on the next rising SCK edge. Data word length varies depending on word type written: 16-bit Control Register writes, 32-bit transmit register writes or 128-bit writes to a channel's label-matching enable/disable memory.

For read instructions, the most significant bit of the requested data word appears at the SO pin after the last op code bit is clocked into the decoder, at the next falling SCK edge. As in write instructions, the data field bit-length varies with read instruction type.

Channel-specific instructions use the upper four bits to specify an ARINC 429 receiver channel, 1-8 hex. The lower four bits specify the op code, described in Table 2. The four channel assignment bits are "don't care" for instructions that are not channel-specific, such as Master Reset.

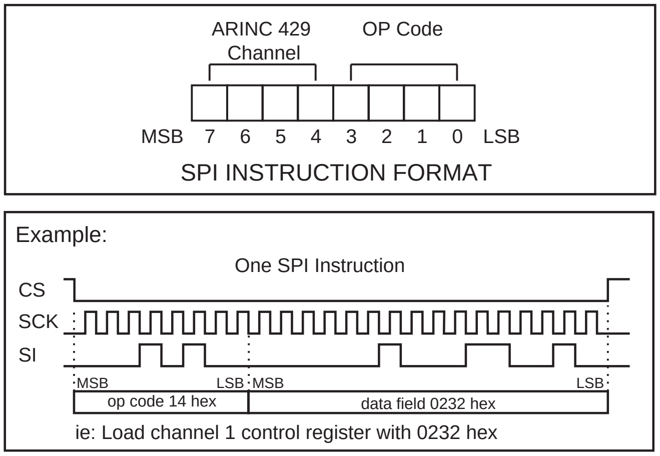


Figure 2. SPI Instruction Format

Table 2. Defined Instructions

ARINC Channel	OP CODE Hex	DATA FIELD	Description
X	0h	None	Instruction not implemented. No operation.
1h - 8h	1h	128 bits	Load label values to label memory. The data field consists of 16, 8-bit labels. If fewer than 16 labels are needed for the application, the memory must be padded with redundant (duplicate) label values.
1h - 8h	2h	128 bits	Read the contents of the label memory for this channel.
1h - 8h	3h	32 bits	Read an ARINC word from the receive FIFO for this channel. If the FIFO is empty all zeros will be read.
1h - 8h	4h	16 bits	Load the specified channel's Control Register and clear that channel's FIFO.
1h - 8h	5h	16 bits	Read the specified channel's Control Register.
X	6h	16 bits	Read the Status Register.
X	7h	None	Master Reset (All channels).
X	8h	32 bits	Load the Transmit Register (High-speed data rate). This can also be used as a test word for each receiver (Loopback self-test).
X	9h	32 bits	Load the Transmit Register (Low-speed data rate). This can also be used as a test word for each receiver (Loopback self-test).
X	Ah - Fh	None	Instruction not implemented. No operation.

FUNCTIONAL DESCRIPTION

Control Word Register

Each HI-359x receive channel is assigned a 16-bit Control Register which configures that receiver. Control Register bits CR15 - CR0 are loaded from a 16-bit data value appended to SPI instruction n4 hex, where "n" is the channel number 1-8 hex. Writing to the Control Register also clears the data FIFO for that channel. The Control Register contents may be read using SPI instruction n5 hex. Table 3 summarizes the Control Register bits functions.

Table 3. Control Register Bits Functions

CR Bit	Function	State	Description
CR0 (LSB)	Receiver Data Rate Select	0	Data rate = ACLK/10 (ARINC 429 High-Speed)
		1	Data rate = ACLK/80 (ARINC 429 Low-Speed)
CR1	RFLAG Definition	0	FLAG goes high when receive FIFO is not empty (Contains at least one word)
		1	FLAG goes high when receive FIFO is full
CR2	Enable Label Recognition	0	Label recognition disabled
		1	Label recognition enabled
CR3	Reset Receiver	0	Normal Operation
		1	Reset this receiver (Clear receiver logic and FIFO). The receive channel is disabled if CR3 is left high
CR4	Receiver Parity Check Enable	0	Receiver parity check disabled
		1	Receiver odd parity check enabled
CR5	Self-Test (Loopback)	0	Receiver's inputs are connected to the Transmit Register serial data output.
		1	Normal operation
CR6	Receiver Decoder	0	Receiver Decoder Disabled
		1	ARINC bits 10 and 9 must match CR7 and CR8
CR7	-	-	If receiver decoder is enabled, the ARINC bit 10 must match this bit
CR8	-	-	If receiver decoder is enabled, the ARINC bit 9 must match this bit
CR9	ARINC Label Bit Order	0	Label bit order reversed (See Table 5)
		1	Label bit order same as received (See Table 5)
CR10 to CR15 (MSB)	Not Used	X	Control register read returns "0" for these bits

Status Register

The HI-359x devices have a single 16-bit Status Register which is read to determine status for the eight received data FIFOs. The Status Register is read using SPI instruction n6 hex. Table 4 summarizes the Status Register bits functions.

Table 4. Status Register Bits Functions

CR Bit	Function	State	Description
SR0 (LSB)	Receiver 1 FIFO Empty	0	Receiver 1 FIFO contains valid data. Resets to Zero when all data has been read. FLAG pin reflects the state of this bit when CR1="0"
		1	Receiver 1 FIFO is empty
SR1	Receiver 2 FIFO Empty	0	Receiver 2 FIFO contains valid data.
		1	Receiver 2 FIFO is empty
SR2 to SR6	Receiver 3 to Receiver 7 FIFO Empty	: : : :	: : : :
SR7	Receiver 8 FIFO Empty	0	Receiver 8 FIFO contains valid data.
		1	Receiver 8 FIFO is empty
SR8	Receiver 1 FIFO Full	0	Receiver 1 FIFO not full. FLAG pin reflects the state of this bit when CR1="1"
		1	Receiver 1 FIFO full. To avoid data loss, the FIFO must be read within one ARINC word period.
SR9	Receiver 2 FIFO Full	0	Receiver 2 FIFO not full.
		1	Receiver 2 FIFO full.
SR10 to SR14	Receiver 3 to Receiver 7 FIFO Full	: : : :	: : : :
SR15 (MSB)	Receiver 8 FIFO Full	0	Receiver 8 FIFO not full.
		1	Receiver 8 FIFO full.

ARINC 429 Data Format

Control Register bit CR9 controls how individual bits in the received ARINC word are mapped to the HI-359x SPI data word during data read operations. Table 5 describes this mapping.

Table 5. SPI / ARINC bit-mapping

SPI / ARINC bit-mapping											
SPI Order	1	2 - 22	23	24	25	26	27	28	29	30	31	32
ARINC bit CR11 = 0	32 Parity	31 - 11 Data	10 SDI	9 SDI	1 Label (MSB)	2 Label	3 Label	4 Label	5 Label	6 Label	7 Label	8 Label (LSB)
ARINC bit CR11 = 1	32 Parity	31 - 11 Data	10 SDI	9 SDI	8 Label (LSB)	7 Label	6 Label	5 Label	4 Label	3 Label	2 Label	1 Label (MSB)

ARINC 429 Receiver

ARINC Bus Interface

Figure 3 shows the input circuit for each on-chip ARINC 429 line receiver. The ARINC 429 specification requires detection levels summarized in Table 6.

Table 6. ARINC 429 Detection Levels

STATE	DIFFERENTIAL VOLTAGE
ONE	+6.5 Volts to +13 Volts
NULL	+2.5 Volts to -2.5 Volts
ZERO	-6.5 Volts to -13 Volts

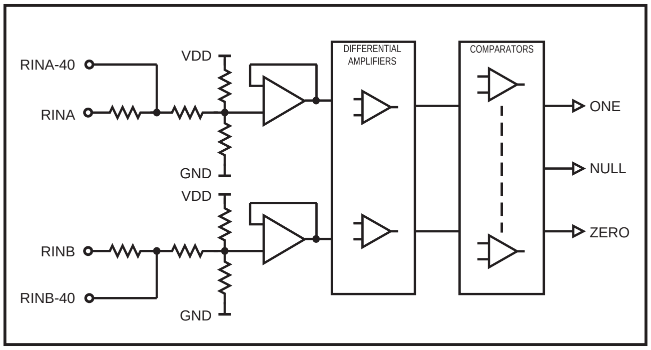


Figure 3. ARINC Receiver Input

The HI-359x family guarantees recognition of these levels with a common mode Voltage with respect to GND less than ±30V for the worst case condition (3.15V supply and 13V signal level).

The tolerances in the design guarantee detection of the above levels, so the actual acceptance ranges are slightly larger. If the ARINC signal is out of the actual acceptance ranges, including the nulls, the chip rejects the data.

Receiver Logic Operation

Figure 4 is a block diagram showing the logic for each receiver.

Bit Timing

The ARINC 429 specification defines timing tolerances for received data according to Table 7.

Table 7. ARINC 429 Receiver Timing Tolerances

	HIGH SPEED	LOW SPEED
Bit Rate	100Kbps ± 1%	12K - 14.5Kbps
Pulse Rise Time	1.5 ± 0.5µs	10 ± 5µs
Pulse Fall Time	1.5 ± 0.5µs	10 ± 5µs
Pulse Width	5µs ± 5%	34.5 to 41.7µs

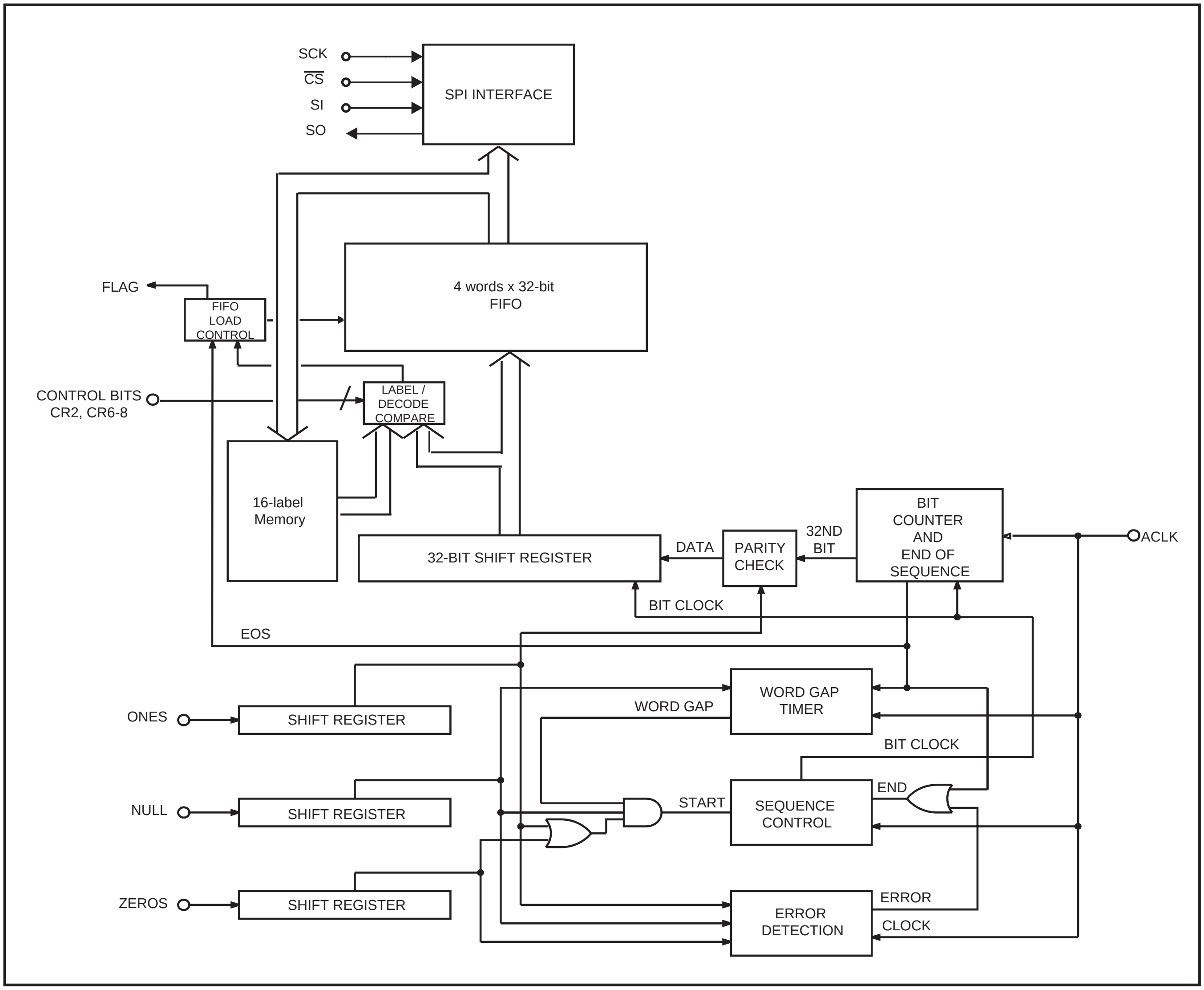

SCK
$\overline{CS}$
SI
SO
SPI INTERFACE
4 words x 32-bit FIFO
FLAG
FIFO LOAD CONTROL
CONTROL BITS CR2, CR6-8
LABEL / DECODE COMPARE
16-label Memory
32-BIT SHIFT REGISTER
DATA
PARITY CHECK
32ND BIT
BIT COUNTER AND END OF SEQUENCE
ACLK
BIT CLOCK
EOS
ONES
SHIFT REGISTER
WORD GAP
WORD GAP TIMER
BIT CLOCK
NULL
SHIFT REGISTER
START
SEQUENCE CONTROL
END
ZEROS
SHIFT REGISTER
ERROR DETECTION
ERROR
CLOCK

Figure 4. Receiver Block Diagram

The HI-359x family accept signals within these tolerances and rejects signals outside these tolerances. Receiver logic achieves this as described below:

1. An accurate 1MHz clock source is required to validate the receive signal timing. Less than 0.1% error is recommended.
2. The receiver uses three separate 10-bit sampling shift registers for Ones detection, Zeros detection and Null detection. When the input signal is within the differential voltage range for any shift register's state (One Zero or Null) sampling clocks a high bit into that register. When the receive signal is outside the differential voltage range defined for any shift register, a low bit is clocked. Only one shift register can clock a high bit for any given sample. All three registers clock low bits if the differential input voltage is between defined state voltage bands.

   Valid data bits require at least three consecutive One or Zero samples (three high bits) in the upper half of the Ones or Zeros sampling shift register, and at least three consecutive Null samples (three high bits) in the lower half of the Null sampling shift register within the data bit interval.

   A word gap Null requires at least three consecutive Null samples (three high bits) in the upper half of the Null sampling shift register and at least three consecutive Null samples (three high bits) in the lower half of the Null sampling shift register. This guarantees the minimum pulse width.

3. To validate the receive data bit rate, each bit must follow its preceding bit by not less than 8 samples and not more than 12 samples. With exactly 1MHz input clock frequency, the acceptable data bit rates are shown in Table 8.

Table 8. Acceptable Data Bit Rates at 1MHz Input Clock Frequency

	HIGH SPEED	LOW SPEED
Data Bit Rate Min	83Kbps	10.4Kbps
Data Bit Rate Max	125Kbps	15.6Kbps

4. Following the last data bit of a valid reception, the Word Gap timer samples the Null shift register every 10 input clocks (every 80 clocks for low speed). If a Null is present, the Word Gap counter is incremented. A Word Gap count of 3 enables the next reception.

Receiver Parity

If enabled by setting Control Register CR4 bit to “1”, the receiver parity circuit counts Ones received, including the parity bit. If the result is odd, then a “0” appears in the 32nd bit.

Setting Control Register CR4 bit to “0” disables parity checking and all 32 bits are treated as data.

Retrieving Data

Once 32 valid bits are recognized, the receiver logic generates an End of Sequence (EOS). Depending on the state of Control Register bits CR2, CR6, CR7 and CR8, the received 32-bit ARINC word is then checked for correct decoding and label match before it is loaded into the 4 x 32 Receive FIFO. ARINC words that do not match required 9th and 10th ARINC bit and do not have a label match are ignored and are not loaded into the Receive FIFO. Table 9 describes this operation.

Table 9. FIFO Loading Control

CR2	ARINC word matches Enabled label	CR6	ARINC word bits 10, 9 match CR7, 8	FIFO
0	X	0	X	Load FIFO
1	No	0	X	Ignore Data
1	Yes	0	X	Load FIFO
0	X	1	No	Ignore Data
0	X	1	Yes	Load FIFO
1	Yes	1	No	Ignore Data
1	No	1	Yes	Ignore Data
1	No	1	No	Ignore Data
1	Yes	1	Yes	Load FIFO

Once a valid ARINC word is loaded into the FIFO, the EOS signal clocks the Data Ready flip-flop to a “1”, and the corresponding channel’s Status Register FIFO Empty bit (SR0- SR7) goes to a “0”. The channel’s Empty bit remains low until the corresponding Receive FIFO is empty. Each received ARINC word is retrieved via the SPI interface using SPI instruction n3 hex where “n” is the channel number 1-8 hex.

Up to 4 ARINC words may be held in each channel’s Receive FIFO. The Status Register FIFO Full bit (SR8 - SR15) goes high when the corresponding channel’s Receive FIFO is full. Failure to offload a full Receive FIFO causes additional received valid ARINC words to overwrite the last received word.

Label Recognition

The user loads the 16 byte label look-up table to specify which 8-bit incoming ARINC labels are captured by the receiver, and which are discarded. If fewer than 16 labels are required, spare label memory locations must be filled with duplicate copies of any valid label. After the look-up table is initialized, set channel Control Register bit CR2 to enable label recognition for that channel.

If label recognition is enabled, the receiver compares the label in each new ARINC word against the channel’s stored label look-up table. If a label match is found, the received word is processed. If no match occurs, the new ARINC word is discarded and no indicators of received ARINC data are presented. Note that 00 hex is treated in the same way as any other label value. Label memory bit significance is not changed by the status of Control Register bit CR9. The most significant label bit is always compared to the first (MSB) bit of each SPI 8-bit data field from SPI instruction n1 hex, where “n” is the channel number 1-8 hex.

If a channel Control Register CR2 bit equals ”0,” the corresponding receiver recognizes all label values as valid, as shown in Table 9.

Reading the Label Memory

The contents of each channel’s Label Memory may be read via the SPI interface using instruction n2 hex where “n” equals the channel number 1-8 hex, as described in Table 2.

Digital Transmit Function

The Transmit Register can be used as a digital transmitter by connecting the TX1 and TX0 pins to an external ARINC 429 line driver such as the HI-8570 or HI-8571 (except HI-3599).

Loopback Self-Test

The HI-359x devices may use the Transmit Register to execute user-defined self-test sequences (loopback test) for each receiver. This feature may be individually enabled for each receiver by resetting Control Register CR5 bit to “0”. A 32-bit test word is loaded to the Transmit Register using SPI instructions n8 hex (for ARINC 429 high-speed data rate) or n9 hex (for ARINC 429 low speed). Upon completion of the instruction, the word is shifted out of the register and routed to all receivers. If self-test mode is enabled and the receive channel is set to the correct speed, each channel will receive the test word as if it came from an external ARINC 429 bus. If loopback is not enabled, the channel ignores the self-test word and continues to respond to the external ARINC 429 bus (**Note:** In the case of HI-3597, RIN1A and RIN1B pins are not available). In all cases, the serial test word may be observed at the TX1 and TX0 pins (except HI-3599), as shown in Table 10.

NOTE: The first bit shifted into the Self Test register will be the first bit sent to the receivers and the TX1 and TX0 pins. In ARINC 429 protocol, this bit is the LSB.

Table 10. Test Outputs

TX1	TX0	ARINC 429 State
0	0	NULL
1	0	ONE
0	1	ZERO

Line Receiver Input Pins

The HI-3598 has two sets of Line Receiver input pins, RINA/B and RINA/B-40. Only one pair may be used to connect to the ARINC 429 bus. THE RINA/B pins may be connected directly to the ARINC 429 bus. The RINA/B-40 pins require an external 40KΩ resistor to be added in series with each ARINC input without affecting the ARINC input thresholds. This option is especially useful in applications where lightning protection circuitry is also required.

When using the RINA/B-40 pins, each side of the ARINC bus must be connected through a 40KΩ series resistor in order for the chip to detect the correct ARINC levels. The typical 10V differential signal is translated and input to a window comparator and latch. The comparator levels are set so that with the external 40KΩ resistors, they are just below the standard 6.5V minimum ARINC data threshold and just above the standard 2.5V maximum ARINC null threshold.

When using HI-3596, HI-3597 or HI-3599, only one set of ARINC 429 receive inputs are provided for each channel. The standard HI-3596, HI-3597 and HI-3599 use the direct-connection RINA / RINB pins. The HI-3596-40, HI-3597-40 and HI-3599-40 devices use the RINA-40 / RINB-40 pins and require external 40KΩ series resistors. See the Ordering Information table for complete part number options.

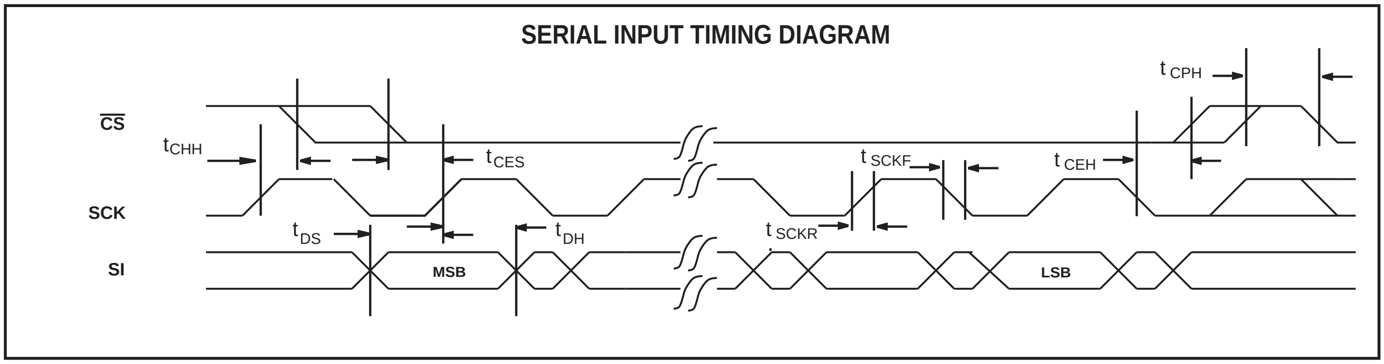
Please refer to the Holt AN-300 Application Note for additional information and recommendations on lightning protection of Holt line drivers and line receivers.

Master Reset (MR)

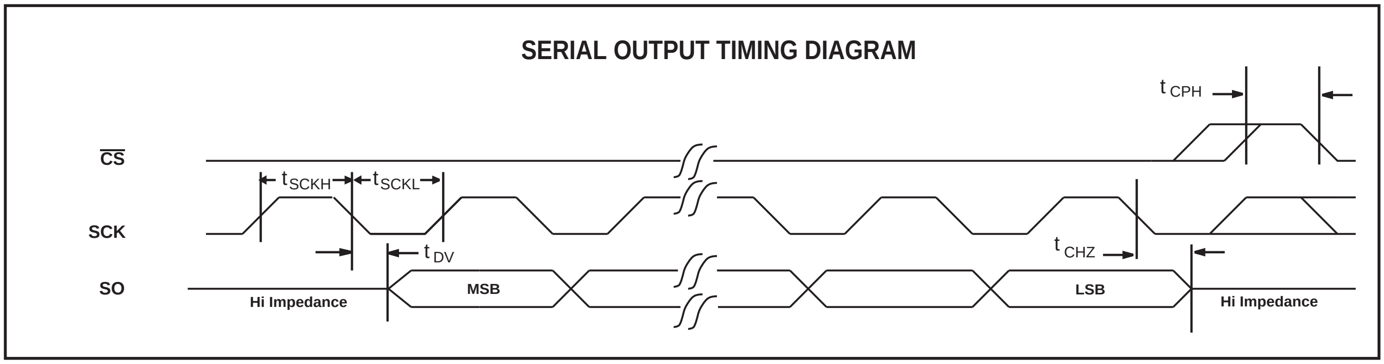
Assertion of Master Reset (MR) causes immediate termination of data reception. The eight Receive FIFOs are cleared. Status Register FIFO flags and FIFO status output signals are also cleared. Master Reset does not affect the eight channel Control Registers. Master Reset may be asserted using the MR input pin (HI-3596 and HI-3598 only) or by executing SPI instruction n7 hex.

An individual receive channel can be reset by setting its corresponding Control Register CR3 bit to “1”. This clears the channel’s receiver logic and Receive FIFO and disables the receiver until CR3 is reset to “0”. For applications requiring less than eight channels, unused receivers should be held in reset by setting the corresponding Control Register CR3 bits.

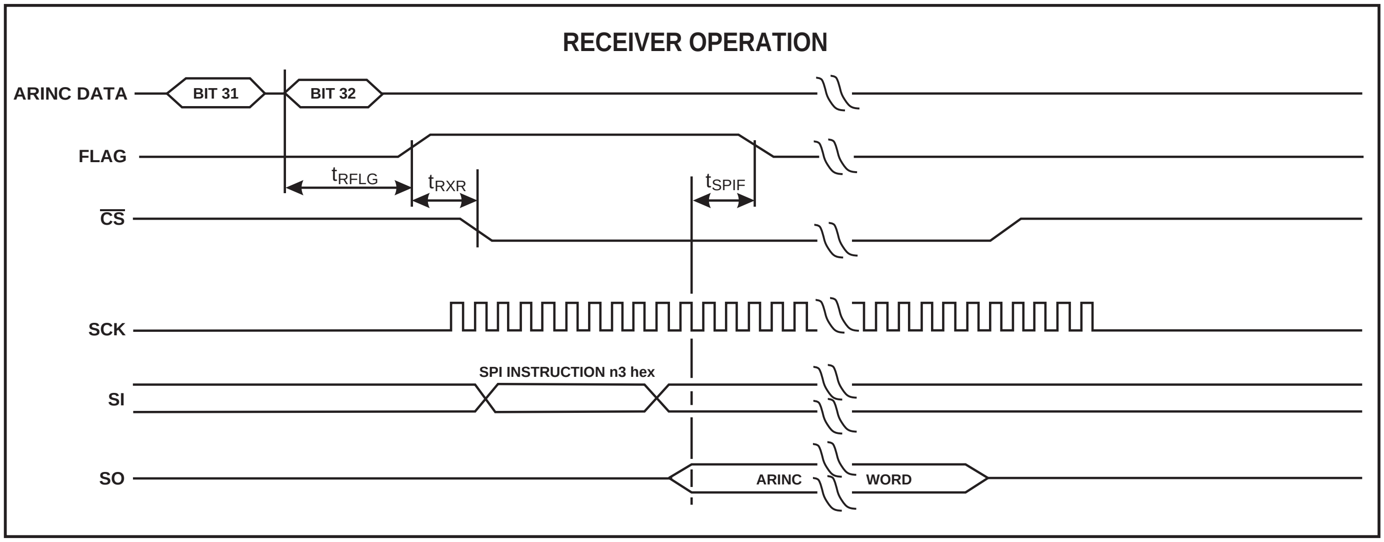
TIMING DIAGRAMS


SERIAL INPUT TIMING DIAGRAM

$\overline{\text{CS}}$
SCK
SI
t_{CHH}
t_{CES}
t_{DS}
t_{DH}
t_{SCKR}
t_{SCKF}
t_{CEH}
t_{CPH}
MSB
LSB


SERIAL OUTPUT TIMING DIAGRAM

$\overline{\text{CS}}$
SCK
SO
t_{SCKH}
t_{SCKL}
t_{DV}
t_{CHZ}
t_{CPH}
Hi Impedance
MSB
LSB
Hi Impedance


RECEIVER OPERATION

ARINC DATA
BIT 31
BIT 32
FLAG
t_{RFLG}
t_{RXR}
t_{SPIF}
$\overline{\text{CS}}$
SCK
SI
SPI INSTRUCTION n3 hex
SO
ARINC
WORD

Figure 5. Timing Diagrams

ABSOLUTE MAXIMUM RATINGS

Supply Voltages V_{DD} .... -0.3 to +7.0V	Power dissipation at 25°C Plastic Quad Flat Pack .... 1.5 W, derate 10mW/°C
Voltage at pins RIN1A, RIN1B, RIN2A, RIN2B .... -29V to +29V	DC Current Drain per pin .... ±10mA
Voltage at any other pin .... -0.3V to V_{DD}+0.3V	Storage Temperature Range .... -65°C to +150°C
Solder temperature (Leads) .... 280°C for 10 seconds (Package) .... 220°C	Operating Temperature Range (Industrial) .... -40°C to +85°C (Extended Temp) .... -55°C to +125°C

NOTE: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

Table 11. DC Electrical Characteristics

V_{DD} = 3.3V or 5.0V, GND = 0V, T_A = Operating Temperature Range (unless otherwise stated)

Parameters		Symbol	Test Conditions	Limits			Unit
				Min	Typ	Max	
ARINC INPUTS - Pins RINA, RINB, RINA-40 (with external 40KΩ), RINB-40 (with external 40KΩ)							
Differential Input Voltage	ONE	V_{IH}	Common mode voltages less than ±30V with respect to GND	6.5	10.0	13.0	V
(RIN1A to RIN1B, RIN2A	ZERO	V_{IL}		-13.0	-10.0	-6.5	V
to RIN2B, etc.)	NULL	V_{NUL}		-2.5	0	2.5	V
Input Resistance	Differential	R_I		-	140	-	kΩ
	To GND	R_G		-	140	-	kΩ
	To V_{DD}	R_H		-	100	-	kΩ
Input Current	Input Sink	I_{IH}		-	-	200	µA
	Input Source	I_{IL}		-450	-	-	µA
Inpit Capacitance	Differential	C_I	(RINA to RINB)	-	-	20	pF
(Guaranteed but not	To GND	C_G		-	-	20	pF
tested)	To V_{DD}	C_H		-	-	20	pF
LOGIC INPUTS							
Input Voltage	Input Voltage HI	V_{IH}		70% V_{DD}	-	-	V
	Input Voltage LO	V_{IL}		-	-	30% V_{DD}	V
Input Current	Input Sink	I_{IH}		-	-	1.5	µA
	Input Source	I_{IL}		-1.5	-	-	µA
	Pull-down Current (MR, SI, SCK, ACLK pins)	I_{PD}		250	-	600	µA
	Pull-up Current ($\overline{\text{CS}}$)	I_{PU}		-600	-	-250	µA
LOGIC OUTPUTS							
Output Voltage	Logic “1” Output Voltage	V_{OH}	I_{OH} = -100µA	90% V_{DD}	-	-	V
	Logic “0” Output Voltage	V_{OL}	I_{OL} = 1.0mA	-	-	10% V_{DD}	V

Parameters		Symbol	Test Conditions	Limits			Unit
				Min	Typ	Max	
Output Current (All outputs and Bi-directional pins)	Output Sink Output Source	I_{OH} I_{OL}	$V_{OUT} = 0.4V$ $V_{OUT} = V_{DD} - 0.4V$	1.6 -	- -	- -1.0	mA mA
Output Capacitance		C_O		-	15	-	pF
OPERATING VOLTAGE RANGE							
		V_{DD}		3.15	-	5.25	V
OPERATING SUPPLY CURRENT							
		I_{DD}		-	2.5	7.0	mA

Table 12. AC electrical characteristics

VDD = 3.3V or 5.0V, GND = 0V, T_A = Operating Temperature Range and f_{clk}=1MHz ±0.1% with 60/40 duty cycle

Parameters	Symbol	Limits			Units
		Min	Typ	Max	
SPI INTERFACE TIMING					
SCK clock Period	t_{CYC}	130	-	-	ns
$\overline{CS}$ active after last SCK rising edge	t_{CHH}	25	-	-	ns
$\overline{CS}$ setup time to first SCK rising edge	t_{CES}	10	-	-	ns
$\overline{CS}$ hold time after last SCK falling edge	t_{CEH}	10	-	-	ns
$\overline{CS}$ inactive between SPI instructions	t_{CPH}	30	-	-	ns
SPI SI Data set-up time to SCK rising edge	t_{DS}	10	-	-	ns
SPI SI Data hold time after SCK rising edge	t_{DH}	30	-	-	ns
SCK rise time	t_{SCKR}	-	-	10	ns
SCK fall time	t_{SCKF}	-	-	10	ns
SCK high time	t_{SCKH}	45	-	-	ns
SCK low time	t_{SCKL}	25	-	-	ns
SO valid after SCK falling edge	t_{DV}	-	-	65	ns
SO high-impedance after SCK falling edge	t_{CHZ}	-	-	65	ns
RECEIVER TIMING					
Delay - Last bit of received ARINC word to FLAG (Full or Empty) - Hi Speed Delay - Last bit of received ARINC word to FLAG (Full or Empty) - Lo Speed	t_{RFLG} t_{RFLG}	- -	- -	16 126	μs μs
Received data available to SPI interface. FLAG to $\overline{CS}$ active	t_{RXR}	0	-	-	ns
SPI receiver read	t_{SPIF}	-	-	85	ns

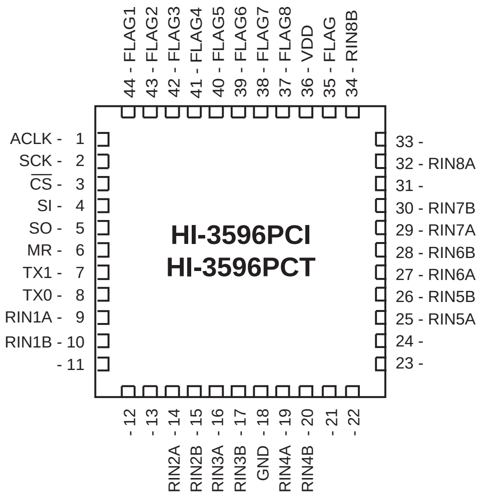
HEAT SINK - CHIP SCALE PACKAGE (QFN) ONLY

The HI-3596PCx, HI-3598PCx, and HI3599PCx use 44-pin or 64-pin plastic chip-scale (QFN) packages. These packages have a metal heat sink pad on the bottom surface that is electrically connected to the die. For these receivers, small size is the primary advantage of this package style. Heat sinking provides little benefit because power dissipation is low. If connected, the bottom heat sink pad should be connected to VDD.

Do not connect heat sink pad to GND.

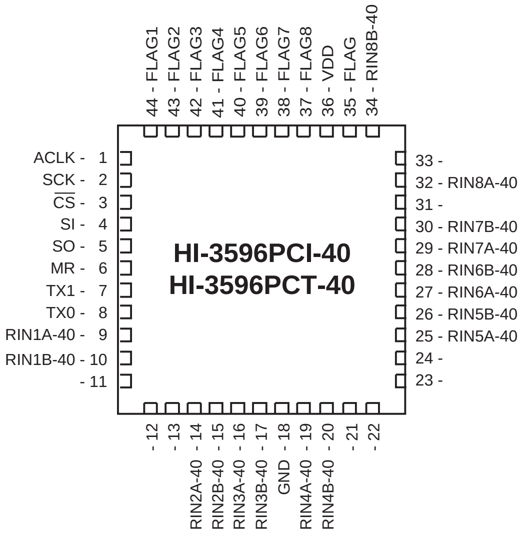
ADDITIONAL PIN / PACKAGE CONFIGURATIONS

HI-3596PCx


44 - FLAG1
43 - FLAG2
42 - FLAG3
41 - FLAG4
40 - FLAG5
39 - FLAG6
38 - FLAG7
37 - FLAG8
36 - VDD
35 - FLAG
34 - RIN8B
ACLK - 1
SCK - 2
CS - 3
SI - 4
SO - 5
MR - 6
TX1 - 7
TX0 - 8
RIN1A - 9
RIN1B - 10
- 11
HI-3596PCI
HI-3596PCT
33 -
32 - RIN8A
31 -
30 - RIN7B
29 - RIN7A
28 - RIN6B
27 - RIN6A
26 - RIN5B
25 - RIN5A
24 -
23 -
- 12
- 13
RIN2A - 14
RIN2B - 15
RIN3A - 16
RIN3B - 17
GND - 18
RIN4A - 19
RIN4B - 20
- 21
- 22

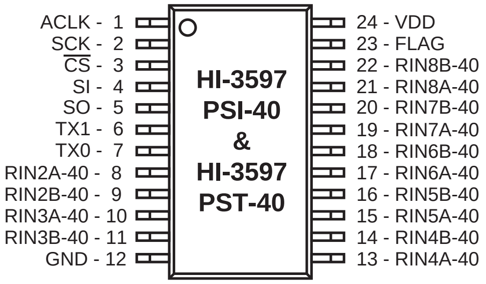
44-Pin Plastic 7mm x 7mm
Chip-Scale Package (QFN)

HI-3596PCx-40


44 - FLAG1
43 - FLAG2
42 - FLAG3
41 - FLAG4
40 - FLAG5
39 - FLAG6
38 - FLAG7
37 - FLAG8
36 - VDD
35 - FLAG
34 - RIN8B-40
ACLK - 1
SCK - 2
CS - 3
SI - 4
SO - 5
MR - 6
TX1 - 7
TX0 - 8
RIN1A-40 - 9
RIN1B-40 - 10
- 11
HI-3596PCI-40
HI-3596PCT-40
33 -
32 - RIN8A-40
31 -
30 - RIN7B-40
29 - RIN7A-40
28 - RIN6B-40
27 - RIN6A-40
26 - RIN5B-40
25 - RIN5A-40
24 -
23 -
- 12
- 13
RIN2A-40 - 14
RIN2B-40 - 15
RIN3A-40 - 16
RIN3B-40 - 17
GND - 18
RIN4A-40 - 19
RIN4B-40 - 20
- 21
- 22

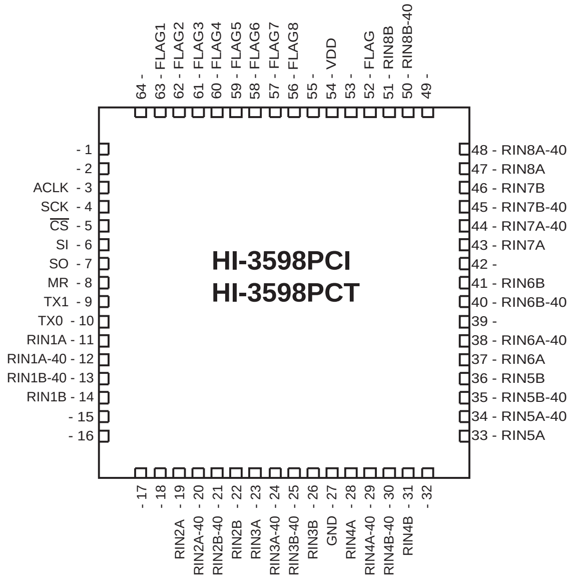
44-Pin Plastic 7mm x 7mm
Chip-Scale Package (QFN)

HI-3597PSx-40


ACLK - 1
SCK - 2
CS - 3
SI - 4
SO - 5
TX1 - 6
TX0 - 7
RIN2A-40 - 8
RIN2B-40 - 9
RIN3A-40 - 10
RIN3B-40 - 11
GND - 12
HI-3597
PSI-40
&
HI-3597
PST-40
24 - VDD
23 - FLAG
22 - RIN8B-40
21 - RIN8A-40
20 - RIN7B-40
19 - RIN7A-40
18 - RIN6B-40
17 - RIN6A-40
16 - RIN5B-40
15 - RIN5A-40
14 - RIN4B-40
13 - RIN4A-40

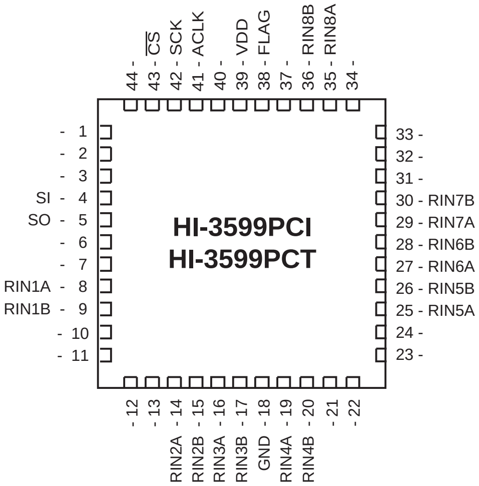
24 - Pin Plastic Small Outline Package (SOIC)

HI-3598PCx


64 -
63 - FLAG1
62 - FLAG2
61 - FLAG3
60 - FLAG4
59 - FLAG5
58 - FLAG6
57 - FLAG7
56 - FLAG8
55 -
54 - VDD
53 -
52 - FLAG
51 - RIN8B
50 - RIN8B-40
49 -
- 1
- 2
ACLK - 3
SCK - 4
CS - 5
SI - 6
SO - 7
MR - 8
TX1 - 9
TX0 - 10
RIN1A - 11
RIN1A-40 - 12
RIN1B-40 - 13
RIN1B - 14
- 15
- 16
HI-3598PCI
HI-3598PCT
48 - RIN8A-40
47 - RIN8A
46 - RIN7B
45 - RIN7B-40
44 - RIN7A-40
43 - RIN7A
42 -
41 - RIN6B
40 - RIN6B-40
39 -
38 - RIN6A-40
37 - RIN6A
36 - RIN5B
35 - RIN5B-40
34 - RIN5A-40
33 - RIN5A
- 17
- 18
RIN2A - 19
RIN2A-40 - 20
RIN2B-40 - 21
RIN2B - 22
RIN3A - 23
RIN3A-40 - 24
RIN3B-40 - 25
RIN3B - 26
GND - 27
RIN4A - 28
RIN4A-40 - 29
RIN4B-40 - 30
RIN4B - 31
- 32

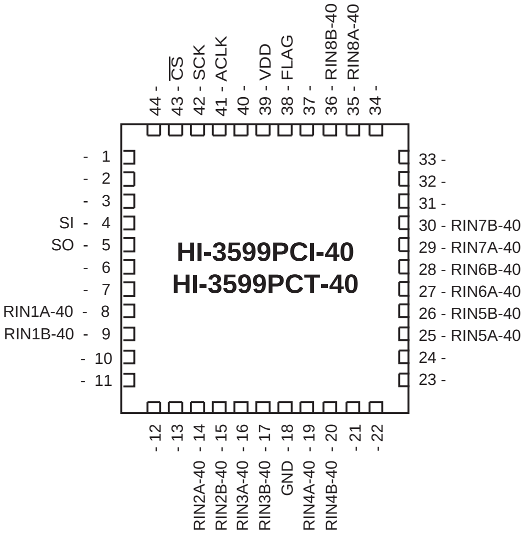
64-Pin Plastic 9mm x 9mm
Chip-Scale Package (QFN)

HI-3599PCx


HI-3599PCI
HI-3599PCT
44 -
43 - CS
42 - SCK
41 - ACLK
40 -
39 - VDD
38 - FLAG
37 -
36 - RIN8B
35 - RIN8A
34 -
- 1
- 2
- 3
SI - 4
SO - 5
- 6
- 7
RIN1A - 8
RIN1B - 9
- 10
- 11
33 -
32 -
31 -
30 - RIN7B
29 - RIN7A
28 - RIN6B
27 - RIN6A
26 - RIN5B
25 - RIN5A
24 -
23 -
- 12
- 13
RIN2A - 14
RIN2B - 15
RIN3A - 16
RIN3B - 17
GND - 18
RIN4A - 19
RIN4B - 20
- 21
- 22

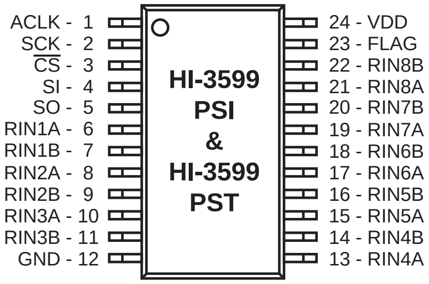
44-Pin Plastic 7mm x 7mm
Chip-Scale Package (QFN)

HI-3599PCx-40


HI-3599PCI-40
HI-3599PCT-40
44 -
43 - CS
42 - SCK
41 - ACLK
40 -
39 - VDD
38 - FLAG
37 -
36 - RIN8B-40
35 - RIN8A-40
34 -
- 1
- 2
- 3
SI - 4
SO - 5
- 6
- 7
RIN1A-40 - 8
RIN1B-40 - 9
- 10
- 11
33 -
32 -
31 -
30 - RIN7B-40
29 - RIN7A-40
28 - RIN6B-40
27 - RIN6A-40
26 - RIN5B-40
25 - RIN5A-40
24 -
23 -
- 12
- 13
RIN2A-40 - 14
RIN2B-40 - 15
RIN3A-40 - 16
RIN3B-40 - 17
GND - 18
RIN4A-40 - 19
RIN4B-40 - 20
- 21
- 22

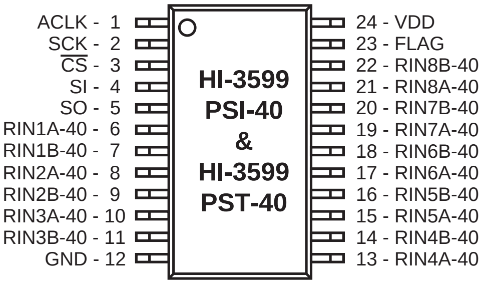
44-Pin Plastic 7mm x 7mm
Chip-Scale Package (QFN)

HI-3599PSx


HI-3599
PSI
&
HI-3599
PST
ACLK - 1
SCK - 2
CS - 3
SI - 4
SO - 5
RIN1A - 6
RIN1B - 7
RIN2A - 8
RIN2B - 9
RIN3A - 10
RIN3B - 11
GND - 12
24 - VDD
23 - FLAG
22 - RIN8B
21 - RIN8A
20 - RIN7B
19 - RIN7A
18 - RIN6B
17 - RIN6A
16 - RIN5B
15 - RIN5A
14 - RIN4B
13 - RIN4A

24 - Pin Plastic Small Outline Package (SOIC)

HI-3599PSx-40


HI-3599
PSI-40
&
HI-3599
PST-40
ACLK - 1
SCK - 2
CS - 3
SI - 4
SO - 5
RIN1A-40 - 6
RIN1B-40 - 7
RIN2A-40 - 8
RIN2B-40 - 9
RIN3A-40 - 10
RIN3B-40 - 11
GND - 12
24 - VDD
23 - FLAG
22 - RIN8B-40
21 - RIN8A-40
20 - RIN7B-40
19 - RIN7A-40
18 - RIN6B-40
17 - RIN6A-40
16 - RIN5B-40
15 - RIN5A-40
14 - RIN4B-40
13 - RIN4A-40

24 - Pin Plastic Small Outline Package (SOIC)

ORDERING INFORMATION (HI-3598 all pins)

HI - 3598 xx x x

PART NUMBER	LEAD FINISH
Blank	Tin / Lead (Sn / Pb) Solder
F	100% Matte Tin (Pb-free, RoHS compliant)

PART NUMBER	TEMPERATURE RANGE	FLOW	BURN IN
I	-40°C to +85°C	I	No
T	-55°C to +125°C	T	No

PART NUMBER	PACKAGE DESCRIPTION
PC	64 PIN PLASTIC CHIP-SCALE PACKAGE, QFN (64PCS)
PQ	52 PIN PLASTIC QUAD FLAT PACK, PQFP (52PTQS)

ORDERING INFORMATION (HI-3596[1], HI-3597[2] & HI-3599)

HI - 359x xx x x - xx

PART NUMBER	INPUT RESISTANCE
Blank	140kΩ. Direct connection to ARINC 429 bus
-40	100kΩ. Requires external 40kΩ resistors

PART NUMBER	LEAD FINISH
Blank	Tin / Lead (Sn / Pb) Solder
F	100% Matte Tin (Pb-free, RoHS compliant)

PART NUMBER	TEMPERATURE RANGE	FLOW	BURN IN
I	-40°C to +85°C	I	No
T	-55°C to +125°C	T	No

PART NUMBER	PACKAGE DESCRIPTION
PC	44 PIN PLASTIC CHIP-SCALE PACKAGE, QFN (44PCS)
PS	24 PIN PLASTIC WIDE SOIC, (24HW)

PART NUMBER	DIGITAL TRANSMIT FUNCTION
3596[1]	Yes
3597[2]	Yes
3599	No

[1] **Not available in PSx package.**

[2] **Not available in PCx package.**

REVISION HISTORY

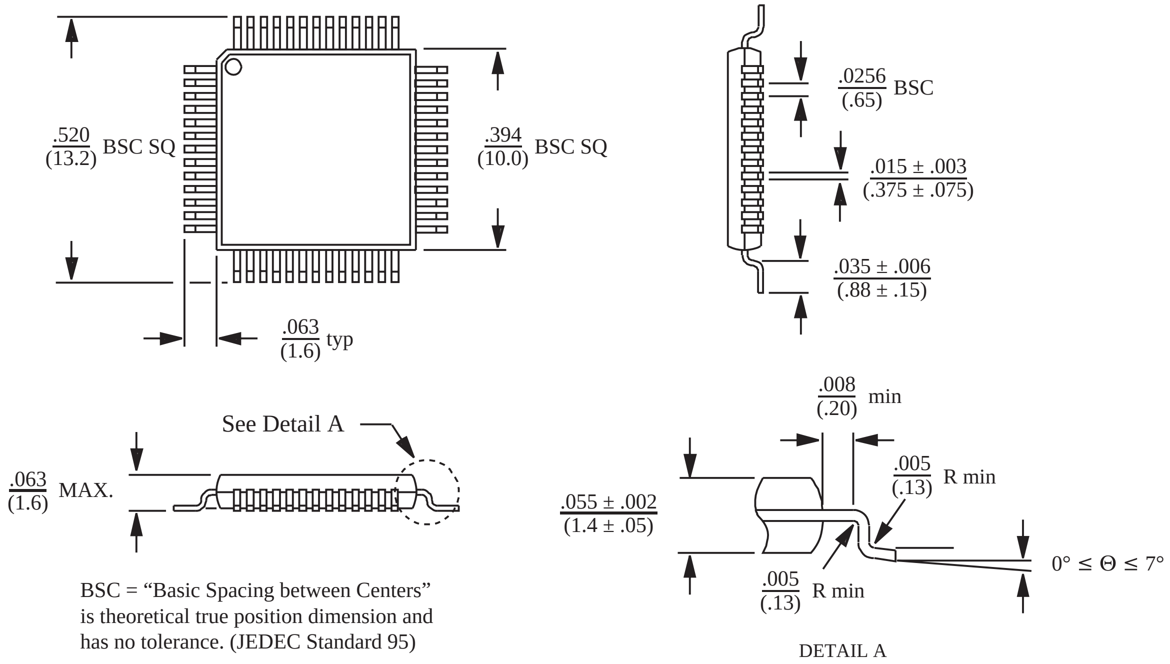
Revision	Date	Description of Change
DS3598, Rev. NEW	6/12/08	Initial Release.
Rev. A	5/22/09	Clarified relationship between SPI bit order and ARINC 429 bit order.
Rev. B	11/23/09	Corrected typo on receivers pin nomenclature on page 3. Added and updated Figure and Table cross-references. Condensed Control and Status Register tables. Corrected minor typos. Clarified certain functional descriptions. Added HI3596 & HI-3597 variants to datasheet.

PACKAGE DIMENSIONS

52-PIN PLASTIC QUAD FLAT PACK (PQFP)

inches (millimeters)

Package Type: 52PTQS

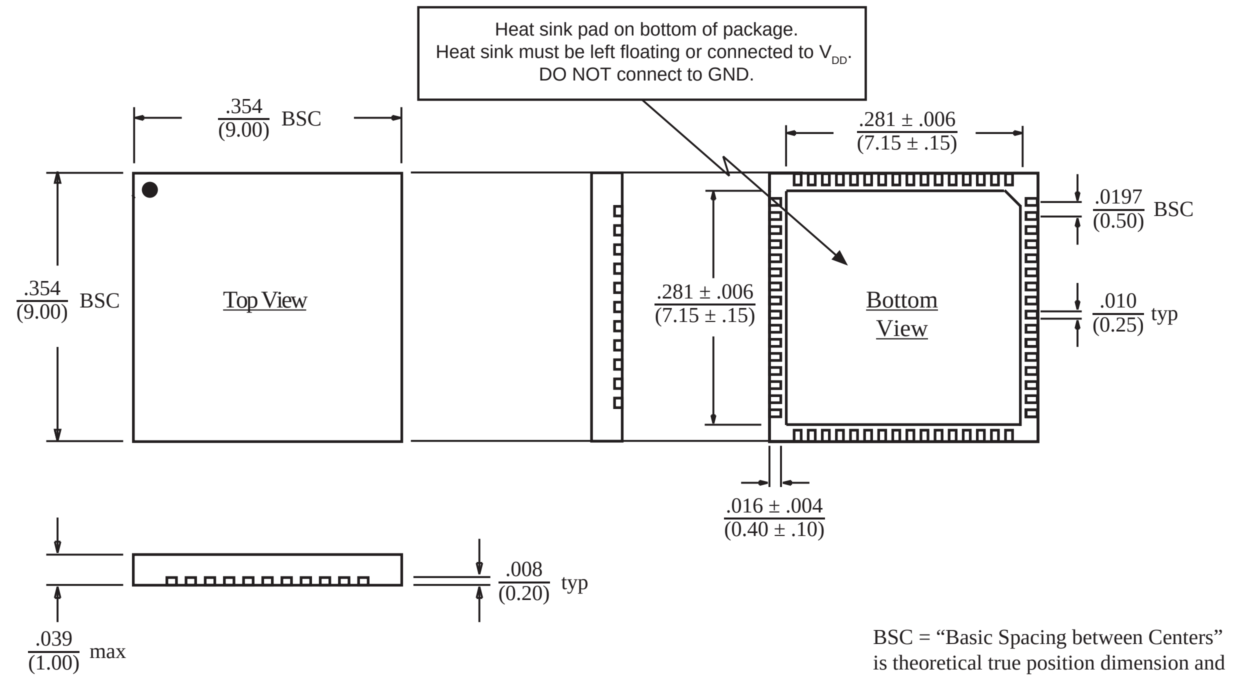

.520 (13.2) BSC SQ
.394 (10.0) BSC SQ
.063 (1.6) typ
.0256 (.65) BSC
.015 ± .003 (.375 ± .075)
.035 ± .006 (.88 ± .15)
See Detail A
.063 (1.6) MAX.
.008 (.20) min
.005 (.13) R min
.055 ± .002 (1.4 ± .05)
.005 (.13) R min
0° ≤ Θ ≤ 7°
DETAIL A

BSC = "Basic Spacing between Centers" is theoretical true position dimension and has no tolerance. (JEDEC Standard 95)

64-PIN PLASTIC CHIP-SCALE PACKAGE (QFN)

inches (millimeters)

Package Type: 64PCS


Heat sink pad on bottom of package.
Heat sink must be left floating or connected to V_{DD}.
DO NOT connect to GND.

.354 (9.00) BSC
.281 ± .006 (7.15 ± .15)
.0197 (0.50) BSC
.354 (9.00) BSC
Top View
.281 ± .006 (7.15 ± .15)
Bottom View
.010 (0.25) typ
.016 ± .004 (0.40 ± .10)
.008 (0.20) typ
.039 (1.00) max

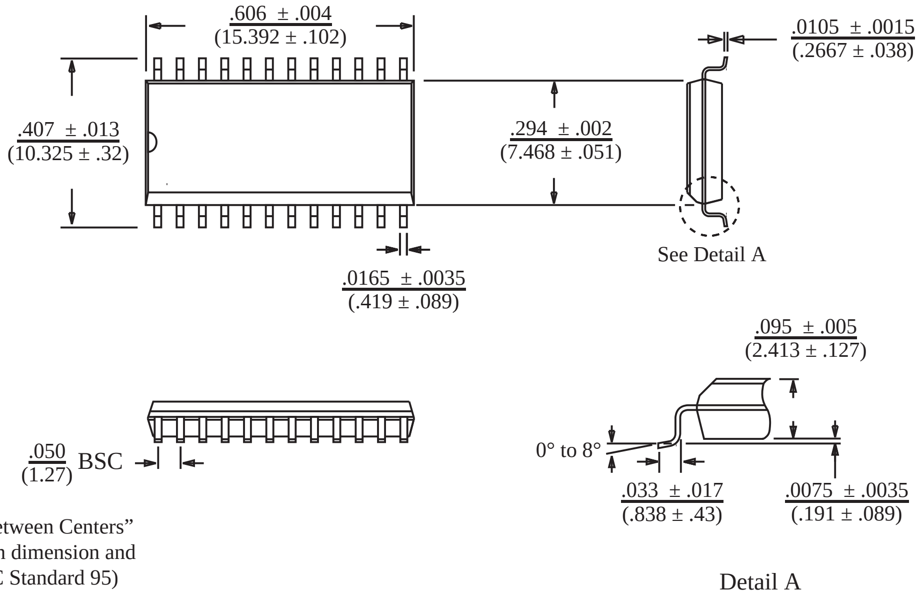
BSC = "Basic Spacing between Centers" is theoretical true position dimension and has no tolerance. (JEDEC Standard 95)

24-PIN PLASTIC SMALL OUTLINE (SOIC) - WB

(Wide Body)

inches (millimeters)

Package Type: 24HW

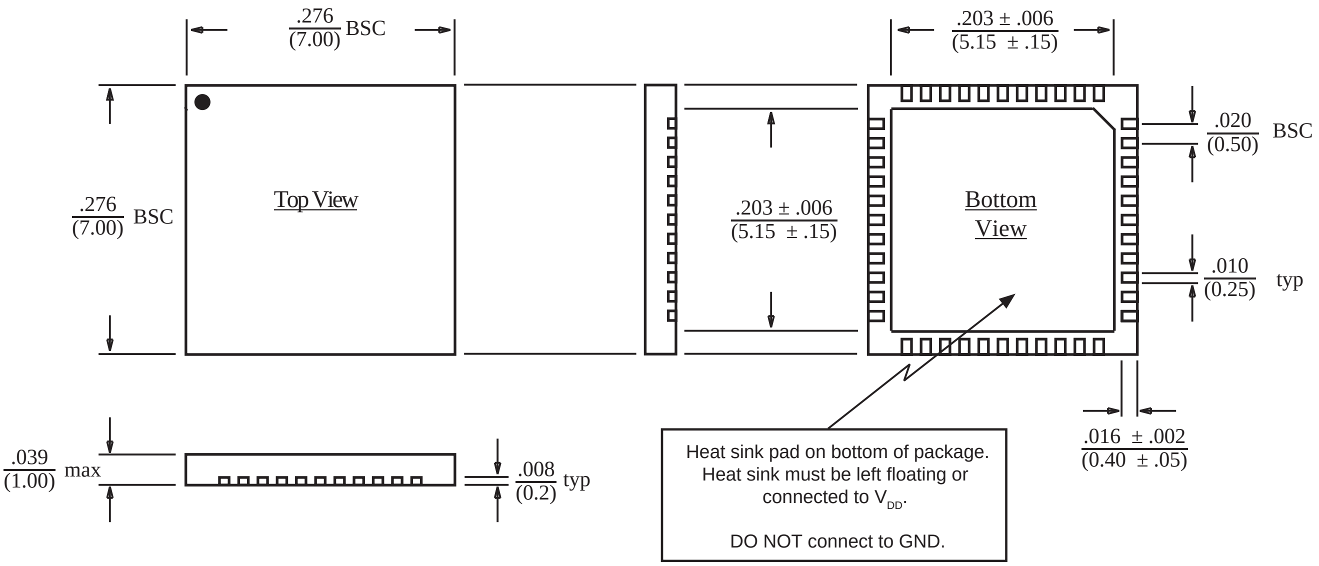

.606 ± .004
(15.392 ± .102)
.0105 ± .0015
(.2667 ± .038)
.407 ± .013
(10.325 ± .32)
.294 ± .002
(7.468 ± .051)
See Detail A
.0165 ± .0035
(.419 ± .089)
.095 ± .005
(2.413 ± .127)
.050
(1.27)
BSC
0° to 8°
.033 ± .017
(.838 ± .43)
.0075 ± .0035
(.191 ± .089)
Detail A

BSC = "Basic Spacing between Centers" is theoretical true position dimension and has no tolerance. (JEDEC Standard 95)

44-PIN PLASTIC CHIP-SCALE PACKAGE (QFN)

inches (millimeters)

Package Type: 44PCS


.276
(7.00)
BSC
.203 ± .006
(5.15 ± .15)
.276
(7.00)
BSC
Top View
.203 ± .006
(5.15 ± .15)
Bottom
View
.020
(0.50)
BSC
.010
(0.25)
typ
.016 ± .002
(0.40 ± .05)
.039
(1.00)
max
.008
(0.2)
typ

Heat sink pad on bottom of package. Heat sink must be left floating or connected to V_{DD}.

DO NOT connect to GND.

BSC = "Basic Spacing between Centers" is theoretical true position dimension and has no tolerance. (JEDEC Standard 95)