

Linear Systems Monolithic Dual PNP Transistor

The LS3550B is a monolithic pair of PNP transistors mounted in a single SOIC package. The monolithic dual chip design reduces parasitics and gives better performance while ensuring extremely tight matching.

The 8 Pin SOIC provides ease of manufacturing, and the symmetrical pinout prevents improper orientation.

(See Packaging Information).

LS3550B Features:

- Tight matching
- Low Output Capacitance

FEATURES

EXCELLENT THERMAL TRACKING	$\leq 5\mu\text{V}/^\circ\text{C}$
TIGHT V_{BE} MATCHING	$ V_{BE1} - V_{BE2} \leq 5\text{mV}$
ABSOLUTE MAXIMUM RATINGS ¹ @ 25°C (unless otherwise noted)	
Maximum Temperatures	
Storage Temperature	-65°C to +150°C
Operating Junction Temperature	-55°C to +150°C
Maximum Power Dissipation	
Continuous Power Dissipation	TBD
Maximum Currents	
Collector Current	10mA
Maximum Voltages	
Collector to Collector Voltage	80V

MATCHING CHARACTERISTICS @ 25°C (unless otherwise stated)

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
$ V_{BE1} - V_{BE2} $	Base Emitter Voltage Differential	--	--	5	mV	$I_C = -10\text{mA}, V_{CE} = -5\text{V}$
$\Delta (V_{BE1} - V_{BE2}) /\Delta T$	Base Emitter Voltage Differential Change with Temperature	--	--	5	$\mu\text{V}/^\circ\text{C}$	$I_C = -10\text{mA}, V_{CE} = -5\text{V}$ $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$
$ I_{B1} - I_{B2} $	Base Current Differential	--	--	10	nA	$I_C = -10\mu\text{A}, V_{CE} = -5\text{V}$
$ \Delta(I_{B1} - I_{B2}) /\Delta T$	Base Current Differential Change with Temperature	--	--	0.5	$\text{nA}/^\circ\text{C}$	$I_C = -10\mu\text{A}, V_{CE} = -5\text{V}$ $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$
h_{FE1}/h_{FE2}	DC Current Gain Differential	--	--	10	%	$I_C = 10\mu\text{A}, V_{CE} = 5\text{V}$

ELECTRICAL CHARACTERISTICS @ 25°C (unless otherwise noted)

SYMBOL	CHARACTERISTICS	MIN.	TYP.	MAX.	UNITS	CONDITIONS
V_{CBO}	Collector to Base Voltage	-40	--	--	V	$I_C = 10\mu\text{A}, I_E = 0$
V_{CEO}	Collector to Emitter Voltage	-40	--	--	V	$I_C = 10\mu\text{A}, I_B = 0$
V_{EBO}	Emitter-Base Breakdown Voltage	-6.2	--	--	V	$I_E = 10\mu\text{A}, I_C = 0^2$
V_{CCO}	Collector to Collector Voltage	-80	--	--	V	$I_C = 10\mu\text{A}, I_E = 0$
h_{FE}	DC Current Gain	100	--	--		$I_C = -1\text{mA}, V_{CE} = -5\text{V}$
		80	--	--		$I_C = -10\text{mA}, V_{CE} = -5\text{V}$
		80	--	--		$I_C = -100\text{mA}, V_{CE} = -5\text{V}$
$V_{CE(SAT)}$	Collector Saturation Voltage	--	--	-0.25	V	$I_C = -100\text{mA}, I_B = -10\text{mA}$
I_{EBO}	Emitter Cutoff Current	--	--	-0.2	nA	$I_E = 0, V_{CB} = -3\text{V}$
I_{CBO}	Collector Cutoff Current	--	--	-0.2	nA	$I_E = 0, V_{CB} = -30\text{V}$
C_{OBO}	Output Capacitance	--	--	2	pF	$I_E = 0, V_{CB} = -10\text{V}$
C_{C1C2}	Collector to Collector Capacitance	--	--	2	pF	$V_{CC} = 0\text{V}$
I_{C1C2}	Collector to Collector Leakage Current	--	--	-1	nA	$V_{CC} = \pm 80\text{V}$
f_T	Current Gain Bandwidth Product(Current)	--	--	600	MHz	$I_C = -1\text{mA}, V_{CE} = -5\text{V}$
NF	Narrow Band Noise Figure	--	--	3	dB	$I_C = -100\mu\text{A}, V_{CE} = -5\text{V}, \text{BW} = 200\text{Hz}, R_G = 10\Omega, f = 1\text{KHz}$

Notes:

1. Absolute Maximum ratings are limiting values above which serviceability may be impaired
2. The reverse base-to-emitter voltage must never exceed 6.2 volts; the reverse base-to-emitter current must never exceed 10 μA .

Available Packages:

LS3550B in SOIC
LS3550B available as bare die

Please contact Micross for full package and die dimensions:

Email: chipcomponents@micross.com
Web: www.micross.com/distribution.aspx

SOIC (Top View)

