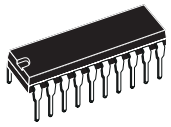
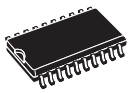
M74HC354

8 CHANNEL MULTIPLEXER/REGISTER (3 STATE)

- HIGH SPEED:
  t_{PD} = 27 ns (TYP.) at V_{CC} = 6V
- LOW POWER DISSIPATION:
  I_{CC} = 4µA(MAX.) at T_A=25°C
- HIGH NOISE IMMUNITY:
  $V_{NIH} = V_{NIL}$ = 28 % V_{CC} (MIN.)
- SYMMETRICAL OUTPUT IMPEDANCE:
  $|I_{OH}| = I_{OL}$ = 6mA (MIN)
- BALANCED PROPAGATION DELAYS:
  $t_{PLH} \cong t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE:
  V_{CC} (OPR) = 2V to 6V
- PIN AND FUNCTION COMPATIBLE WITH 74 SERIES 354



DIP



SOP

TSSOP

ORDER CODES

PACKAGE	TUBE	T & R
DIP	M74HC354B1R	
SOP	M74HC354M1R	M74HC354RM13TR
TSSOP		M74HC354TTR

DESCRIPTION

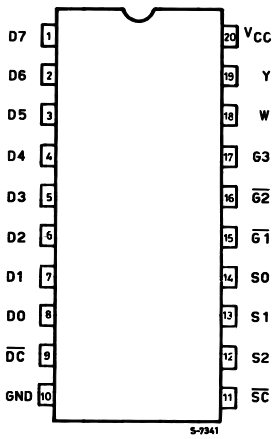
The M74HC354 is an high speed CMOS 8 CHANNEL MULTIPLEXER/REGISTER (3-STATE) fabricated with silicon gate C^2MOS technology.

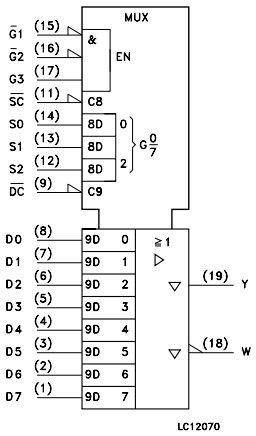
This device contains an 8 channel digital multiplexer with an 8-input data register and a 3-bit address input register with 3-state outputs. The one of eight input data will be provided on the Y output pin (non-inverted output) and W output pin (inverted output) determined by the address data. The information at the data inputs (D0 to D7) is stored in the 8-bit latch at the negative pulse on $\overline{DC}$ input. The information at the address inputs (S0 to S2) is stored in the 3-bit latch at the negative pulse on $\overline{SC}$ input. These outputs are disabled to be high-impedance when inputs $\overline{G1}$, $\overline{G2}$ are held high or input G3 is held low. This device is suitable for interfacing with bus lines in a bus organized system.

The M74HC354 is similar in function to the M74HC356, which has an 8-bit flip-flop as the data register instead of an 8-bit latch.

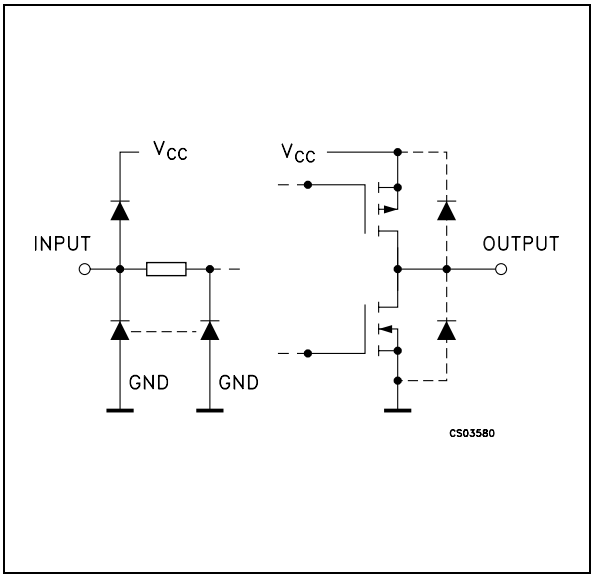
All inputs are equipped with protection circuits against static discharge and transient excess voltage.

PIN CONNECTION AND IEC LOGIC SYMBOLS





INPUT AND OUTPUT EQUIVALENT CIRCUIT



PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
8, 7, 6, 5, 4, 3, 2, 1	D0 to D7	Data Inputs
9	$\overline{DC}$	Data Enable Input (Active LOW)
11	$\overline{SC}$	Latch Enable Input (Active LOW)
14, 13, 12	S0, S1, S2	Select Inputs
15, 16	$\overline{G1}$, $\overline{G2}$	Output Enable Inputs (Active LOW)
17	G3	Output Enable Input (Active HIGH)
18	W	3 - state Multiplexer Output (Active LOW)
19	Y	3 - state Multiplexer Output (Active HIGH)
10	GND	Ground (0V)
20	V_{CC}	Positive Supply Voltage

TRUTH TABLE

INPUTS							OUTPUTS	
SELECT *			$\overline{DC}$	OUTPUT ENABLES			W	Y
S2	S1	S0		G1	$\overline{G2}$	G3		
X	X	X	X	H	X	X	Z	Z
X	X	X	X	X	H	X	Z	Z
X	X	X	X	X	X	L	Z	Z
L	L	L	L	L	L	H	$\overline{D0}$	D0
L	L	L	H	L	L	H	$\overline{D0n}$	D0n
L	L	H	L	L	L	H	$\overline{D1}$	D1
L	L	H	H	L	L	H	$\overline{D1n}$	D1n
L	H	L	L	L	L	H	$\overline{D2}$	D2
L	H	L	H	L	L	H	$\overline{D2n}$	D2n
L	H	H	L	L	L	H	$\overline{D3}$	D3
L	H	H	H	L	L	H	$\overline{D3n}$	D3n
H	L	L	L	L	L	H	$\overline{D4}$	D4
H	L	L	H	L	L	H	$\overline{D4n}$	D4n
H	L	H	L	L	L	H	$\overline{D5}$	D5
H	L	H	H	L	L	H	$\overline{D5n}$	D5n
H	H	L	L	L	L	H	$\overline{D6}$	D6
H	H	L	H	L	L	H	$\overline{D6n}$	D6n
H	H	H	L	L	L	H	$\overline{D7}$	D7
H	H	H	H	L	L	H	$\overline{D7n}$	D7n

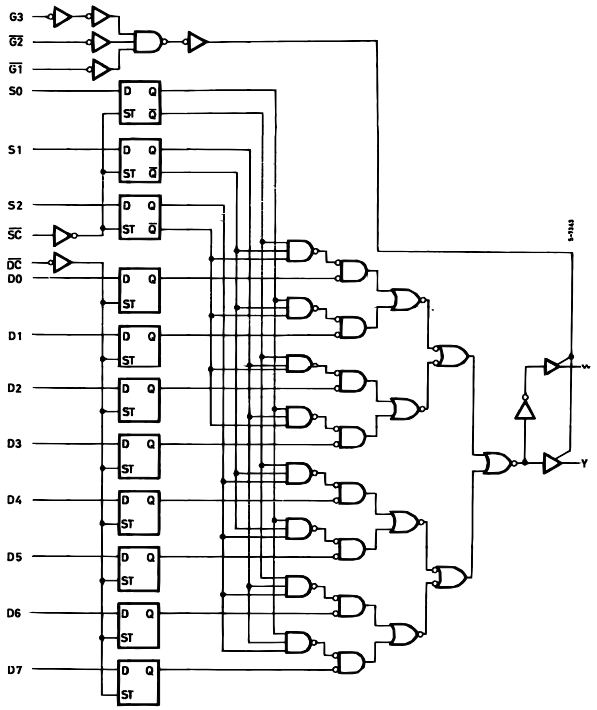
X : Don't Care
Z : High Impedance
* : This Column Shows the Input Address Setup with $\overline{SC}$ low.
D0n....D7n : The level of steady state inputs at input D0 through D7, respectively, before the most recent low to high transition of data control.

TRUTH TABLE OF INTERNAL LATCH

INPUTS		OUTPUTS	
D	**ST**	**Q**	**$\overline{Q}$**
L	H	L	H
H	H	H	L
X	L	Qn	$\overline{Qn}$

X : Don't Care
Qn : Data Stored at the trailing edge of the most recent ST pulse.

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Current	± 35	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 70	mA
P_D	Power Dissipation	500(*)	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied
(*) 500mW at 65 °C; derate to 300mW by 10mW/°C from 65°C to 85°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		2 to 6	V
V_I	Input Voltage		0 to V_{CC}	V
V_O	Output Voltage		0 to V_{CC}	V
T_{op}	Operating Temperature		-55 to 125	°C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2.0V	0 to 1000	ns
		V_{CC} = 4.5V	0 to 500	ns
		V_{CC} = 6.0V	0 to 400	ns

DC SPECIFICATIONS

Symbol	Parameter	Test Condition		Value							Unit
		V_{CC} (V)		T_A = 25°C			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0		1.5			1.5		1.5		V
		4.5		3.15			3.15		3.15		
		6.0		4.2			4.2		4.2		
V_{IL}	Low Level Input Voltage	2.0				0.5		0.5		0.5	V
		4.5				1.35		1.35		1.35	
		6.0				1.8		1.8		1.8	
V_{OH}	High Level Output Voltage	2.0	I_O=-20 µA	1.9	2.0		1.9		1.9		V
		4.5	I_O=-20 µA	4.4	4.5		4.4		4.4		
		6.0	I_O=-20 µA	5.9	6.0		5.9		5.9		
		4.5	I_O=-6.0 mA	4.18	4.31		4.13		4.10		
		6.0	I_O=-7.8 mA	5.68	5.8		5.63		5.60		
V_{OL}	Low Level Output Voltage	2.0	I_O=20 µA		0.0	0.1		0.1		0.1	V
		4.5	I_O=20 µA		0.0	0.1		0.1		0.1	
		6.0	I_O=20 µA		0.0	0.1		0.1		0.1	
		4.5	I_O=6.0 mA		0.17	0.26		0.33		0.40	
		6.0	I_O=7.8 mA		0.18	0.26		0.33		0.40	
I_I	Input Leakage Current	6.0	V_I = V_{CC} or GND			± 0.1		± 1		± 1	µA
I_{OZ}	High Impedance Output Leakage Current	6.0	V_I = V_{IH} or V_{IL} V_O = V_{CC} or GND			± 0.5		± 5		± 5	µA
I_{CC}	Quiescent Supply Current	6.0	V_I = V_{CC} or GND			4		40		80	µA

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6ns)

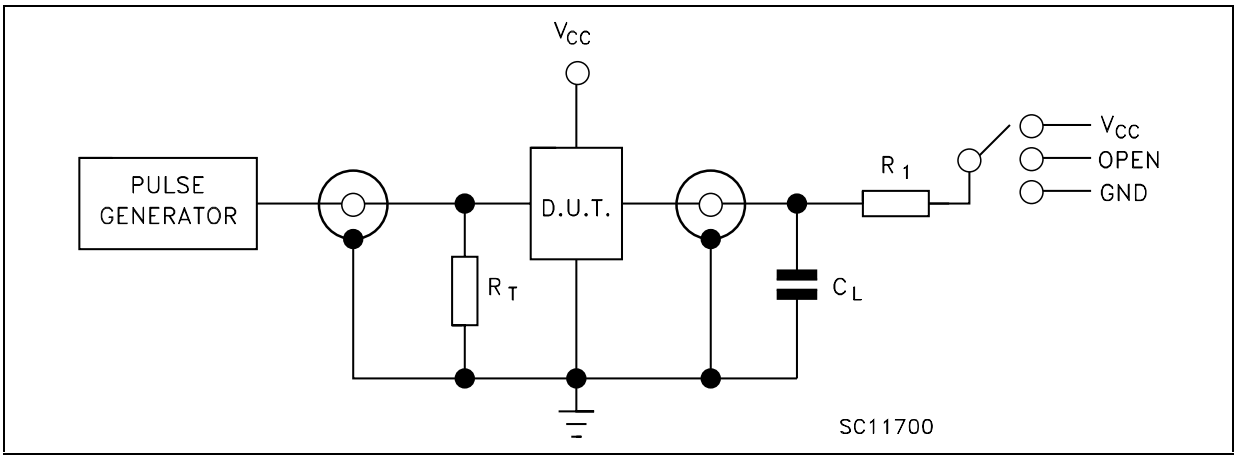
Symbol	Parameter	Test Condition			Value							Unit
		V_{CC} (V)			T_A = 25°C			-40 to 85°C		-55 to 125°C		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0	50			25	60		75		90	ns
		4.5				7	12		15		18	
		6.0				6	10		13		15	
t_{PLH} t_{PHL}	Propagation Delay Time (Dn, $\overline{DC}$ - Y, W)	2.0	50			83	210		265		315	ns
		4.5				26	42		53		63	
		6.0				21	36		45		54	
		2.0	150			99	250		315		375	
		4.5				31	50		63		75	
		6.0				25	43		54		64	
t_{PLH} t_{PHL}	Propagation Delay Time (Sn - Y, W)	2.0	50			98	260		325		390	ns
		4.5				30	52		65		78	
		6.0				25	44		55		66	
		2.0	150			114	300		375		450	
		4.5				35	60		75		90	
		6.0				29	51		64		77	
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{SC}$ - Y, W)	2.0	50			102	270		340		405	ns
		4.5				31	54		68		81	
		6.0				27	46		58		69	
		2.0	150			118	310		390		465	
		4.5				36	62		78		93	
		6.0				31	53		66		79	
t_{PZL} t_{PZH}	High Impedance Output Enable Time	2.0	50	R_L = 1KΩ		44	125		155		190	ns
		4.5				14	25		31		38	
		6.0				12	21		26		32	
		2.0	150	R_L = 1KΩ		60	165		205		250	
		4.5				19	33		41		50	
		6.0				16	28		35		43	
t_{PLZ} t_{PHZ}	High Impedance Output Disable Time	2.0	50	R_L = 1KΩ		42	155		195		235	ns
		4.5				20	31		39		47	
		6.0				17	26		33		40	
$t_{W(L)}$	Minimum Pulse Width ($\overline{DC}$) ($\overline{SC}$)	2.0	50			18	75		95		110	ns
		4.5				6	15		19		22	
		6.0				6	13		16		19	
t_S	Minimum Set-up Time (Dn) (Sn)	2.0	50			10	50		65		75	ns
		4.5				3	10		13		15	
		6.0				3	9		11		13	
t_H	Minimum Hold Time (Dn) (Sn)	2.0	50				5		5		5	ns
		4.5					5		5		5	
		6.0					5		5		5	

CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Test Condition		Value							Unit
		V_{CC} (V)		T_A = 25°C			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
C_{IN}	Input Capacitance	5.0			5	10		10		10	pF
C_{PD}	Power Dissipation Capacitance (note 1)	5.0			77						pF

1) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operating current can be obtained by the following equation. $I_{CC(opr)} = C_{PD} \times V_{CC} \times f_{IN} + I_{CC}$

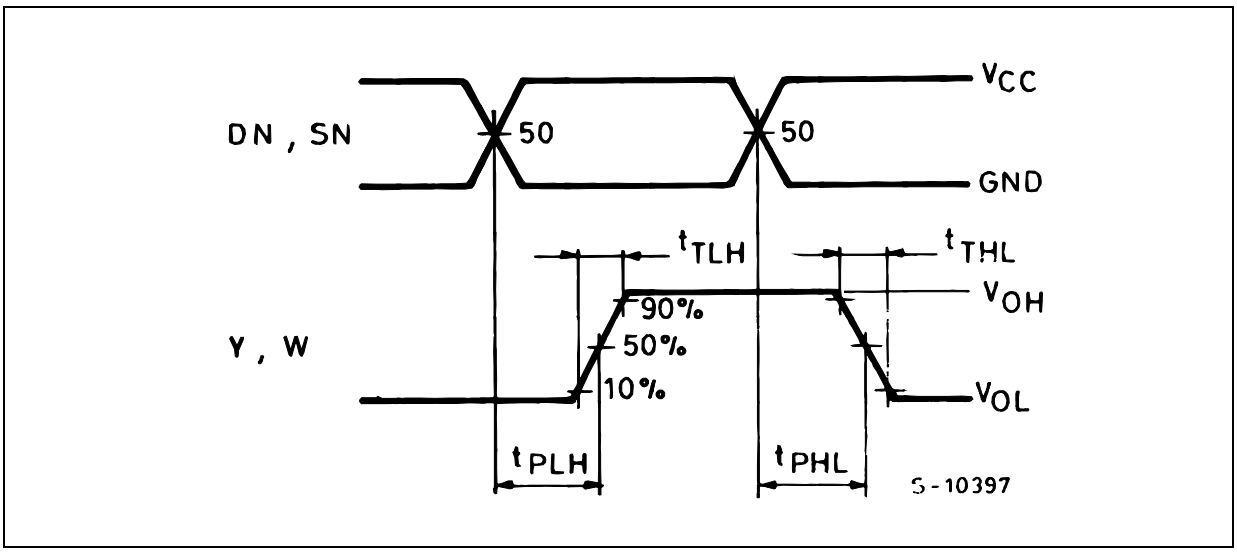
TEST CIRCUIT



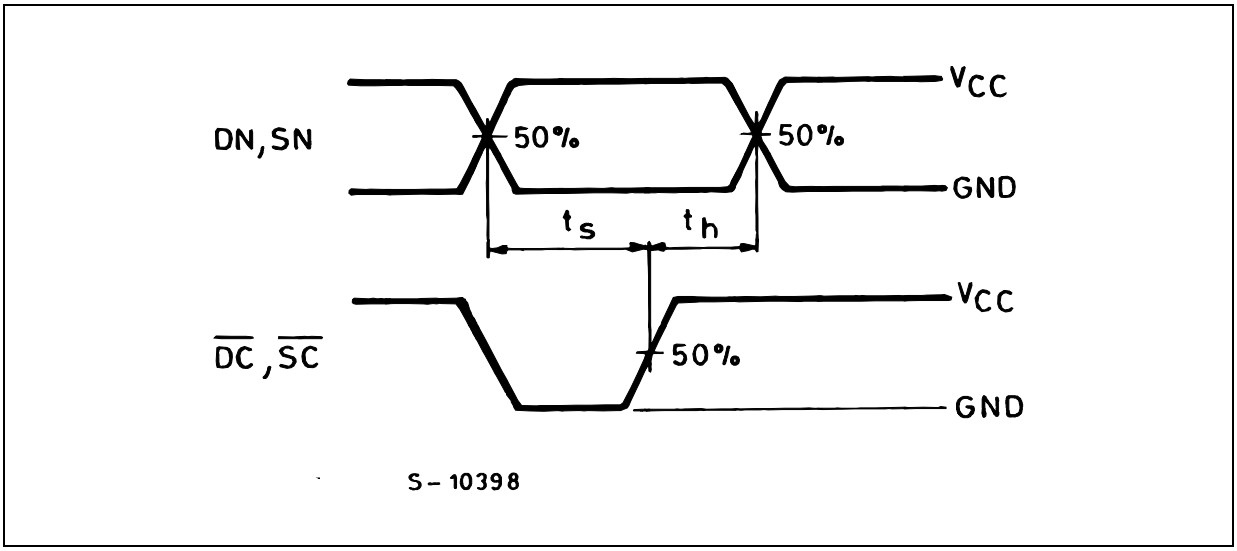
TEST	SWITCH
t_{PLH}, t_{PHL}	Open
t_{PZL}, t_{PLZ}	V_{CC}
t_{PZH}, t_{PHZ}	GND

C_L = 50pF/150pF or equivalent (includes jig and probe capacitance)
R_1 = 1KΩ or equivalent
R_T = Z_{OUT} of pulse generator (typically 50Ω)

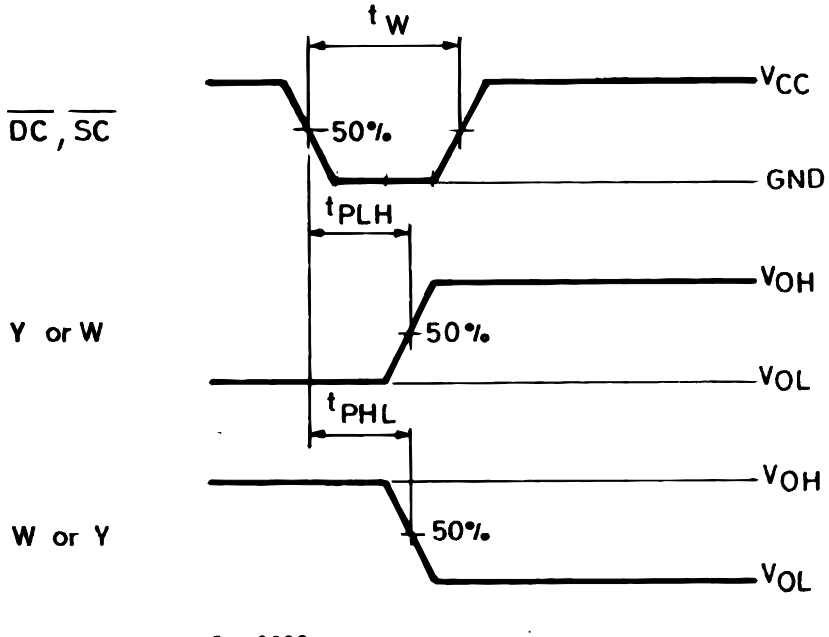
WAVEFORM 1: PROPAGATION DELAY TIME (f=1MHz; 50% duty cycle)



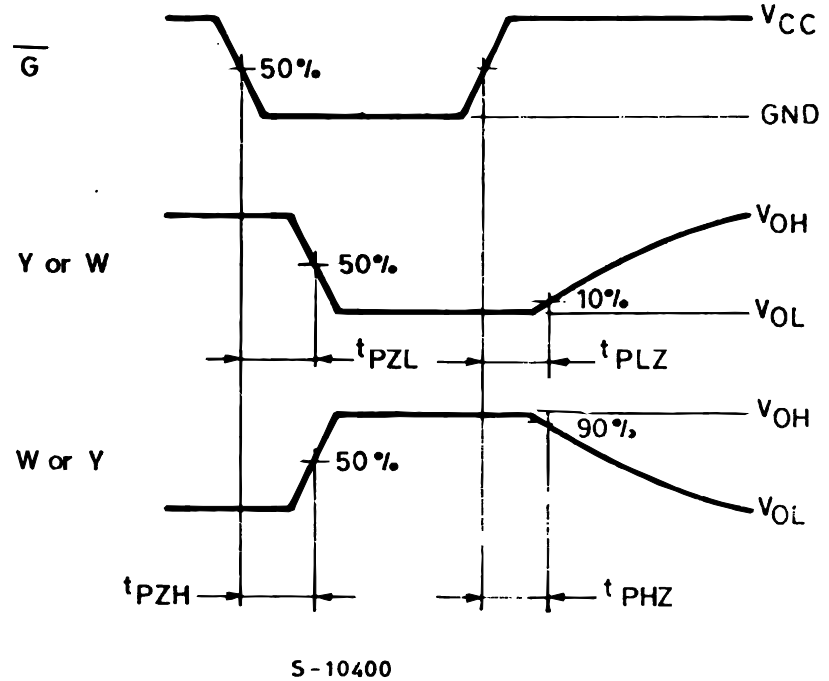
WAVEFORM 2: SETUP AND HOLD TIMES (f=1MHz; 50% duty cycle)



WAVEFORM 3 : PROPAGATION DELAY TIMES, MINIMUM PULSE WIDTH (f=1MHz; 50% duty cycle)

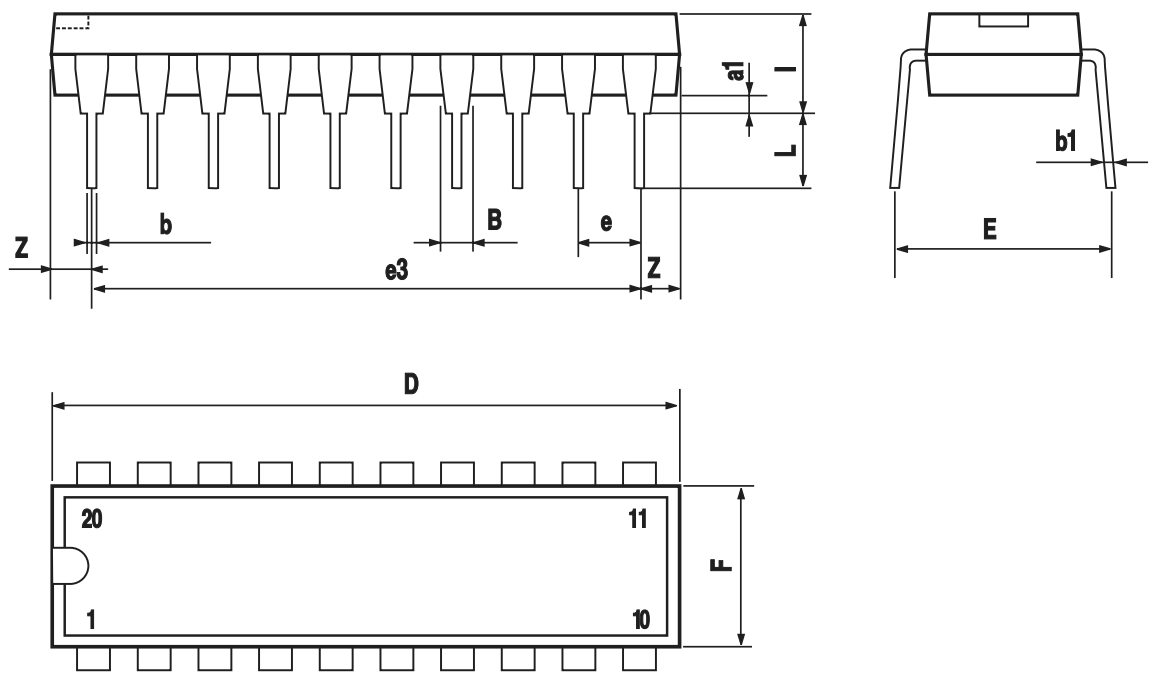


WAVEFORM 4 : OUTPUT ENABLE AND DISABLE TIME (f=1MHz; 50% duty cycle)



Plastic DIP-20 (0.25) MECHANICAL DATA

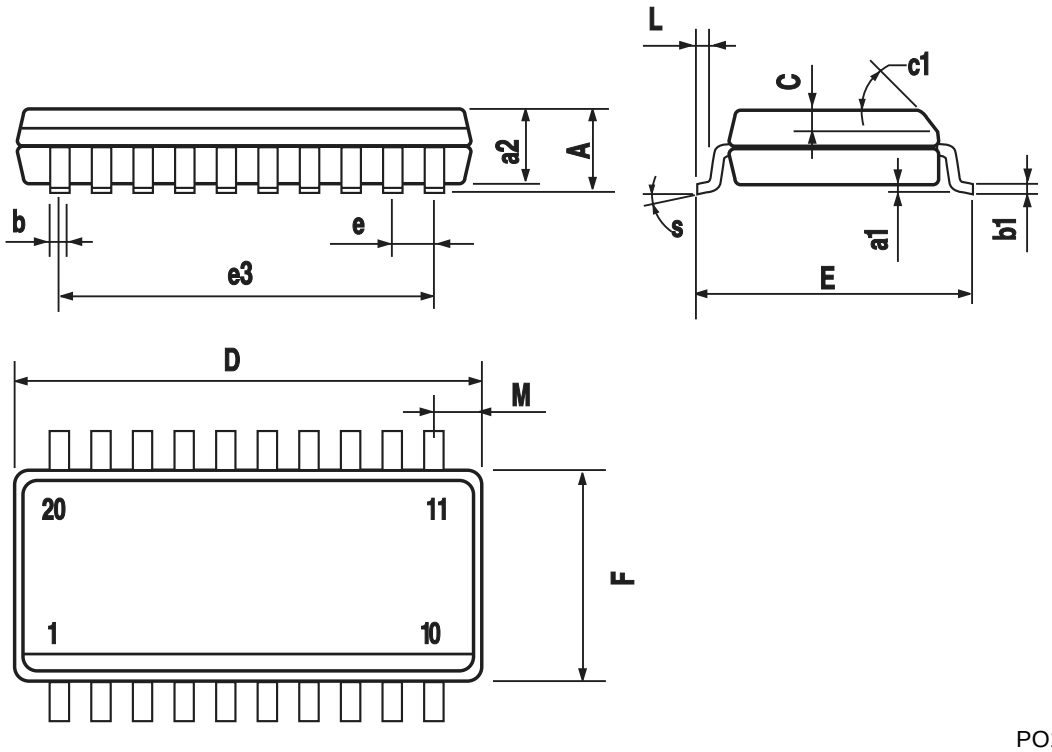
DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
a1	0.254			0.010		
B	1.39		1.65	0.055		0.065
b		0.45			0.018	
b1		0.25			0.010	
D			25.4			1.000
E		8.5			0.335	
e		2.54			0.100	
e3		22.86			0.900	
F			7.1			0.280
I			3.93			0.155
L		3.3			0.130	
Z			1.34			0.053



P001J

SO-20 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			2.65			0.104
a1	0.1		0.2	0.004		0.008
a2			2.45			0.096
b	0.35		0.49	0.014		0.019
b1	0.23		0.32	0.009		0.012
C		0.5			0.020	
c1	45° (typ.)					
D	12.60		13.00	0.496		0.512
E	10.00		10.65	0.393		0.419
e		1.27			0.050	
e3		11.43			0.450	
F	7.40		7.60	0.291		0.300
L	0.50		1.27	0.020		0.050
M			0.75			0.029
S	8° (max.)					



PO13L

TSSOP20 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			1.2			0.047
A1	0.05		0.15	0.002	0.004	0.006
A2	0.8	1	1.05	0.031	0.039	0.041
b	0.19		0.30	0.007		0.012
c	0.09		0.20	0.004		0.0089
D	6.4	6.5	6.6	0.252	0.256	0.260
E	6.2	6.4	6.6	0.244	0.252	0.260
E1	4.3	4.4	4.48	0.169	0.173	0.176
e		0.65 BSC			0.0256 BSC	
K	0°		8°	0°		8°
L	0.45	0.60	0.75	0.018	0.024	0.030