CML Semiconductor Products

PRODUCT INFORMATION

FX214 FX224

VSB* Audio Scrambler

Publication D/214/3 July 1994

Features/Applications

- *Variable Split-Band Frequency Inversion Voice Scrambler
- 32 Programmable Split Frequencies
- CTCSS HP Filter
- High Recovered Audio Quality
- Low-Power 5 Volt CMOS
- Half-Duplex Switching
- Powersave Facility
- Mobile or Cellular Radio Applications
- Fixed or Rolling Code Applications
- Serial/Parallel Load Options: FX214 (Serial), FX224 (Parallel),
- DIL and SMD Package Options

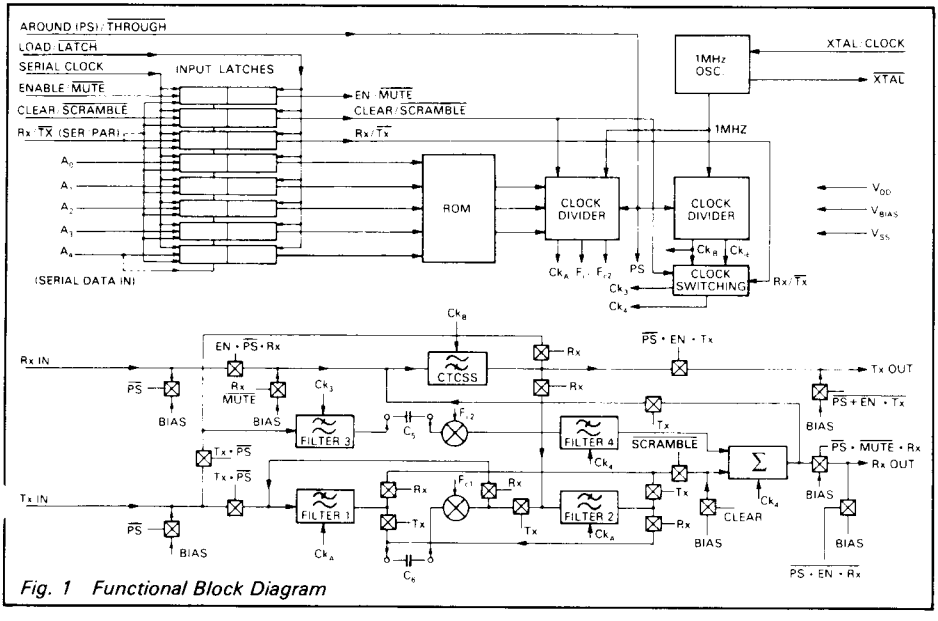


Fig. 1 Functional Block Diagram

FX214
FX224

Brief Description

The FX214 and 224 are low-power CMOS LSI devices designed as Variable Split-Band (VSB) voice scramblers.

The device uses separate Rx and Tx paths which are switched for half-duplex operation. To prevent interference from sub-audio products, an on-chip Continuous Tone Controlled Squelch System (CTCSS) highpass filter is automatically switched to the input in Rx and to the output in Tx.

Scrambling is achieved by splitting the input voice frequencies into upper and lower frequency bands using switched capacitor filters, modulating each band with selected carrier frequencies to "frequency invert" the bands and then summing the output.

A total of 32 different split-point and carrier frequency combinations are externally programmable using a 5-bit code; this code can be either fixed or varying (rolling), for greater security.

'Sync/Speech Mute', 'Powersave', 'Clear' and 'Audio-Bypass' facilities are controlled via external commands.

Timing and filter clocks are derived internally from an on-chip oscillator requiring only an external 1MHz Xtal or clock pulse input.

This device demonstrates high baseband and carrier frequency rejection with good 'recovered audio' quality. Serial or parallel command loading functions are available in both DIL and SMD Packages

Pin Functions

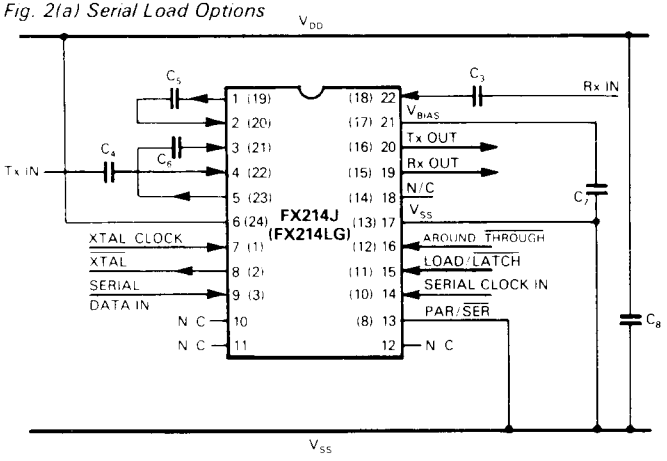
FX 214J	FX 214LG 214L2	FX 224J	FX 224LG 224LS	
7	1	1	1	**Xtal/Clock:** Input to the clock oscillator inverter. A 1MHz Xtal input or externally derived 1MHz clock is injected here. See Figure 2.
8	2	2	2	**$\overline{\text{Xtal}}$:** Output of the clock oscillator inverter.
9	3			**Serial Data Input:** This pin is used, on devices wired in the serial loading mode, to input an 8- bit word representing the digital control functions. This word is loaded using the serial data clock and is input in the following sequence: ENABLE; CLEAR; Rx/Tx; A_0; A_1; A_2; A_3; A_4, with the Load/Latch being operated on completion. See Timing Diagram Figure 7.
		3	3	A_4: **Programming Inputs:** In parallel mode, these are the 5 digital inputs
		4	4	A_3: whose code defines the split point frequency and the High and Low band
		5	5	A_2: carrier frquencies. Each of the 5 input pins have a 1MΩ internal pullup
		6	6	A_1: resistor. Table 2 contains programming information .
		7	7	A_0:
		8	8	**Rx/Tx:** This digital input selects the Receive or Transmit paths and configures Upperband and Lowerband filter bandwidths whilst setting the CTCSS High Pass Filter position in the signal path. See Table 1 and Figures 5 and 6. 1MΩ internal pullup resistor [Rx].
13	8			**Parallel/Serial:** This pin defines the loading mode of the digital function inputs. In the parallel load devices this pin has no external connections. For serial load devices this pin must be externally conected to V_{SS}. This pin on all devices has an 1MΩ internal pullup resistor.
		9	9	**Clear/Scramble:** This digital input puts the device 'Clear' or 'Frequency Inversion' mode by controlling the application of carrier frequency to the upper and lower band balanced modulators. In 'Scramble' the balanced modulator carrier frequency values are selected by the split point address A_0 - A_4 [Table 2]. In 'Clear' carriers are turned off and the balanced modulators are bypassed internally, the lower band is not added to the output signal. 1MΩ internal resistor [Clear].
		10	10	**Enable/$\overline{\text{Mute}}$:** This digital function is used to disable receive or transmit signal paths for rolling code synchronization whilst maintaining bias conditions. To allow synchronizing information to be transmitted, or receiver audio output to be removed during sync periods, a logic '1' will enable' a logic '0' will disable the selected [Rx/Tx] audio path. See Table 1. 1MΩ internal pullup resistor.
14	10			**Serial Clock Input:** The externally applied data clock frequency used to shift input data along on devices wired in the Serial loading mode. One full data clock cycle is required to shift one data bit completely into the register. See Timing Diagram Figure 7. This pin has a 1MΩ internal pullup resistor.
15	11	11	11	**Load/$\overline{\text{Latch}}$:** Controls the loading of the 8 digital function inputs: ENABLE; CLEAR; Rx/Tx; A_0-A_4 into the internal register. When this pin is '1' all 8 inputs are transparent and new data acts directly. For controlled changing of parameters in the parallel mode Load/Latch must be kept at logic '0' whilst a new function is loaded, then Load/Latch strobed 0-1-0 to latch the inputs in. For serial loading the data should be loaded with Load/Latch at logic '0' and then Load/Latch strobed 0-1-0 on completion of data loading. 1MΩ internal pullup resistor. See Figure 7. NOTE: Serial and/or parallel loading functions are dependant upon device type.

Pin Functions

FX 214J	FX 214LG 214L2	FX 224J	FX 224LG 224LS	
16	12	12	12	**Around [Powersave]/Through:** This digital input is used, when logic '1' to put the device into a powersave condition where all parts of the device except the 1MHz oscillator circuits are shut down, and signal input and output lines made open-circuit, free of all bias. This allows signal paths to be routed externally around the device. whilst reducing current consumption. A logic '0' enables the device to work normally as shown in Table 1. 1MΩ internal pullup resistor.
17	13	13	13	**V_{SS}:** Negative Supply [GND].
18	14	14	14	Internally connected , leave open circuit .
19	15	15	15	**Rx Output:** The processed audio signal output. This pin is held at dc 'bias' voltage for all functions except Powersave. This buffered output is driven by the Summer circuit in the Rx mode. Signal paths and bias levels are detailed in the Table 1 and Figure 6.
20	16	16	16	**Tx Output:** The processed audio output for the transmission channel. This pin is held at a dc 'bias' for all functions except Powersave. This summed and buffered signal is passed through the CTCSS High Pass Filter to the output pin in the Tx mode. Signal paths and bias levels are detailed in Table 1 and Figure 5.
21	17	17	17	**V_{BIAS}:** Normally at $V_{DD}/2$ this pin requires an external decoupling capacitor to V_{SS}.
22	18	18	18	**Rx Input:** The analogue received audio signal input. This pin is held at a dc 'bias' voltage by a 300kΩ on-chip bias resistor which is selected for all functions except Powersave, and therefore requires to be connected to external circuitry by a capacitor, C_3. See Figure 2. This input is routed through the CTCSS High Pass Filter in Rx mode to remove sub-audio frequencies from the voiceband. Signal paths and bias levels are detailed in Table 1 and Figure 6.
1	19	19	19	**Highband Filter Output:** The output of the Input Filter of the Upperband arm. The Rx/Tx function sets the lowpass filter at 3400Hz or 2700Hz respectively. This output must be connected to the Highband Balanced Modulator input via capacitor C_5. See Figure 2.
2	20	20	20	**Highband Balanced Modulator Input:** The input to the Balanced Modulator of the Upperband arm. This input must be connected to the Highband Filter Output via capacitor C_5.
3	21	21	21	**Lowband Balanced Modulator Input:** The input to the Balanced Modulator of the Lowerband arm. This input must be connected to the Lowerband Filter Output with capacitor C_6.
4	22	22	22	**Tx Input:** This is the analogue 'Clear' audio input for the VSB scrambler. This pin is held at a dc 'bias' voltage by a 300KΩ on-chip bias resistor which is selected for all functions except Powersave, and therefore requires to be connected to external circuitry by C_4. This input, in the Tx mode, is connected to Upper and Lowerband input filters, signal paths and bias levels are detailed in Table 1 and Figure 5.
5	23	23	23	**Lowband Filter Output:** The output of the Input Filter of the Lowerband arm, the Rx/Tx function determines which filter is used [Filter 1 or 2]. Figures 5 and 6. This output must be connected to the Lowerband Balanced Modulator Input via C_6.
6	24	24	24	**V_{DD}:** A single + 5V supply is required.

Component Connections

Fig. 2(a) Serial Load Options

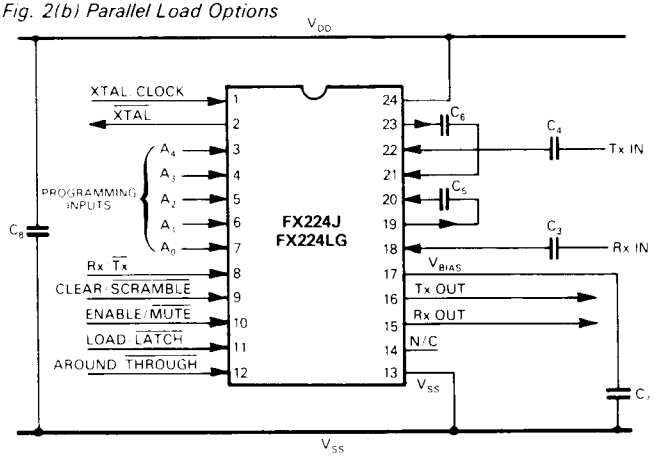


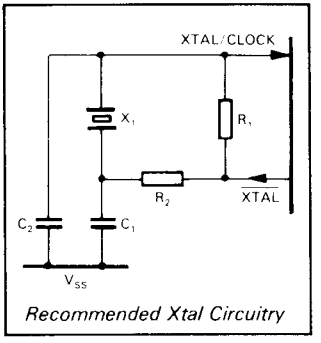
Not Connected

FX214J	10, 11, 12, 18*
FX214LG	4, 5, 6, 7, 9, 14*
FX224J	14*
FX224LG	14*

*Internally connected, do not connect to.

Fig. 2(b) Parallel Load Options





Recommended Xtal Circuitry

Xtal circuitry shown is in accordance with CML Application Note D/XT/1 April '86.

Component References	
Component	Unit Value
R_1	1M
R_2	Selectable
C_1	33p
C_2	68p
C_3	15n
C_4	15n
C_5	1.0µ
C_6	1.0µ
C_7	1.0µ
C_8	1.0µ
X_1	1MHz

Tolerance Resistors ± 10%
Capacitors ± 20%

C_5 and C_6 are coupling capacitors between filter outputs and balanced modulator inputs.

Fig. 2 External Component Connections

Application Information

This device can be used in 'Scramble' (frequency inversion) or 'Clear' speech modes. The inversion frequencies, when selected are controlled by the ROM address code (table 2). Keeping the code in one state (fixed) is the simplest form of operation. A more secure method is to continually change the ROM address code (rolling code) therefore changing split-point and carrier frequencies. This method requires some external form of code change generation with synchronization between transmit and receive stations. Many variations of code sequence are possible.

The recommended external component connections are shown in figure 2. In the Scramble mode, Split-point and Low and High band carrier frequencies (F_c1, F_c2) are selected and set in accordance with the ROM address code present at the inputs A_0 to A_4, *See Table 2.*

During the Clear speech function both Lower and Upperband filter arms are selected (figures 5 or 6), the carrier frequencies are turned off and the balanced modulators are bypassed internally. The Low band audio is removed from the output signal prior to summation.

Enable/$\overline{\text{Mute}}$
To enable code synchronization to be transmitted the speech output can be interrupted with the Enable/$\overline{\text{Mute}}$ function. A logic '0' will isolate the whole device whilst leaving the audio input and output pins at bias level. *See Table 1.*

Powersave
When the Around/$\overline{\text{Through}}$ function is at a logic '1' the device is in the powersave condition. Audio signals may be hardwired around the device normally as the input and output pins are open circuit. *See Table 1.*

Effect of Chosen Function on Inputs and Outputs		CHOSEN FUNCTION			
		Rx = '1'	**$\overline{\text{Tx}}$ = '0'**	**$\overline{\text{Mute}}$ = '0'**	**Around** (Powersave) = **'1'**
Rx Input	Path	Enabled	Disconnect	Disconnect	High Impedance
	Level	Bias	Bias	Bias	
Rx Output	Path	Enabled	Disconnected	Disconnect	High Impedance
	Level	Bias	Bias	Bias	
Tx Input	Path	Disconnected	Enabled	Enabled	High Impedance
	Level	Bias	Bias	Bias	
Tx Output	Path	Disconnected	Enabled	Disconnected	High Impedance
	Level	Bias	Bias	Bias	

Table 1 Functions Influencing Signal Paths

ROM Address A_4-A_0	Split Point Hz	Low Band Carrier, Hz f_{c1}	High Band Carrier, Hz f_{c2}
0 0 0 0 0	2800	3105	6172
0 0 0 0 1	2625	2923	6024
0 0 0 1 0	2470	2777	5813
0 0 0 1 1	2333	2631	5681
0 0 1 0 0	2210	2512	5555
0 0 1 0 1	2100	2403	5494
0 0 1 1 0	2000	2304	5376
0 0 1 1 1	1909	2212	5263
0 1 0 0 0	1826	2127	5208
0 1 0 0 1	1750	2049	5102
0 1 0 1 0	1680	1984	5050
0 1 0 1 1	1555	1858	4950
0 1 1 0 0	1448	1748	4807
0 1 1 0 1	1354	1655	4716
0 1 1 1 0	1272	1572	4629
0 1 1 1 1	1200	1501	4587

ROM Address A_4-A_0	Split Point Hz	Low Band Carrier, Hz f_{c1}	High Band Carrier, Hz f_{c2}
1 0 0 0 0	1135	1436	4504
1 0 0 0 1	1050	1351	4424
1 0 0 1 0	976	1278	4347
1 0 0 1 1	913	1213	4310
1 0 1 0 0	857	1157	4273
1 0 1 0 1	792	1094	4166
1 0 1 1 0	736	1037	4132
1 0 1 1 1	688	988	4065
1 1 0 0 0	636	936	4032
1 1 0 0 1	591	891	3968
1 1 0 1 0	552	853	3937
1 1 0 1 1	512	813	3906
1 1 1 0 0	471	772	3846
1 1 1 0 1	428	728	3816
1 1 1 1 0	388	688	3787
1 1 1 1 1	350	650	3731

Table 2 ROM Address Programming Table

Application Information

For the following descriptions, the term 'FX214' can be taken to mean FX214 or FX224.

Audio Quality

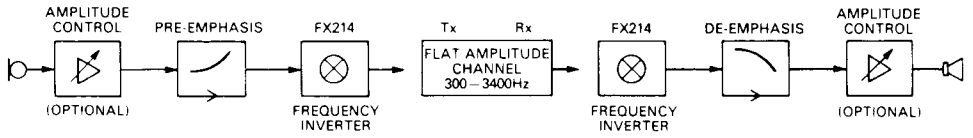


Fig. 3 Recommended Basic Communication Audio System Layout

Figure 3 shows the recommended basic audio system layout using added pre- and de-emphasis circuitry to maintain good recovered speech quality. In the Transmit mode *Do Not* pre-emphasise the audio output of the FX214. In the Receive mode de-emphasis should be used after the FX214.

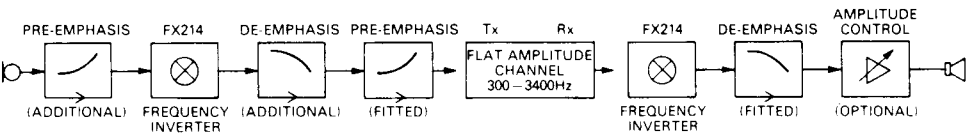


Fig. 4 Recommended Basic Radio Communication Audio System Layout

Figure 4 shows the recommended basic audio system layout if it is necessary to install the FX214 within a radio having pre- and de-emphasis circuitry as a standard. This is where post-emphasis access is not possible in the transmitter.

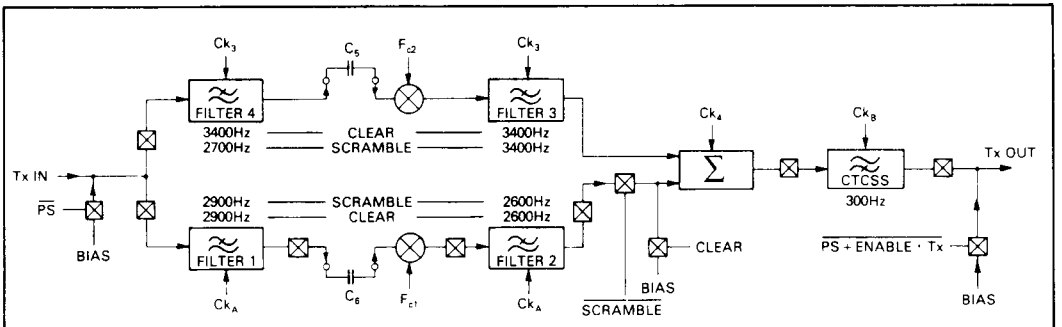


Fig. 5 Basic Tx Path

During the Transmit function the Low Pass and CTCSS filters are configured automatically as shown in Figure 5, with cut-off frequencies (-3dB) indicated.

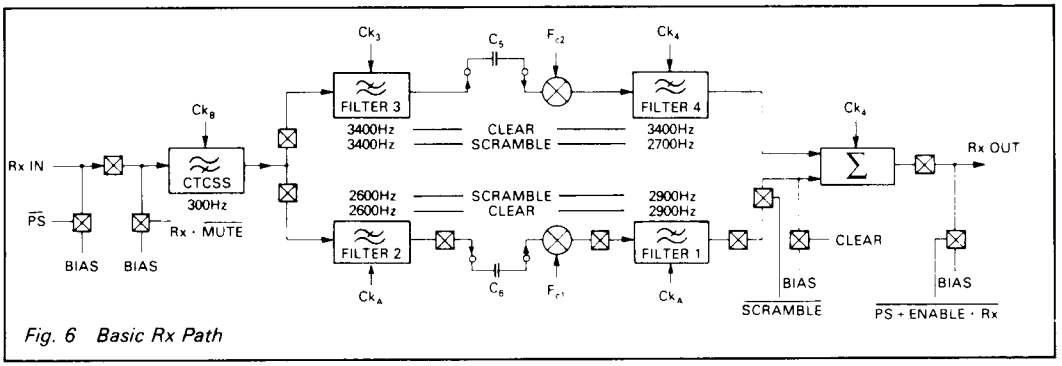


Fig. 6 Basic Rx Path

During the Receive function the Low Pass and CTCSS filters are configured automatically as shown in Figure 6, with cut-off frequencies (-3dB) indicated.

Electrical Specifications

Absolute Maximum Ratings

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not implied.

Supply voltage		−0.3V to 7.0V
Input voltage at any pin (ref V_{SS} = OV)		−0.3V to (V_{DD} + 0.3V)
Sink/source current (supply pins)		± 30mA
	(other pins)	± 20mA
Total device dissipation @ 25°C		800mW Max.
Derating		10mW/°C
Operating temperature range:	FX214J/224J	−30°C to +85°C (Ceramic)
	FX214LG/224LG	−30°C to +70°C (Plastic)
Storage temperature range:	FX214J/224J	−55°C to +125°C (Ceramic)
	FX214LG/224LG	−40°C to +85°C (Plastic)

Operating Limits

All characteristics measured using the following parameters unless otherwise specified:
V_{DD} = 5.0V, T_{amb} = 25°C, F_{clk} = 1.0MHz, Audio Level Ref: 0dB = 775mVrms.

Characteristics	See Note	Min.	Typ.	Max.	Unit
Static Values					
Supply voltage		4.5	5	5.5	V
Supply current (Enabled)		—	8	—	mA
Supply current (Powersave)		—	1.2	—	mA
Analogue Input Impedances					
Tx/Rx Input (Enabled)		—	100	—	kΩ
Tx/Rx Input (Powersave)		1	—	—	MΩ
Balanced Modulator		—	40	—	kΩ
Analogue Output Impedances					
Rx Output (Tx Mode)		—	100	—	kΩ
Rx Output (Rx Mode)		—	—	2	kΩ
Rx Output (Powersave)		1	—	—	MΩ
Tx Output (Tx Mode)		—	—	2	kΩ
Tx Output (Rx Mode)		—	100	—	kΩ
Tx Output (Powersave)		1	—	—	MΩ
Input LPF		—	—	1	kΩ
Digital Values					
Digital Input Impedance		100	—	—	kΩ
Dynamic Values					
Input Logic '1'		3.5	—	—	V
Input Logic '0'		—	—	1.5	V
Xtal/Clock Frequency		—	1	—	MHz
Analogue Input Level		−18	—	+6	dB
Carrier Breakthrough	1	—	−55	—	dB
Baseband Breakthrough	1, 2 or 3	—	−33	—	dB
Filter Clock Breakthrough	1, 2 or 3	—	−50	—	dB
Output Noise	1, 4	—	−45	—	dB
Passband Characteristics					
Clear Mode	7				
Passband Gain		—	0	—	dB
Output Lower 3dB Point (Rx or Tx)		—	300	—	Hz
Output Upper 3dB Point (Rx or Tx)		—	3400	—	Hz
Scramble-Descramble	5				
Received Signal Passband Gain	6	—	0	—	dB
Received Signal Lower 3dB Point		—	400	—	Hz
Received Signal Upper 3dB Point		—	2700	—	Hz
Transmitted Signal Lower 3dB Point		—	300	—	Hz
Transmitted Signal Upper 3dB Point		—	3400	—	Hz
CTCSS (Highpass Filter)					
−3dB Point		—	300	—	Hz
Passband Gain		—	0	—	dB
Stopband Attenuation at f>250 Hz		—	40	—	dB

Electrical Specifications...

Characteristics	See Note	Min.	Typ.	Max.	Unit
Timing *(Figure 7)*					
Serial Mode Enable Set Up (t_{SMS})		250	—	—	ns
Serial Clock 'High' Pulse Width (t_{PWH})		250	—	—	ns
Serial Clock 'Low' Pulse Width (t_{PWL})		250	—	—	ns
Data Set Up Time (t_{DS})		150	—	—	ns
Data Hold Time (t_{DHS})		50	—	—	ns
Load/$\overline{\text{Latch}}$ Set Up Time (t_{LL})		250	—	—	ns
Load/$\overline{\text{Latch}}$ Pulse Width (t_{LLW})		150	—	—	ns
Data Set Up Time (t_{DSP})		150	—	—	ns
Data Hold Time (t_{DHP})		20	—	—	ns

Notes:
1. *Measured at the output of a single device.*
2. *Tx Mode.*
3. *Rx Mode.*
4. *With input A.C. short-circuited to V_{SS}.*
5. *Measured at the output of a receiving device in a scrambler-descrambler system with a transmission channel having a flat amplitude response and a bandwidth of 300Hz to 3400Hz and measured relative to the input signal at the transmitting device.*
6. *Excluding split point ± 150Hz.*
7. *Measured at the Rx or Tx output pin of a single device.*

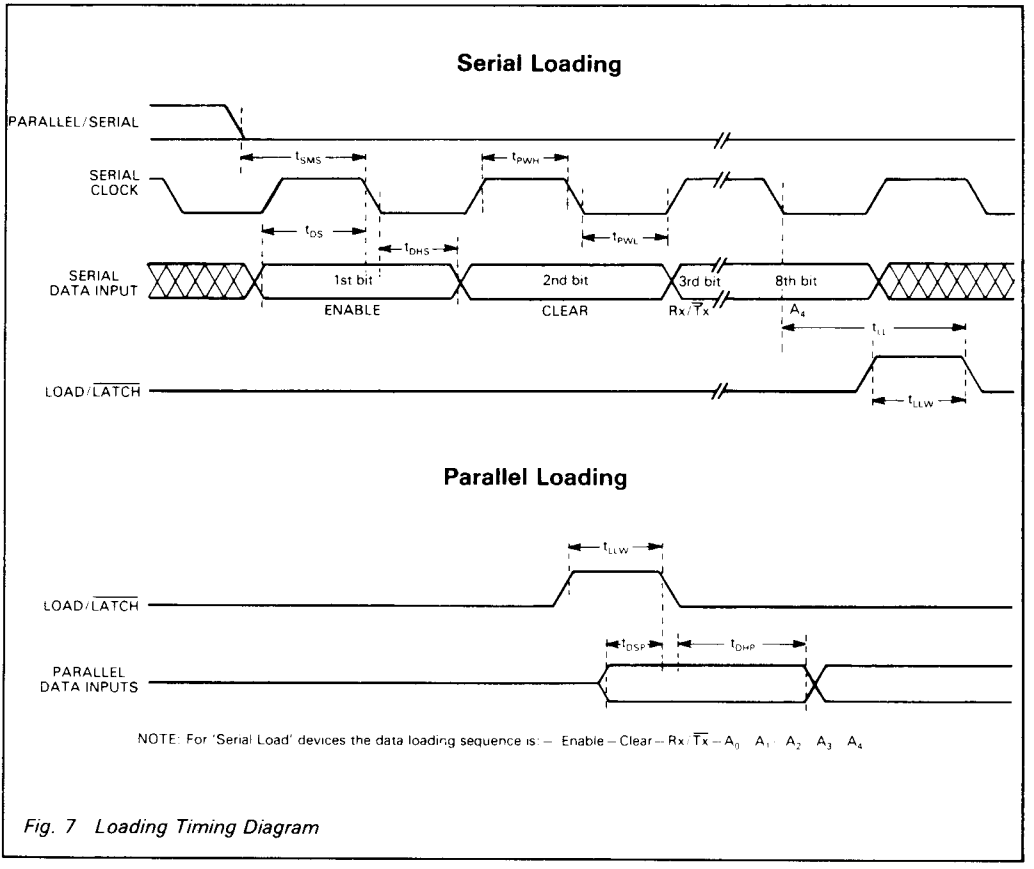


Fig. 7 Loading Timing Diagram

Package Outlines

The FX214 and FX224 are available in the package styles outlined below. Mechanical package diagrams and specifications are detailed in Section 10 of this document.
Pin 1 identification marking is shown on the relevant diagram and pins on all package styles number anti-clockwise when viewed from the top.

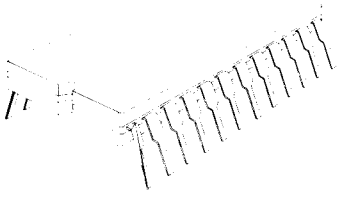
FX214J 22-pin cerdip DIL (J3)

NOT TO SCALE

Max. Body Length 27.38mm
Max. Body Width 9.75mm

FX224J 24-pin cerdip DIL (J4)

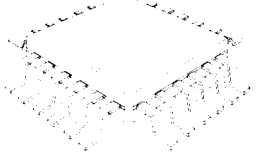
NOT TO SCALE



Max. Body Length 32.03mm
Max. Body Width 14.81mm

FX214LG/224LG 24-pin quad plastic encapsulated bent and cropped (L1)

NOT TO SCALE



Max. Body Length 10.25mm
Max. Body Width 10.25mm

Handling Precautions

The FX214 and FX224 are CMOS LSI circuits which include input protection. However precautions should be taken to prevent static discharges which may cause damage.

Package Outlines .....

FX214L2/224LS 24-lead plastic leaded chip carrier

NOT TO SCALE

Max. Body Length 10.40mm
Max. Body Width 10.40mm

Ordering Information

FX214J	22-pin cerdip DIL	(J3)
FX214LG	24-pin quad plastic encapsulated bent and croppped	(L1)
FX214L2	24-lead plastic leaded chip carrier	
FX224J	24-pin cerdip DIL	(J4)
FX224LG	24-pin quad plastic encapsulated bent and croppped	(L1)
FX224LS	24-lead plastic leaded chip carrier	(L2)