

# PRELIMINARY

Notice : This is not a final specification.  
Some parametric limits are subject to change.

## MITSUBISHI LSIs M6MFB/T16S2TP

16777216-BIT (2M x 8-BIT / 1M x 16-BIT) CMOS 3.3V-ONLY  
FLASH MEMORY &  
2097152-BIT (256k x 8-BIT) CMOS STATIC RAM  
MCP (Multi Chip Package)

### DESCRIPTION

The MITSUBISHI M6MFB/T16S2TP is a Multi Chip Package (MCP) that contents 16-Mbit Flash memory and 2M-bit Static RAM in a 82-pin TSOP(TYPE-II).

16M-bit Flash memory is a 2097152 bytes/1048572 words, 3.3V-only, and high performance non-volatile memory fabricated by CMOS technology for the peripheral circuit and DINOR(Divided bit-line NOR) architecture for the memory cell.

2M-bit SRAM is a 262144 bytes unsynchronous SRAM fabricated by silicon-gate CMOS technology.

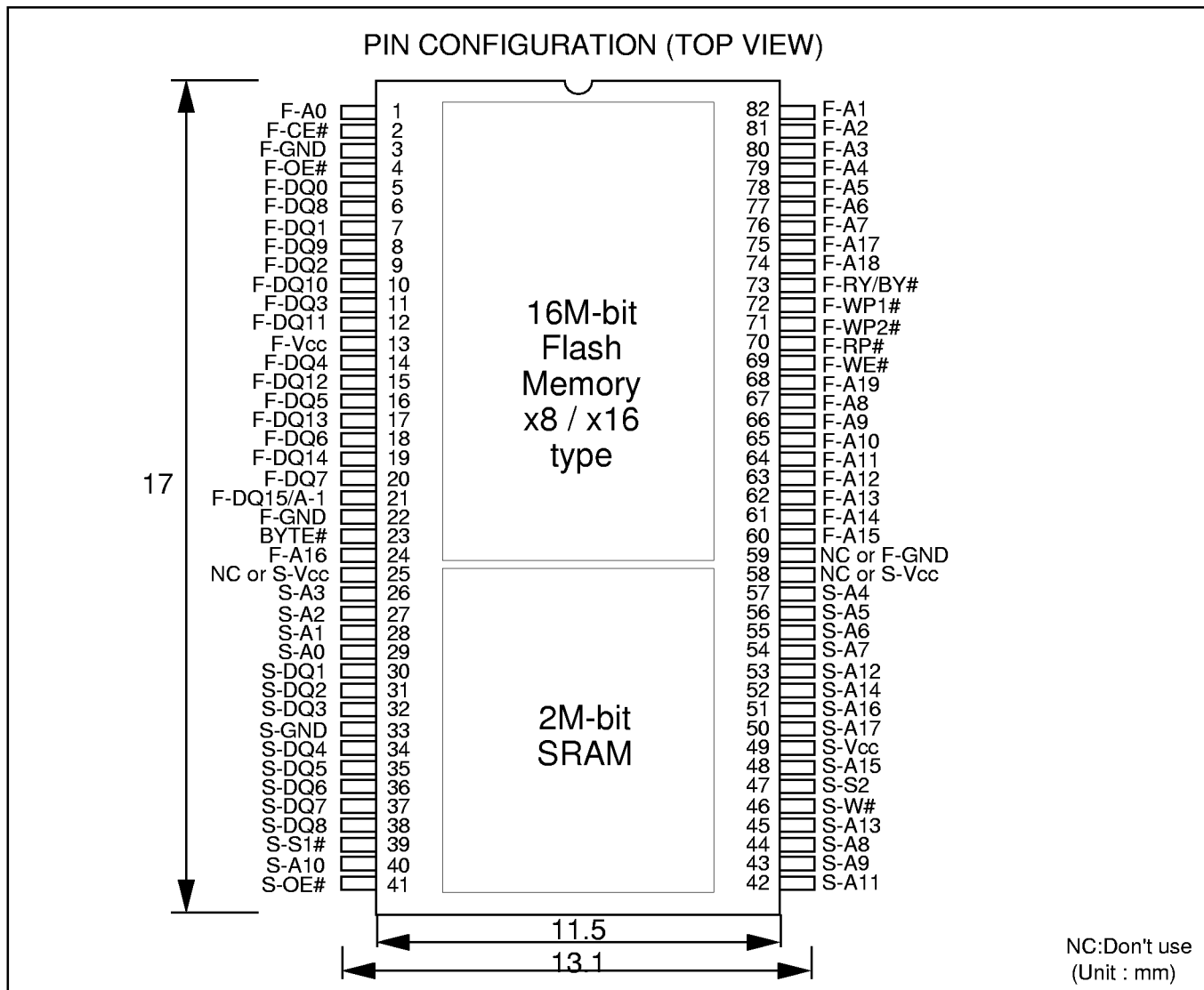
M6MFB/T16S2TP is suitable for the application of the mobile-communication-system to reduce both the mount space and weight .

### FEATURES

- Flash memory, SRAM Access time ----- 110ns (Max.)
- Supply voltage ----- Vcc=2.7 ~ 3.6V
- Ambient temperature ----- Ta=-20 ~ 85°C
- Flash Memory / SRAM : Operates individually
- Package : 82-pin TSOP (Type-II) , 0.4mm lead pitch

### APPLICATION

Mobile communication products



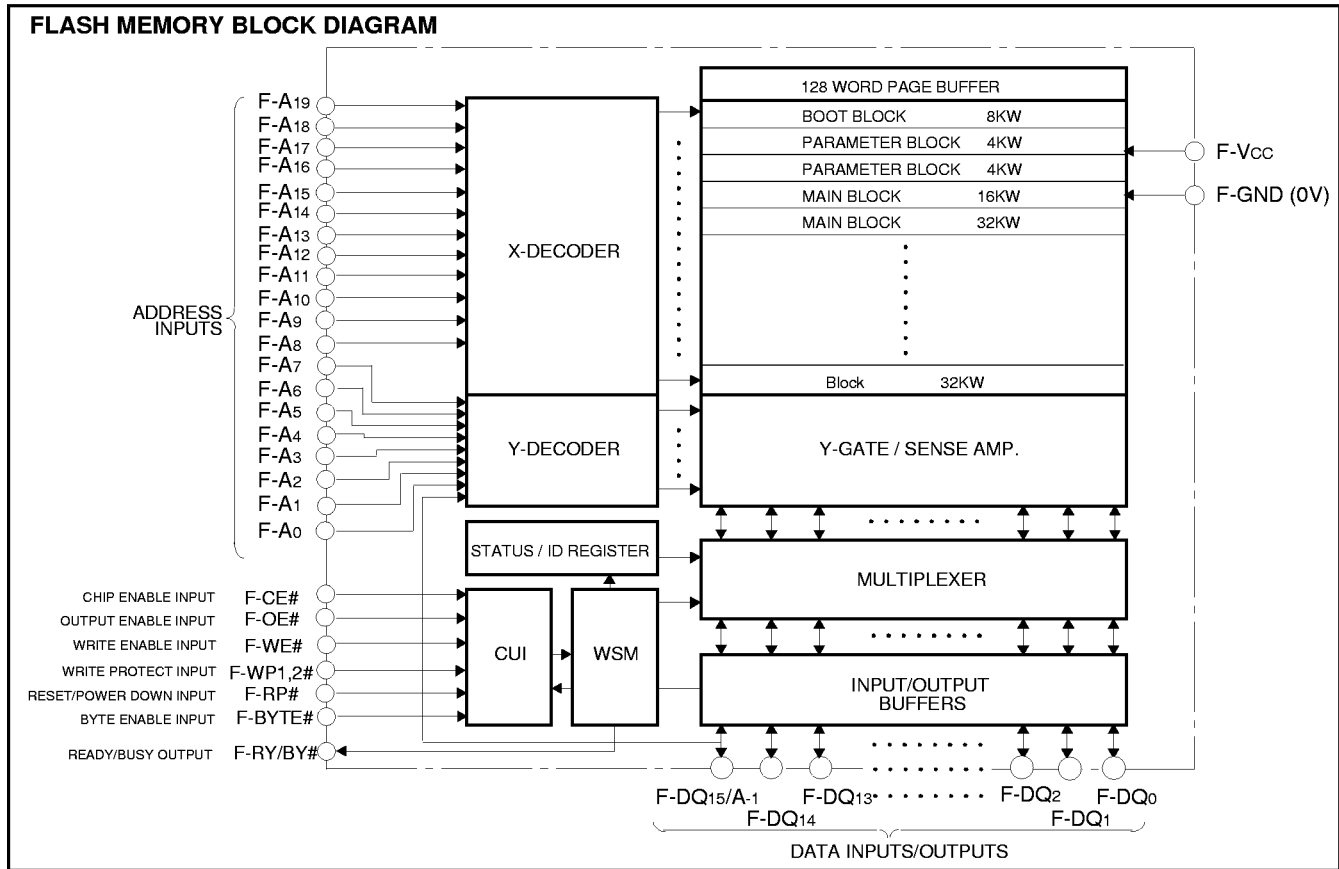
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# M6MFB/T16S2TP

16777216-BIT (2M x 8-BIT/1M x 16-BIT)  
CMOS 3.3V-ONLY FLASH MEMORY



### FUNCTION

The flash memory of M6MFT/B16S2TP includes on-chip program/erase control circuitry. The Write State Machine (WSM) controls block erase and page program operations. Operational modes are selected by the commands written to the Command User Interface (CUI). The Status Register indicates the status of the WSM and when the WSM successfully completes the desired program or block erase operation.

A Deep Powerdown mode is enabled when the F-RP# pin is at GND, minimizing power consumption.

### Read

The flash memory of M6MFT/B16S2TP has three read modes, which accesses to the memory array, the Device Identifier and the Status Register. The appropriate read command are required to be written to the CUI. Upon initial device powerup or after exit from deep powerdown, the flash memory automatically resets to read array mode. In the read array mode, low level input to F-CE# and F-OE#, high level input to F-WE# and F-RP#, and address signals to the address inputs (F-A0-19) output the data of the addressed location to the data input/output(F-DQ0-15).

### Write

Writes to the CUI enables reading of memory array data, device identifiers and reading and clearing of the Status Register. They also enable block erase and program. The CUI is written by bringing F-WE# to low level, while F-CE# is at low level and F-OE# is at high level. Address and data are latched on the earlier rising edge of F-WE# and F-CE#. Standard micro-processor write timings are used.

### Output Disable

When F-OE# is at  $V_{IH}$ , output from the devices is disabled. Data input/output are in a high-impedance(High-Z) state.

### Standby

When F-CE# is at  $V_{IH}$ , the device is in the standby mode and its power consumption is reduced. Data input/output are in a high-impedance(High-Z) state. If the memory is deselected during block erase or program, the internal control circuits remain active and the device consume normal active power until the operation completes.

### Automatic Power Saving

When addresses remain stable for about 300ns(T.B.D), the device enters the automatic power saving mode. While in power saving mode, output data is latched and always available to the system.

### Deep Power-Down

When F-RP# is at  $V_{IL}$ , the device is in the deep powerdown mode and its power consumption is substantially low. During read modes, the memory is deselected and the data input/output are in a high-impedance(High-Z) state. After return from powerdown, the CUI is reset to Read Array, and the Status Register is cleared to value 80H.

During block erase or program modes, F-RP# low will abort either operation. Memory array data of the block being altered become invalid.

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16777216-BIT (2M x 8-BIT/1M x 16-BIT)  
CMOS 3.3V-ONLY FLASH MEMORY

## SOFTWARE COMMAND DEFINITIONS

The device operations are selected by writing specific software command into the Command User Interface.

### Read Array Command (FFH)

The device is in Read Array mode on initial device powerup and after exit from deep powerdown, or by writing FFH to the Command User Interface. The device remains in Read Array mode until the other commands are written.

### Read Device Identifier Command (90H)

The Device Identifier is read after writing the Read Device Identifier command of 90H to the Command User Interface. Following the command write, the manufacturer code and the device code can be read from address 000000H and 000001H, respectively. Additionally, The Device Identifier is read by rising F-A# to high voltage for PROM programmers.

### Read Status Register Command (70H)

The Status Register is read after writing the Read Status Register command of 70H to the Command User Interface.

The contents of Status Register are latched on the later falling edge of F-OE# or F-CE#. So F-CE# or F-OE# must be toggled every status read.

### Clear Status Register Command (50H)

The Erase Status and Program Status bits are set to "1"s by the Write State Machine and can only be reset by the Clear Status Register command of 50H. These bits indicates various failure conditions.

### Block Erase / Confirm Command (20H/D0H)

Automated block erase is initiated by writing the Block Erase command of 20H followed by the Confirm command of D0H. An address within the block to be erased is required. The WSM executes iterative erase pulse application and erase verify operation.

### Page Program Commands(41H)

Page Program allows fast programming of 128words of data in word-wide mode. Writing of 41H initiates the page program operation. From 2nd cycle to 129th cycle write data must be serially inputted. Address A6-0 have to be incremented from 00H to 7FH. After completion of data loading, the WSM controls the program pulse application and verify operation.

Basically re-program must not be done on a page which has already programmed.

### Suspend/Resume Command (B0H/D0H)

Writing the Suspend command of B0H during block erase operation interrupts the block erase operation and allows read out from another block of memory. Writing the Suspend command of B0H during program operation interrupts the program operation and allows read out from another block of memory. The device continues to output Status Register data when read, after the Suspend command is written to it. Polling the WSM Status and Suspend Status bits will determine when the erase operation or program operation has been suspended. At this point, writing of

the Read Array command to the CUI enables reading data from blocks other than that which is suspended. When the Resume command of D0H is written to the CUI, the WSM will continue with the erase or program processes.

## DATA PROTECTION

The flash memory of M6MFB/T16S2TP provides hardware-locking of boot block, when F-WP1# is fixed to GND, boot block and all main blocks, when F-WP2# is fixed to GND, all blocks, when F-WP1# and F-WP2# are fixed to GND, and selectable block locking of parameter/main blocks by the lock-bit state. Hardware-locking is prevented from any modifications

## Power Supply Voltage

When the power supply voltage (Vcc) is less than 2.2V, the device is set to the Read-only mode.

A delay time of 2 us is required before any device operation is initiated. The delay time is measured from the time Vcc reaches Vccmin.

During power up, F-RP#=GND is recommended. Falling in Busy status is not recommended for possibility of damaging the device.



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## MITSUBISHI LSIs

# M6MFB/T16S2TP

### 16777216-BIT (2M x 8-BIT/1M x 16-BIT) CMOS 3.3V-ONLY FLASH MEMORY

x8 ( Bytemode)	x16 ( Wordmode)	
1F0000H-1FFFFFH	F8000H-FFFFFH	32Kword BLOCK
1E0000H-1EFFFFH	F0000H-F7FFFH	32Kword BLOCK
1D0000H-1DFFFFH	E8000H-EFFFFH	32Kword BLOCK
1C0000H-1CFFFFH	E0000H-E7FFFH	32Kword BLOCK
1B0000H-1BFFFFH	D8000H-DFFFFH	32Kword BLOCK
1A0000H-1AFFFFH	D0000H-D7FFFH	32Kword BLOCK
190000H-19FFFFH	C8000H-CFFFFH	32Kword BLOCK
180000H-18FFFFH	C0000H-C7FFFH	32Kword BLOCK
⋮	⋮	⋮
040000H-04FFFFH	20000H-27FFFH	32Kword BLOCK
030000H-03FFFFH	18000H-1FFFFH	32Kword BLOCK
020000H-02FFFFH	10000H-17FFFH	32Kword BLOCK
010000H-01FFFFH	08000H-0FFFFH	32Kword BLOCK
008000H-00FFFFH	04000H-07FFFH	16Kword BLOCK
006000H-007FFFH	03000H-03FFFH	4Kword PARAMETER BLOCK
004000H-005FFFH	02000H-02FFFH	4Kword PARAMETER BLOCK
000000H-003FFFH	00000H-01FFFH	8Kword BOOT BLOCK

F-A<sub>1</sub>~F-A<sub>19</sub>(Bytemode) F-A<sub>0</sub>~F-A<sub>19</sub>(Wordmode)

**M6MFB16S2TP Flash Memory Map**

x8 ( Bytemode)	x16 ( Wordmode)	
1FC000H-1FFFFFFH	FE000H-FFFFFFH	8Kword BOOT BLOCK
1FA000H-1FBFFFH	FD000H-FDFFFH	4Kword PARAMETER BLOCK
1F8000H-1F9FFFH	FC000H-FCFFFH	4Kword PARAMETER BLOCK
1F0000H-1F7FFFH	F8000H-FBFFFH	16Kword BLOCK
1E0000H-1EFFFFH	F0000H-F7FFFH	32Kword BLOCK
1D0000H-1DFFFFH	E8000H-EFFFFH	32Kword BLOCK
1C0000H-1CFFFFH	E0000H-E7FFFH	32Kword BLOCK
1B0000H-1BFFFFH	D8000H-DFFFFH	32Kword BLOCK
1A0000H-1AFFFFH	D0000H-D7FFFH	32Kword BLOCK
⋮	⋮	⋮
060000H-06FFFFH	30000H-37FFFH	32Kword BLOCK
050000H-05FFFFH	28000H-2FFFFH	32Kword BLOCK
040000H-04FFFFH	20000H-27FFFH	32Kword BLOCK
030000H-03FFFFH	18000H-1FFFFH	32Kword BLOCK
020000H-02FFFFH	10000H-17FFFH	32Kword BLOCK
010000H-01FFFFH	08000H-0FFFFH	32Kword BLOCK
000000H-00FFFFH	00000H-07FFFH	32Kword BLOCK

F-A<sub>1</sub>~F-A<sub>19</sub>(Bytemode) F-A<sub>0</sub>~F-A<sub>19</sub>(Wordmode)

**M6MFT16S2TP Flash Memory Map**

## BUS OPERATIONS

### Bus Operations for Word-Wide Mode (F-BYTE#=VIH)

Mode	Pins	F-CE#	F-OE#	F-WE#	F-RP#	F-DQ <sub>0-15</sub>	F-RY/BY#
Read	Array	V <sub>IL</sub>	V <sub>IL</sub>	V <sub>IH</sub>	V <sub>IH</sub>	Data out	V <sub>OH</sub> (HI-Z)
	Status Register	V <sub>IL</sub>	V <sub>IL</sub>	V <sub>IH</sub>	V <sub>IH</sub>	Status Register Data	X <sup>1)</sup>
	Lock Bit Status	V <sub>IL</sub>	V <sub>IL</sub>	V <sub>IH</sub>	V <sub>IH</sub>	Lock Bit Data (DQ <sub>6</sub> )	X
	Identifier Code	V <sub>IL</sub>	V <sub>IL</sub>	V <sub>IH</sub>	V <sub>IH</sub>	Identifier Code	V <sub>OH</sub> (HI-Z)
Output disable		V <sub>IL</sub>	V <sub>IH</sub>	V <sub>IH</sub>	V <sub>IH</sub>	Hi-Z	X
Stand by		V <sub>IH</sub>	X <sup>2)</sup>	X	V <sub>IH</sub>	Hi-Z	X
Write	Program	V <sub>IL</sub>	V <sub>IH</sub>	V <sub>IL</sub>	V <sub>IH</sub>	Command/Data in	X
	Erase	V <sub>IL</sub>	V <sub>IH</sub>	V <sub>IL</sub>	V <sub>IH</sub>	Command	X
	Others	V <sub>IL</sub>	V <sub>IH</sub>	V <sub>IL</sub>	V <sub>IH</sub>	Command	X
Deep Power Down		X	X	X	V <sub>IL</sub>	Hi-Z	V <sub>OH</sub> (HI-Z)

### Bus Operations for Byte-Wide Mode (F-BYTE#=VIL)

Mode	Pins	F-CE#	F-OE#	F-WE#	F-RP#	F-DQ <sub>0-7</sub>	F-RY/BY#
Read	Array	V <sub>IL</sub>	V <sub>IL</sub>	V <sub>IH</sub>	V <sub>IH</sub>	Data out	V <sub>OH</sub> (HI-Z)
	Status Register	V <sub>IL</sub>	V <sub>IL</sub>	V <sub>IH</sub>	V <sub>IH</sub>	Status Register Data	X <sup>1)</sup>
	Lock Bit Status	V <sub>IL</sub>	V <sub>IL</sub>	V <sub>IH</sub>	V <sub>IH</sub>	Lock Bit Data (DQ <sub>6</sub> )	X
	Identifier Code	V <sub>IL</sub>	V <sub>IL</sub>	V <sub>IH</sub>	V <sub>IH</sub>	Identifier Code	V <sub>OH</sub> (HI-Z)
Output disable		V <sub>IL</sub>	V <sub>IH</sub>	V <sub>IH</sub>	V <sub>IH</sub>	Hi-Z	X
Stand by		V <sub>IH</sub>	X <sup>2)</sup>	X	V <sub>IH</sub>	Hi-Z	X
Write	Program	V <sub>IL</sub>	V <sub>IH</sub>	V <sub>IL</sub>	V <sub>IH</sub>	Command/Data in	X
	Erase	V <sub>IL</sub>	V <sub>IH</sub>	V <sub>IL</sub>	V <sub>IH</sub>	Command	X
	Others	V <sub>IL</sub>	V <sub>IH</sub>	V <sub>IL</sub>	V <sub>IH</sub>	Command	X
Deep Power Down		X	X	X	V <sub>IL</sub>	Hi-Z	V <sub>OH</sub> (HI-Z)

1) X at F-RY/BY# is V<sub>OL</sub> or V<sub>OH</sub>(HI-Z).

\*The F-RY/BY# is an open drain output pin and indicates status of the internal WSM. When low, it indicates that the WSM is Busy performing an operation. A pull-up resistor of 10K-100K Ohms is required to allow the F-RY/BY# signal to transition high indicating a Ready WSM condition.

2) X can be V<sub>IH</sub> or V<sub>IL</sub> for control pins.

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16777216-BIT (2M x 8-BIT/1M x 16-BIT)  
CMOS 3.3V-ONLY FLASH MEMORY

## SOFTWARE COMMAND DEFINITION Command List

Command	1st bus cycle			2nd bus cycle			3rd bus cycle		
	Mode	Address	Data (F-DQ7-0)	Mode	Address	Data (F-DQ7-0)	Mode	Address	Data (F-DQ7-0)
Read Array	Write	X	FFH						
Device Identifier	Write	X	90H	Read	IA <sup>2)</sup>	ID <sup>2)</sup>			
Read Status Register	Write	X	70H	Read	X	SRD <sup>3)</sup>			
Clear Status Register	Write	X	50H						
Page Program <sup>4)</sup>	Write	X	41H	Write	WA0 <sup>4)</sup>	WD0 <sup>4)</sup>	Write	WA1	WD1
Block Erase / Confirm	Write	X	20H	Write	BA <sup>5)</sup>	D0H			
Suspend	Write	X	B0H						
Resume	Write	X	D0H						
Read Lock Bit Status	Write	X	71H	Read	BA	DQ6 <sup>6)</sup>			
Lock Bit Program / Confirm <sup>7)</sup>	Write	X	77H	Write	BA	D0H			
Erase All Unlocked Blocks	Write	X	A7H	Write	X	D0H			
Sleep <sup>8)</sup>	Write	X	F0H						

1) In the word-wide mode, upper byte data (F-DQ8~F-DQ15) is ignored.

2) IA=ID Code Address : F-A0=VIL (Manufacturer's Code), ID=ID Code, F-BYTE# =VIL : F-A-1, F-A1~F-A18 = VIL, F-BYTE# =VIH : F-A1~F-A18 = VIL

3) SRD = Status Register Data

4) WA=Write Address, WD=Write Data.

F-BYTE# =VIL : Write Address and Write Data must be provided sequentially from 00H to FFH for F-A-1~As.

Page size is 256Byte (256byte x 8bit), F-BYTE# =VIH : Write Address and Write Data must be provided sequentially from 00H to 7FH for F-A0~F-A6. Page size is 128word (128word x 16bit).

5) BA = Block Address

6) DQ6 provides Block Lock Status, DQ6 = 1 : Block Unlock, DQ6 = 0 : Block Locked.

7) Must be set F-RP# to VHH and F-WP# to VIH.

8) Sleep command (F0H) put the device into the sleep mode after completing the current operation. The active current is reduced to deep power -down levels. The Read Array command (FFH) must be written to get the device out of sleep mode.

## BLOCK LOCKING

F-RP#	F-WP1#	F-WP2#	Boot Block	Parameter Block	Main Block	Lock Bit	Write Protection Provided
VHH	X	X	Unlock	Unlock	Unlock	Unlock	All Blocks/LockBits Unlocked (Erase/Program enable)
VIH	VIH	VIH	Unlock	Unlock	Unlock	Unlock	All Blocks/LockBits Unlocked (Erase/Program enable)
VIH	VIH	VIL	Lock	Depend on Lock Bit data 1)	Lock	Lock	Boot block and Main block block (hard)locked, and Parameter block locked by Lock Bit.
VIH	VIL	VIH	Lock	Depend on Lock Bit data 1)	Depend on Lock Bit data 1)	Lock	Boot block (hard)locked, and other blocks locked by Lock Bit.
VIH	VIL	VIL	Lock	Lock	Lock	Lock	All Blocks/LockBits (hard)locked
VIL	X	X	Lock	Lock	Lock	Lock	All Blocks/LockBits locked (Deep Power Down Mode)

1) When the Lock bit is "0", its block cannot be programmed and erased.

Lock bit is set to "0" by LOCK BIT PROGRAM.

Locked bit("0") is cleared to "1" with block memory by BLOCK ERASE on setting unlock mode.

2) F-DQ6 provides Lock Status of each block after writing the Read Lock Status command(71H).

3) F-WP#(1,2) pin must not be switched during performing Read/Write operations or WSM Busy (WSMS=0).

## STATUS REGISTER

Symbol	Status	Definition	
		"1"	"0"
SR.7 (DQ7)	Write State Machine Status	Ready	Busy
SR.6 (DQ6)	Suspend Status	Suspended	Operation in Progress / Completed
SR.5 (DQ5)	Erase Status	Error	Successful
SR.4 (DQ4)	Program Status	Error	Successful
SR.3 (DQ3)	Block Status after Program	Error	Successful
SR.2 (DQ2)	Reserved	-	-
SR.1 (DQ1)	Reserved	-	-
SR.0 (DQ0)	Device Sleep Status	Device in Sleep	Device Not in Sleep

\*The F-RY/BY# is an open drain output pin and indicates status of the internal WSM. When low, it indicates that the WSM is Busy performing an operation. A pull-up resistor of 10K-100K Ohms is required to allow the F-RY/BY# signal to transition high indicating a Ready WSM condition.

\*F-DQ3 indicates the block status after the page programming. When F-DQ3 is "1", the page has the over-programmed cell. If over-program occurs, the device is block fail. However if F-DQ3 is "1", please try the block erase to the block. The block may revive.



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### DEVICE IDENTIFIER CODE

Code	Pins	F-A0	F-DQ7	F-DQ6	F-DQ5	F-DQ4	F-DQ3	F-DQ2	F-DQ1	F-DQ0	Hex. Data
Manufacturer Code		V <sub>IL</sub>	0	0	0	1	1	1	0	0	1CH
Device Code (-T)		V <sub>IH</sub>	0	1	1	0	0	0	1	0	62H
Device Code (-B)		V <sub>IH</sub>	0	1	1	0	0	1	0	0	64H

In the word-wide mode, F-DQ15-8 = 00H.

F-A9 = V<sub>HH</sub> Mode : F-A9 = 11.4V~12.6V Set F-A9 to V<sub>HH</sub> min.200ns before falling edge of F-CE in ready status. Min.200ns after return to V<sub>IH</sub>, device can't be accessed.

F-A1~F-A8, F-A10~F-A18, F-CE#, F-OE# = V<sub>IL</sub>, F-WE# = V<sub>IH</sub>

F-DQ15/A-1 = V<sub>IL</sub> (F-BYTE# = L)

### ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Min	Max	Unit
F-V <sub>cc</sub>	V <sub>cc</sub> voltage (Flash Memory)	With respect to Ground	-0.2	4.6	V
V <sub>I1</sub>	All input or output voltage except V <sub>cc</sub> , A9, RP# 1)		-0.6	4.6	V
V <sub>I2</sub>	A9, RP# supply voltage		-0.6	14.0	V
T <sub>a</sub>	Ambient temperature		-20	85	°C
T <sub>bs</sub>	Temperature under bias		-30	95	°C
T <sub>stg</sub>	Storage temperature		-65	125	°C
I <sub>OUT</sub>	Output short circuit current			100	mA

1) Minimum DC voltage is -0.5V on input/output pins. During transitions, this level may undershoot to -2.0V for periods <20ns. Maximum DC voltage on input/output pins is V<sub>cc</sub>+0.5V which, during transitions, may overshoot to V<sub>cc</sub>+1.5V for periods <20ns.

### CAPACITANCE

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
C <sub>IN</sub>	Input capacitance (Address, Control Pins)	T <sub>a</sub> = 25°C, f = 1MHz, V <sub>in</sub> = V <sub>out</sub> = 0V			8	pF
C <sub>OUT</sub>	Output capacitance				12	pF

### DC ELECTRICAL CHARACTERISTICS (T<sub>a</sub> = -20 ~ 85°C, V<sub>cc</sub> = 2.7V ~ 3.6V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ1)	Max	
I <sub>LI</sub>	Input leakage current	0V ≤ V <sub>IN</sub> ≤ F-V <sub>cc</sub>			±1.0	μA
I <sub>LO</sub>	Output leakage current	0V ≤ V <sub>OUT</sub> ≤ F-V <sub>cc</sub>			±10	μA
ISB1	V <sub>cc</sub> standby current	F-V <sub>cc</sub> =3.6V, V <sub>IN</sub> =V <sub>IL</sub> /V <sub>IH</sub> , F-CE#=F-RP#=F-WP1,2#=V <sub>IH</sub>		50	200	μA
ISB2		F-V <sub>cc</sub> =3.6V, V <sub>IN</sub> =F-GND or F-V <sub>cc</sub> , F-CE#=F-RP#=F-WP1,2#=F-V <sub>cc</sub> ±0.3V		0.1	5	μA
ISB3	V <sub>cc</sub> deep powerdown current	F-V <sub>cc</sub> = 3.6V, V <sub>IN</sub> =V <sub>IL</sub> /V <sub>IH</sub> , F-RP# = V <sub>IL</sub>		5	15	μA
ISB4		F-V <sub>cc</sub> = 3.6V, V <sub>IN</sub> =F-GND or F-V <sub>cc</sub> , F-RP# =F-GND±0.3V		0.1	5	μA
I <sub>CC1</sub>	V <sub>cc</sub> read current for Word or Byte	F-V <sub>cc</sub> = 3.6V, V <sub>IN</sub> =V <sub>IL</sub> /V <sub>IH</sub> , F-CE# = V <sub>IL</sub> , F-RP# = F-OE# = V <sub>IH</sub> , f = 5MHz, I <sub>OUT</sub> = 0mA		7	25	mA
I <sub>CC2</sub>	V <sub>cc</sub> Write current for Word or Byte	F-V <sub>cc</sub> =3.6V, V <sub>IN</sub> =V <sub>IL</sub> /V <sub>IH</sub> , F-CE#=F-WE#=V <sub>IL</sub> , F-RP#=F-OE#=V <sub>IH</sub>			25	mA
I <sub>CC3</sub>	V <sub>cc</sub> program current	F-V <sub>cc</sub> = 3.6V, V <sub>IN</sub> =V <sub>IL</sub> /V <sub>IH</sub> , F-CE# = F-RP# =F-WP1,2# = V <sub>IH</sub>			30	mA
I <sub>CC4</sub>	V <sub>cc</sub> erase current	F-V <sub>cc</sub> = 3.6V, V <sub>IN</sub> =V <sub>IL</sub> /V <sub>IH</sub> , F-CE# = F-RP# =F-WP1,2# = V <sub>IH</sub>			40	mA
I <sub>CC5</sub>	V <sub>cc</sub> suspend current	F-V <sub>cc</sub> = 3.6V, V <sub>IN</sub> =V <sub>IL</sub> /V <sub>IH</sub> , F-CE# = F-RP# =F-WP1,2# = V <sub>IH</sub>			200	μA
I <sub>CC6</sub>	Automatic power saving	F-V <sub>cc</sub> = 3.6V, V <sub>IN</sub> =F-GND or F-V <sub>cc</sub>		0.1	5	μA
I <sub>RP</sub>	F-RP# block unlock current	F-RP# = V <sub>IHH</sub> max			100	μA
I <sub>ID</sub>	F-A9 intelligent identifier current	F-A9 = V <sub>ID</sub> max			100	μA
V <sub>IHH</sub>	F-RP# block unlock voltage		11.4	12.0	12.6	V
V <sub>ID</sub>	F-A9 intelligent identifier voltage		11.4	12.0	12.6	V
V <sub>IL</sub>	Input low voltage		-0.5		0.8	V
V <sub>IH</sub>	Input high voltage		2.0		V <sub>cc</sub> +0.5	V
V <sub>OL</sub>	Output low voltage	I <sub>OL</sub> = 5.8mA			0.45	V
V <sub>OH1</sub>	Output high voltage	I <sub>OH</sub> = -2.5mA	0.85V <sub>cc</sub>			V
V <sub>OH2</sub>		I <sub>OH</sub> = -100μA	V <sub>cc</sub> -0.4			V
V <sub>LKO</sub>	Low V <sub>cc</sub> Lock-Out voltage 2)		1.5		2.5	V

All currents are in RMS unless otherwise noted.

1) Typical values at V<sub>cc</sub>=3.3V, T<sub>a</sub>=25°C

2) To protect against initiation of write cycle during V<sub>cc</sub> power-up/ down, a write cycle is locked out for V<sub>cc</sub> less than V<sub>LKO</sub>.

If V<sub>cc</sub> is less than V<sub>LKO</sub>, Write State Machine is reset to read mode. When the Write State Machine is in Busy state, if V<sub>cc</sub> is less than V<sub>LKO</sub>, the alteration of memory contents may occur.



# PRELIMINARY

Notice : This is not a final specification.  
Some parametric limits are subject to change.

MITSUBISHI LSIs  
**M6MFB/T16S2TP**  
16777216-BIT (2M x 8-BIT/1M x 16-BIT)  
CMOS 3.3V-ONLY FLASH MEMORY

### AC ELECTRICAL CHARACTERISTICS (Ta = -20 ~ 85°C, Vcc = 2.7V ~ 3.6V, unless otherwise noted)

#### Read-Only Mode

Symbol		Parameter	Limits			Unit
			Min	Typ	Max	
tRC	tAVAV	Read cycle time	110			ns
ta (AD)	tAVQV	Address access time			110	ns
ta (CE)	tELQV	Chip enable access time			110	ns
ta (OE)	tGLQV	Output enable access time			55	ns
tCLZ	tELQX	Chip enable to output in low-Z	0			ns
tDF(CE)	tEHQZ	Chip enable high to output in high Z			30	ns
tOLZ	tGLQX	Output enable to output in low-Z	0			ns
tDF(OE)	tGHQZ	Output enable high to output in high Z			30	ns
tPHZ	tPLQZ	F-RP# low to output high-Z			300	ns
ta(BYTE)	tFL/HQV	F-BYTE# access time			110	ns
tBHZ	tFLQZ	F-BYTE# low to output high-Z			30	ns
tOH	tOH	Output hold from F-CE#, F-OE#, addresses	0			ns
tBCD	tELFL/H	F-CE# low to F-BYTE# high or low			5	ns
tBAD	tAVFL/H	Address to F-BYTE# high or low			5	ns
tOEH	tWHGL	F-OE# hold from F-WE# high	110			ns
tPWH	tPEHL	F-RP# high recovery to F-CE# low	500			ns

Timing measurements are made under AC waveforms for read operations.

### AC ELECTRICAL CHARACTERISTICS (Ta = -20 ~ 85°C, Vcc = 2.7V ~ 3.6V, unless otherwise noted)

#### Write Mode (WE control)

Symbol		Parameter	Limits			Unit
			Min	Typ	Max	
tWC	tAVAV	Write cycle time	110			ns
tAS	tAVWH	Address set-up time	50			ns
tAH	tWHAX	Address hold time	10			ns
tDS	tDVWH	Data set-up time	50			ns
tDH	tWHDX	Data hold time	10			ns
tCS	tELWL	Chip enable set-up time	0			ns
tCH	tWHEH	Chip enable hold time	0			ns
tWP	tWLWH	Write pulse width	60			ns
tWPH	tWHWL	Write pulse width high	20			ns
tBS	tFL/HWH	Byte enable high or low set-up time	50			ns
tBH	tWHFL/H	Byte enable high or low hold time	110			ns
tBLS	tPHHWH	Block Lock set-up to write enable high	110			ns
tWPS						
tBLH	tQVPH	Block Lockhold from valid SRD	0			ns
tWPH						
tDAP	tWHRH1	Duration of auto-program operation		4	80	ms
tDAE	tWHRH2	Duration of auto-block erase operation		40	600	ms
tWHRL	tWHRL	Write enable high to F-RY/BY# low			110	ns
tPS	tPHWL	F-RP# high recovery to write enable low	500			ns

Read timing parameters during command write operations mode are the same as during read-only operations mode.  
Typical values at F-Vcc=3.3V, Ta=25°C



# PRELIMINARY

Notice : This is not a final specification.  
Some parametric limits are subject to change.

## MITSUBISHI LSIs M6MFB/T16S2TP 16777216-BIT (2M x 8-BIT/1M x 16-BIT) CMOS 3.3V-ONLY FLASH MEMORY

### AC ELECTRICAL CHARACTERISTICS (Ta = -20 ~ 85°C, Vcc = 2.7V ~ 3.6V, unless otherwise noted)

#### Write Mode (CE control)

Symbol		Parameter	Limits			Unit
			Min	Typ	Max	
tWC	tAVAV	Write cycle time	110			ns
tAS	tAVEH	Address set-up time	50			ns
tAH	tEHAX	Address hold time	10			ns
tDS	tDVEH	Data set-up time	50			ns
tDH	tEHDX	Data hold time	10			ns
tWS	tWLEL	Write enable set-up time	0			ns
tWH	tEHWL	Write enable hold time	0			ns
tCEP	tELEH	F-CE# pulse width	60			ns
tCEPH	tEHEL	F-CE# pulse width high	20			ns
tBS	tFL/HEH	Byte enable high or low set-up time	50			ns
tBH	tEHFL/H	Byte enable high or low hold time	110			ns
tBLS	tPHHEH	Block Lock set-up to write enable high	110			ns
tWPS						
tBLH	tQVPH	Block Lockhold from valid SRD	0			ns
tWPH						
tDAP	tEHRH1	Duration of auto-program operation		4	80	ms
tDAE	tEHRH2	Duration of auto-block erase operation		40	600	ms
tEHRH	tEHRH	F-CE# enable high to F-RY/BY# low			110	ns
tPS	tPHL	F-RP# high recovery to write enable low	500			ns

Read timing parameters during command write operations mode are the same as during read-only operations mode.  
Typical values at Vcc=3.3V, Ta=25°C

#### Erase and Program Performance

Parameter	Min	Typ	Max	Unit
Block Erase Time		40	600	ms
Main Block Write Time (Page Mode)		1.3	5	sec
Page Write Time		4	80	ms

#### Vcc Power Up / Down Timing

Symbol	Parameter	Min	Typ	Max	Unit
tVCS	F-RP = VIH set-up time from Vccmin	2			μs

During power up/down, by the noise pulses on control pins, the device has possibility of accidental erasure or programming. The device must be protected against initiation of write cycle for memory contents during power up/down. The delay time of min.2μsec is always required before read operation or write operation is initiated from the time Vcc reaches Vccmin during power up/down. By holding RP# VIL, the contents of memory is protected during Vcc power up/down. During power up, RP# must be held VIL for min.2μs from the time Vcc reaches Vccmin. During power down, RP# must be held VIL until Vcc reaches GND. RP# doesn't have latch mode, so RP# must be held VIH during read operation or erase/program operation.



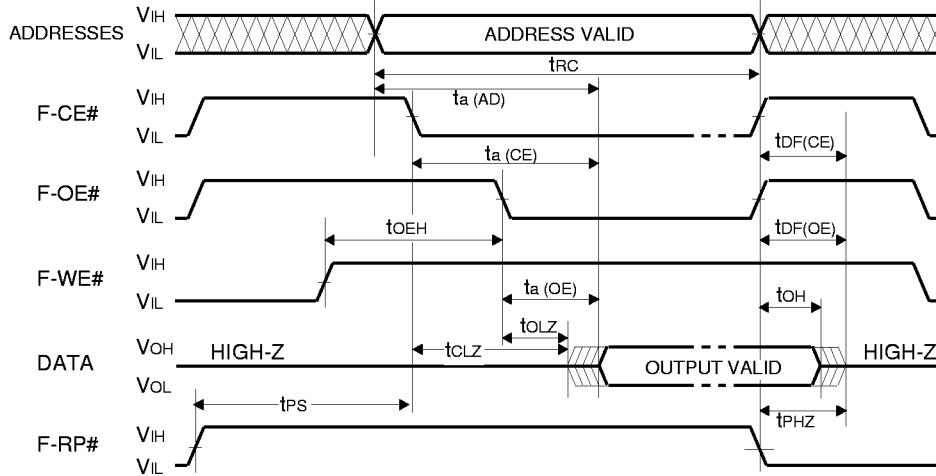


# PRELIMINARY

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MITSUBISHI LSIs  
**M6MFB/T16S2TP**  
16777216-BIT (2M x 8-BIT/1M x 16-BIT)  
CMOS 3.3V-ONLY FLASH MEMORY

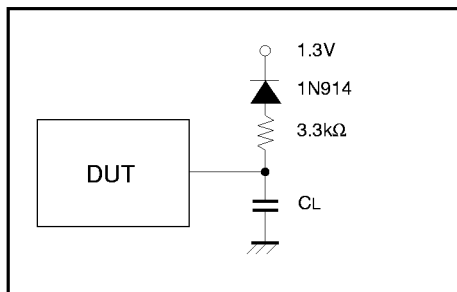
## AC WAVEFORMS FOR READ OPERATION AND TEST CONDITIONS



## TEST CONDITIONS FOR AC CHARACTERISTICS

Test Configuration		F-Vcc=2.7V ~ 3.6V
Input voltage	V <sub>IL</sub>	0V
	V <sub>IH</sub>	3.0V
Input rise and fall times (10%-90%)		5ns
Reference voltage at timing measurement		1.5V
Capacitance Load value	CL	100pF

Output load : 1TTL gate + CL  
or

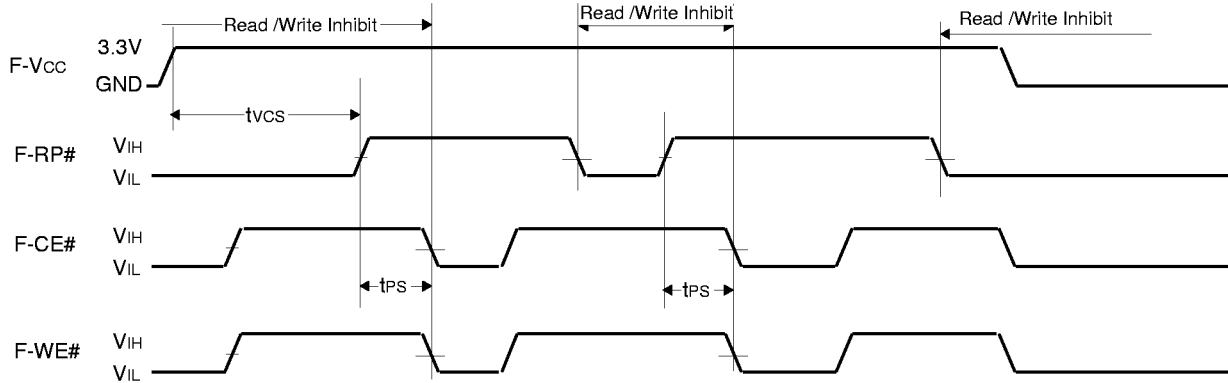


# PRELIMINARY

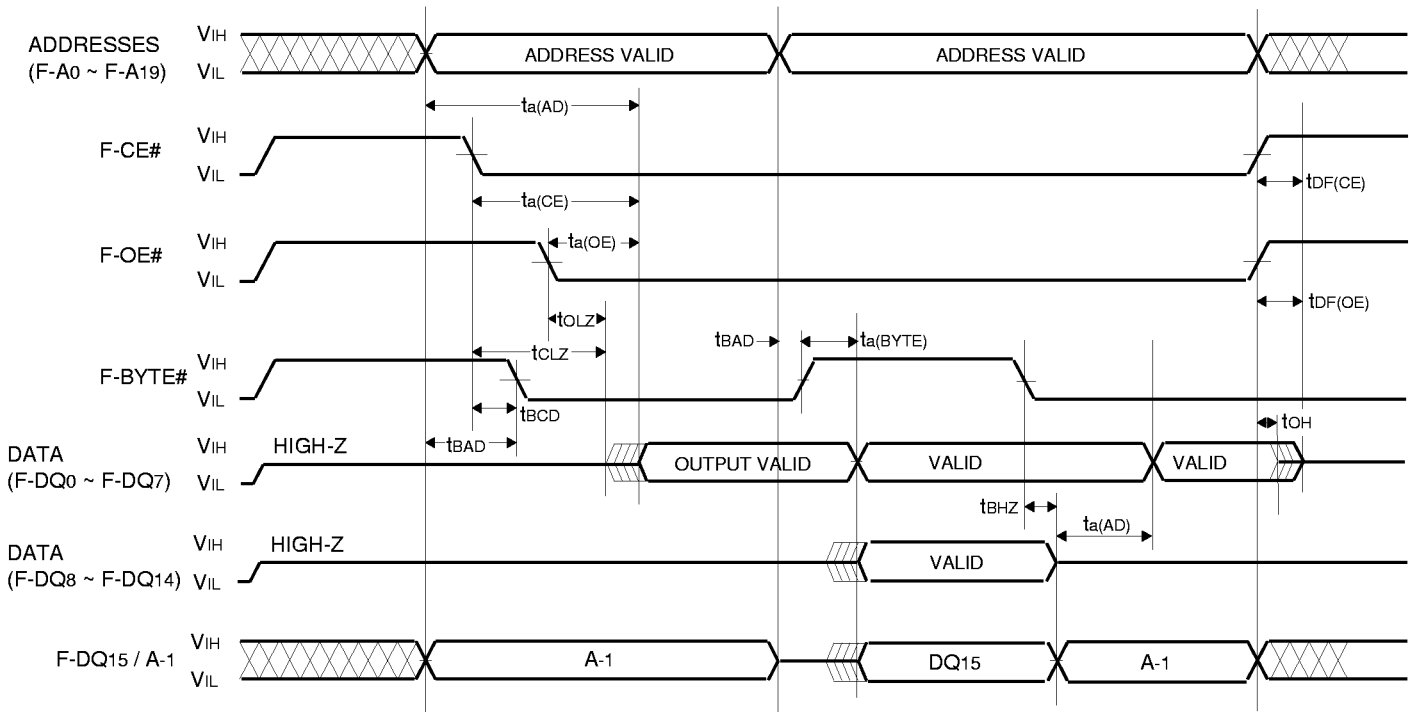
Notice : This is not a final specification.  
Some parametric limits are subject to change.

MITSUBISHI LSIs  
**M6MFB/T16S2TP**  
16777216-BIT (2M x 8-BIT/1M x 16-BIT)  
CMOS 3.3V-ONLY FLASH MEMORY

### Vcc POWER UP / DOWN TIMING



### BYTE# AC WAVEFORMS FOR READ OPERATION



When F-BYTE#=VIH, F-CE#=F-OE#=VIL, DQ15/A-1 is output status. At this time, input signal must not be applied.

# PRELIMINARY

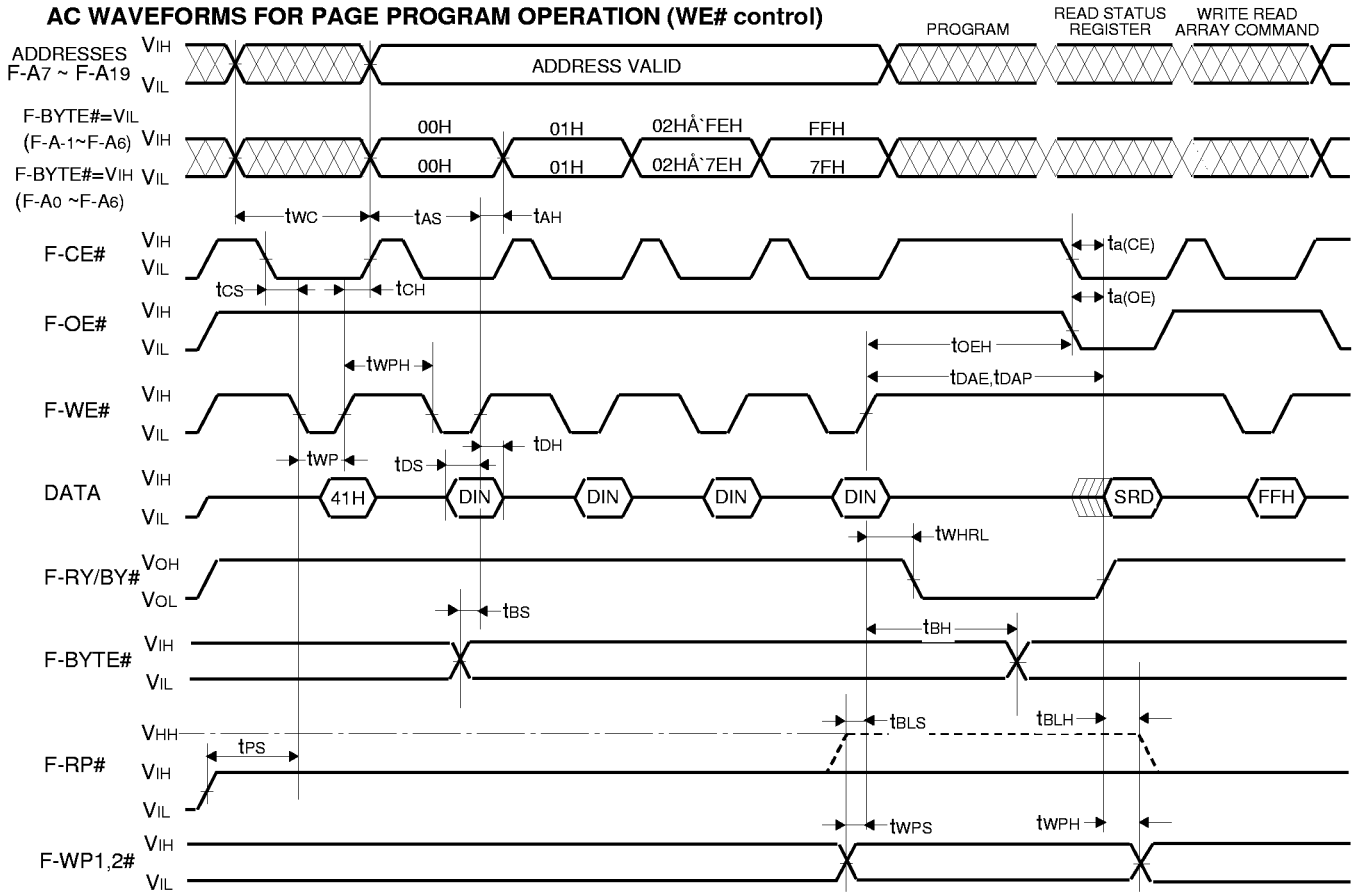
Notice : This is not a final specification.  
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## MITSUBISHI LSIs

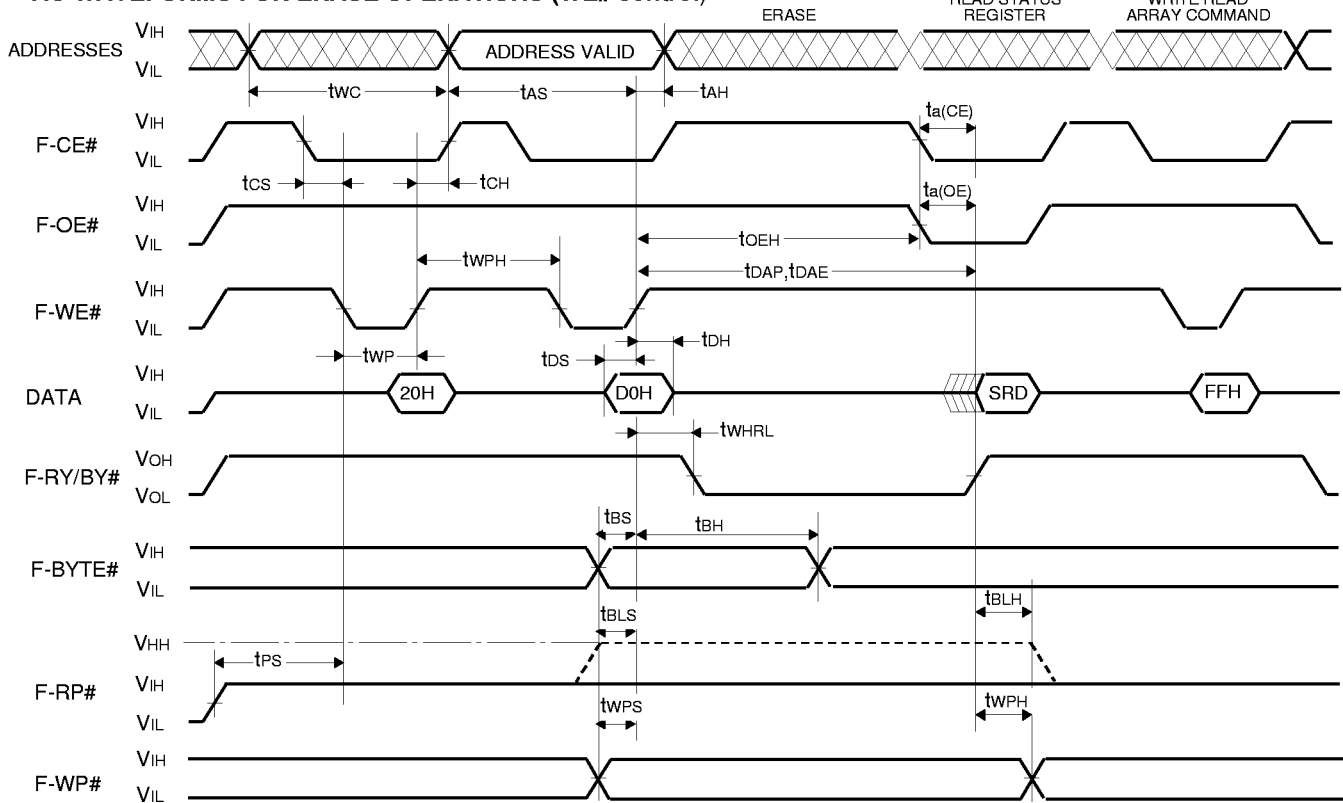
# M6MFB/T16S2TP

1677216-BIT (2M x 8-BIT/1M x 16-BIT)  
CMOS 3.3V-ONLY FLASH MEMORY

### AC WAVEFORMS FOR PAGE PROGRAM OPERATION (WE# control)



### AC WAVEFORMS FOR ERASE OPERATIONS (WE# control)



# PRELIMINARY

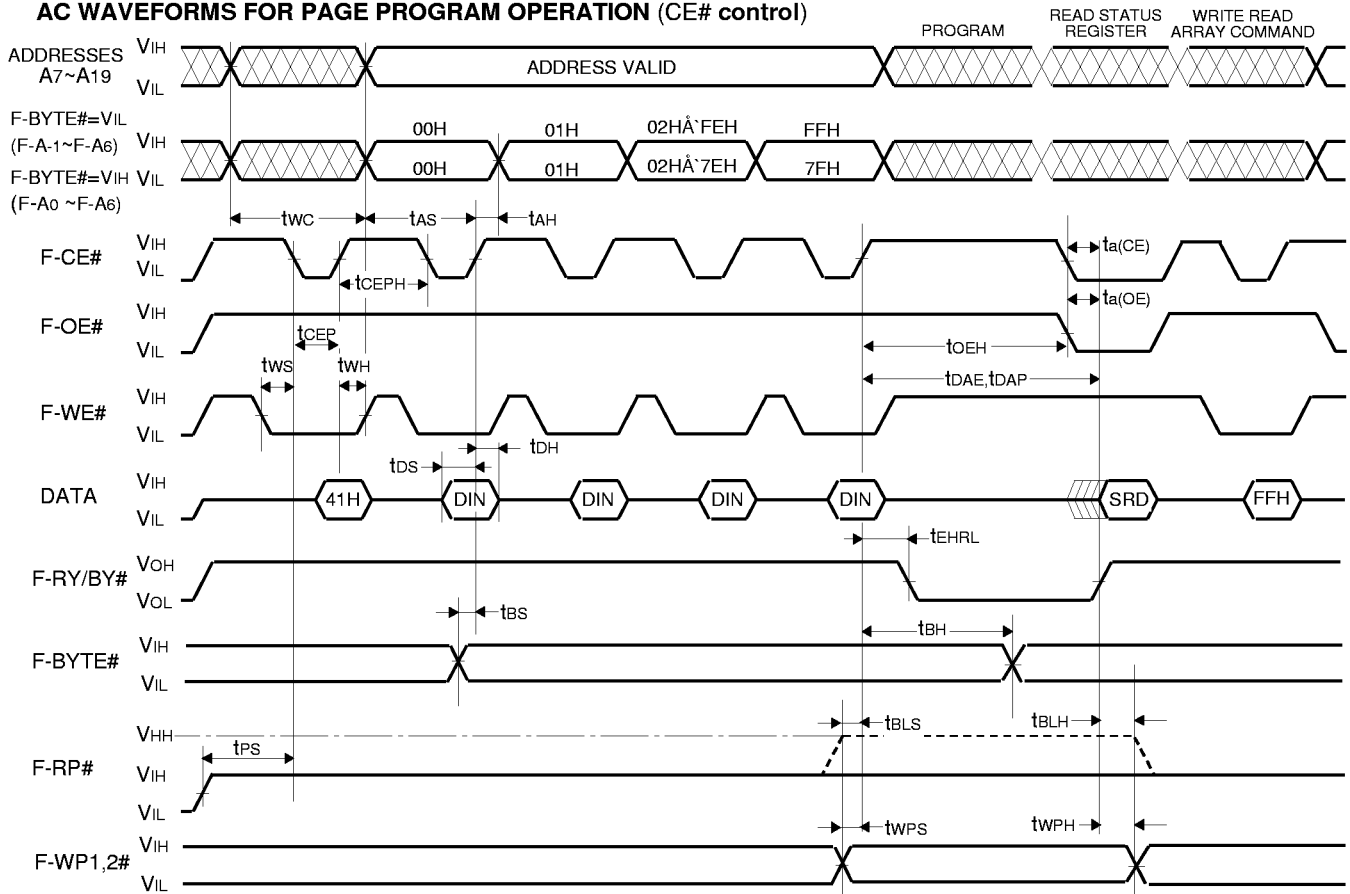
Notice : This is not a final specification.  
Some parametric limits are subject to change.

## MITSUBISHI LSIs

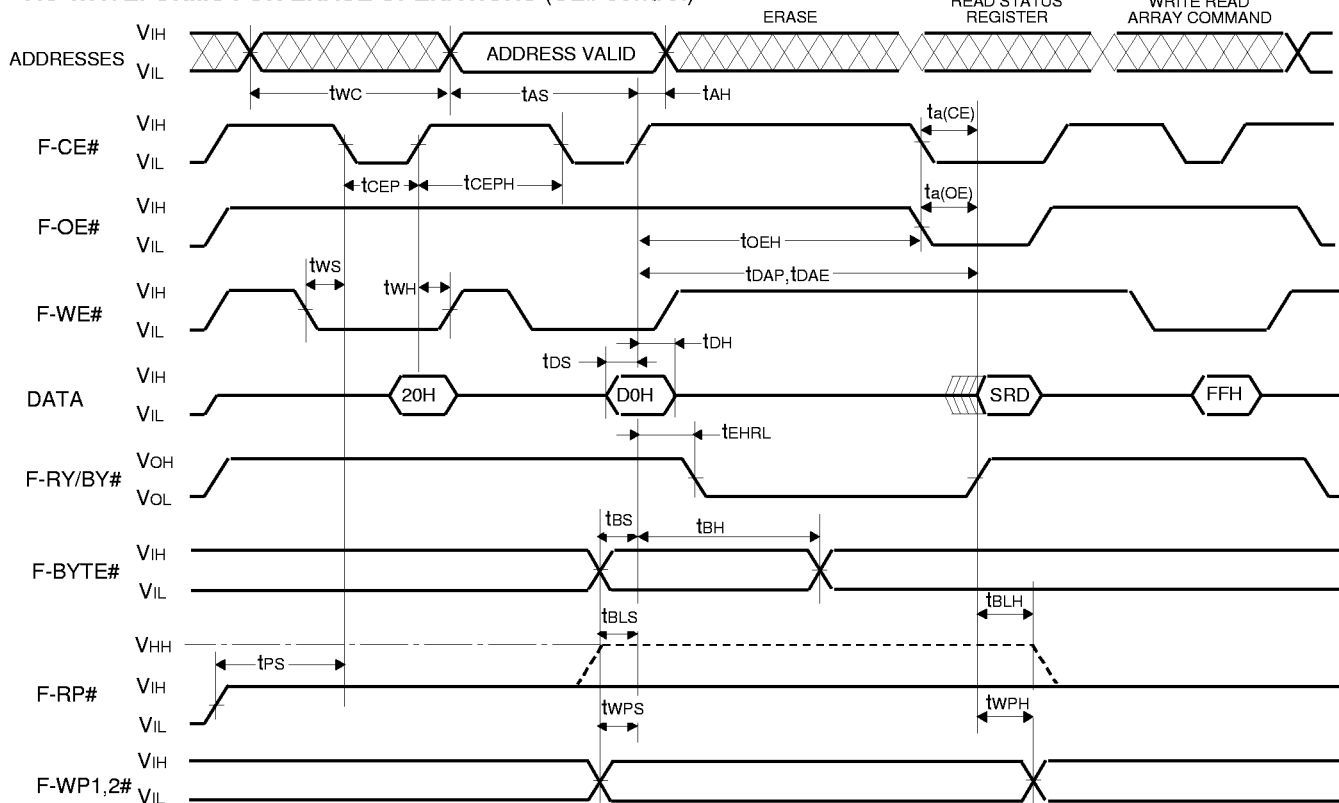
# M6MFB/T16S2TP

1677216-BIT (2M x 8-BIT/1M x 16-BIT)  
CMOS 3.3V-ONLY FLASH MEMORY

### AC WAVEFORMS FOR PAGE PROGRAM OPERATION (CE# control)



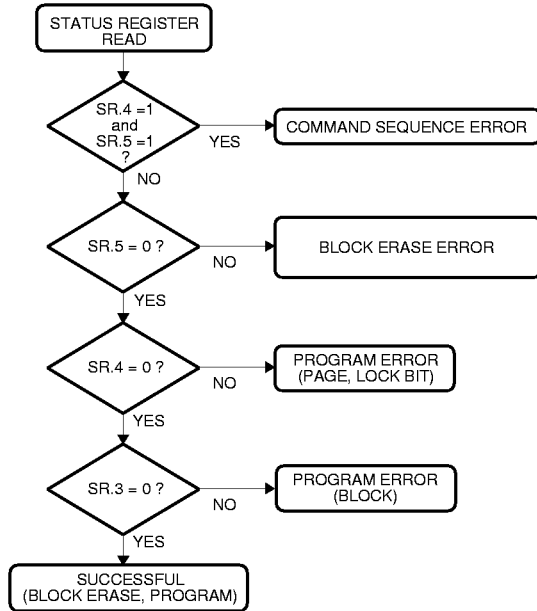
### AC WAVEFORMS FOR ERASE OPERATIONS (CE# control)



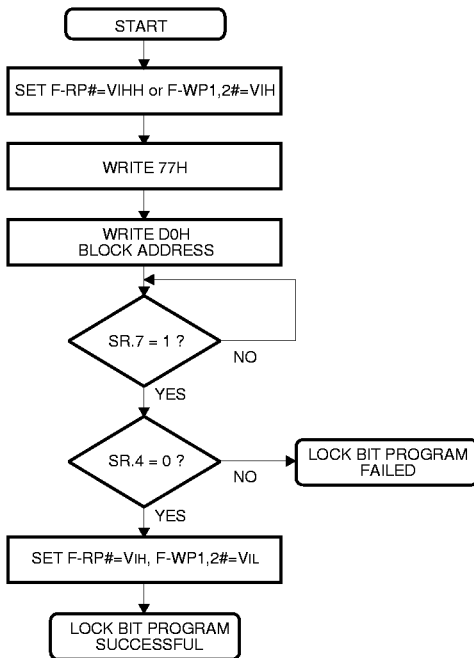
# PRELIMINARY

Notice : This is not a final specification.  
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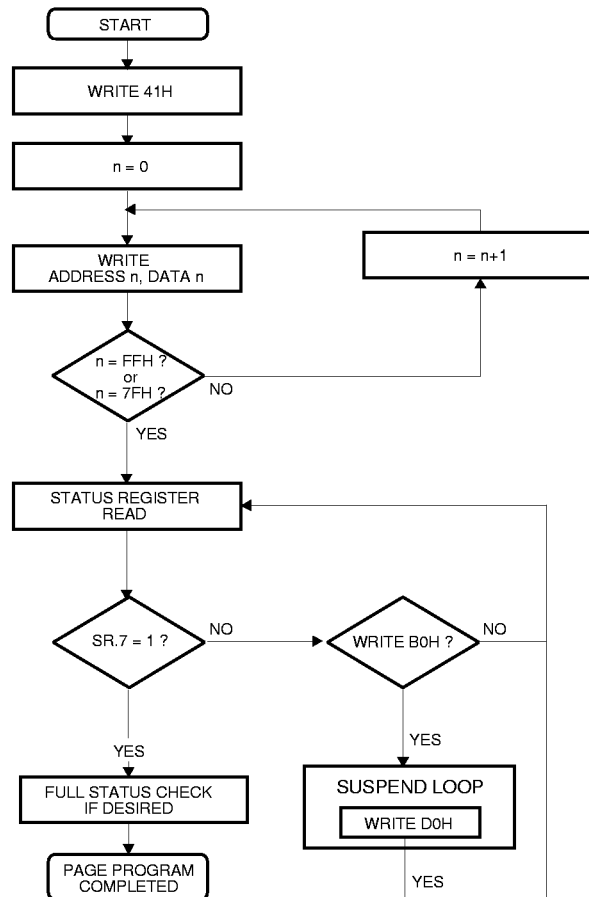
## FULL STATUS CHECK PROCEDURE



## LOCK BIT PROGRAM FLOW CHART



## PAGE PROGRAM FLOW CHART

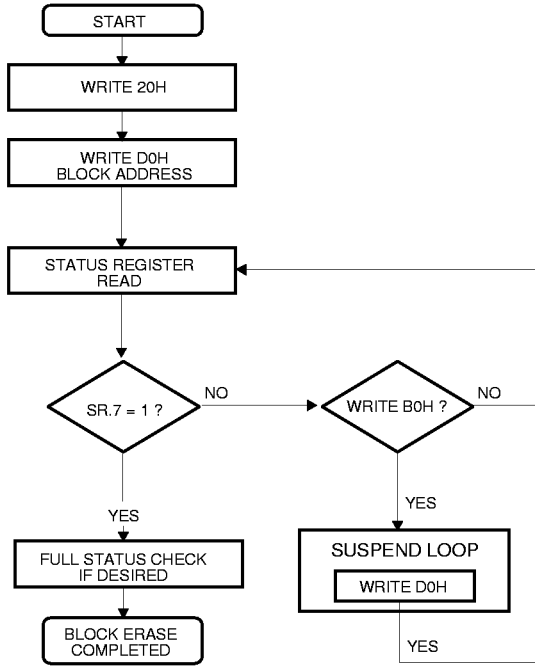


# PRELIMINARY

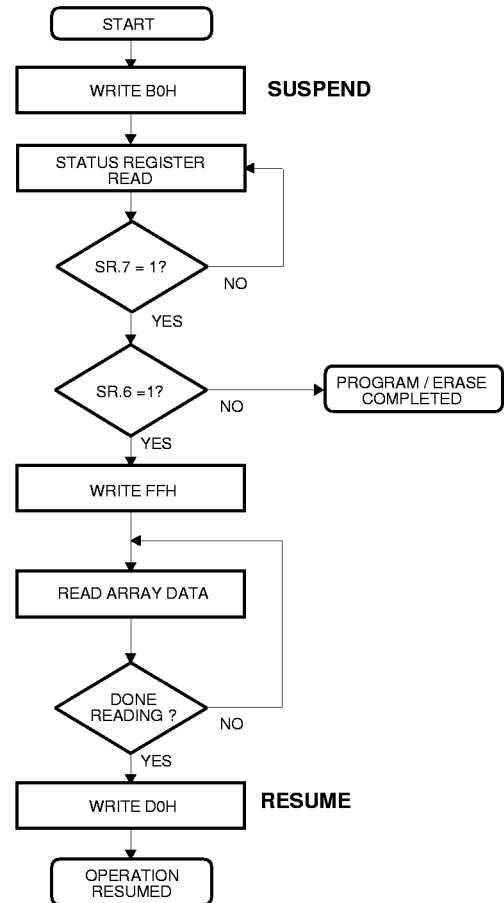
Notice : This is not a final specification.  
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MITSUBISHI LSIs  
**M6MFB/T16S2TP**  
16777216-BIT (2M x 8-BIT/1M x 16-BIT)  
CMOS 3.3V-ONLY FLASH MEMORY

### BLOCK ERASE FLOW CHART



### SUSPEND / RESUME FLOW CHART



# PRELIMINARY

Notice : This is not a final specification.  
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## MITSUBISHI LSIs M6MFB/T16S2TP

2097152-BIT (256k x 8-BIT)  
CMOS STATIC RAM

### FUNCTION

The SRAM of the M6MFT/B16S2TP operation mode is determined by a combination of the device control inputs S-S1#,S-S2,S-W# and S-OE#.

Each mode is summarized in the function table.

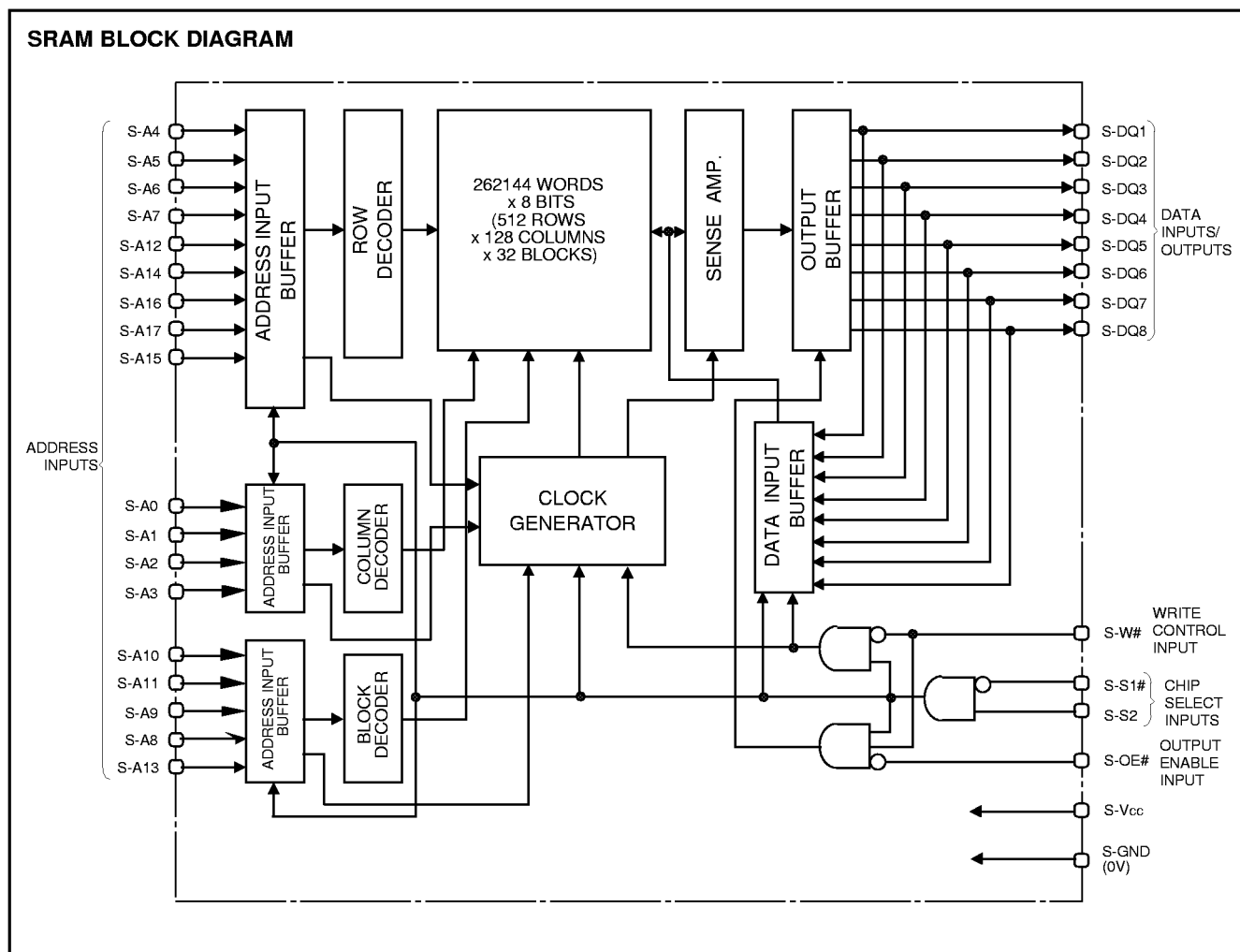
A write cycle is executed whenever the low level S-W# overlaps with the low level S-S1# and the high level S-S2. The address must be set up before the write cycle and must be stable during the entire cycle. The data is latched into a cell on the trailing edge of S-W#,S-S1# or S-S2, whichever occurs first, requiring the set-up and hold time relative to these edge to be maintained. The output enable input S-OE# directly controls the output stage. Setting the S-OE# at a high level, the output stage is in a high-impedance state, and the data bus contention problem in the write cycle is eliminated.

A read cycle is executed by setting S-W# at a high level and S-OE# at a low level while S-S1# and S-S2 are in an active state(S-S1#=L,S-S2=H).

When setting S-S1# at a high level or S-S2 at a low level, the chip are in a non-selectable mode in which both reading and writing are disabled. In this mode, the output stage is in a high-impedance state, allowing OR-tie with other chips and memory expansion by S-S1# and S-S2. The power supply current is reduced as low as the stand-by current which is specified as Icc3 or Icc4, and the memory data can be held at +2V power supply, enabling battery back-up operation during power failure or power-down operation in the non-selected mode.

### FUNCTION TABLE

S-S1#	S-S2	S-W#	S-OE#	Mode	DQ	Icc
X	L	X	X	Non selection	High-impedance	Stand-by
H	X	X	X	Non selection	High-impedance	Stand-by
L	H	L	X	Write	Din	Active
L	H	H	L	Read	Dout	Active
L	H	H	H		High-impedance	Active



# PRELIMINARY

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## MITSUBISHI LSIs M6MFB/T16S2TP

2097152-BIT (256k x 8-BIT)  
CMOS STATIC RAM

### ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
S-V <sub>cc</sub>	Supply voltage (SRAM)	With respect to GND	-0.3* ~ 4.6	V
V <sub>I</sub>	Input voltage		-0.3* ~ V <sub>cc</sub> + 0.5 (Max 4.6)	V
V <sub>O</sub>	Output voltage		0 ~ V <sub>cc</sub>	V
P <sub>d</sub>	Power dissipation	T <sub>a</sub> =25°C	700	mW
T <sub>opr</sub>	Operating temperature		-20 ~ 85	°C
T <sub>stg</sub>	Storage temperature		-65 ~ 150	°C

\* -3.0V in case of AC ( Pulse width ≤ 30ns )

### DC ELECTRICAL CHARACTERISTICS (T<sub>a</sub>=-20 ~ 85°C, V<sub>cc</sub>=2.7V~3.6V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit	
			Min	Typ	Max		
V <sub>IH</sub>	High-level input voltage		2.0		V <sub>cc</sub> +0.3V	V	
V <sub>IL</sub>	Low-level input voltage		-0.3*		0.6	V	
V <sub>OH1</sub>	High-level output voltage 1	I <sub>OH</sub> = -0.5mA	2.4			V	
V <sub>OH2</sub>	High-level output voltage 2	I <sub>OH</sub> = -0.05mA	V <sub>cc</sub> -0.5V			V	
V <sub>OL</sub>	Low-level output voltage	I <sub>OL</sub> =2mA			0.4	V	
I <sub>I</sub>	Input current	V <sub>I</sub> =0 ~ V <sub>cc</sub>			±1	µA	
I <sub>O</sub>	Output current in off-state	S-S <sub>1</sub> =V <sub>IH</sub> or S-S <sub>2</sub> =V <sub>IL</sub> or S-OE=V <sub>IH</sub> V <sub>I/O</sub> =0 ~ S-V <sub>cc</sub>			±1	µA	
I <sub>CC1</sub>	Active supply current (MOS level input)	S-S <sub>1</sub> ≤ 0.2V, S-S <sub>2</sub> ≥ V <sub>cc</sub> - 0.2V other inputs ≤ 0.2V or ≥ S-V <sub>cc</sub> - 0.2V Output-open(duty 100%)	10MHz	-	20	25	mA
			5MHz	-	10	13	
			1MHz	-	3	5	
I <sub>CC2</sub>	Active supply current (TTL level input)	S-S <sub>1</sub> =V <sub>IL</sub> , S-S <sub>2</sub> =V <sub>IH</sub> , other inputs=V <sub>IH</sub> or V <sub>IL</sub> Output-open(duty 100%)	10MHz	-	22	27	mA
			5MHz	-	12	15	
			1MHz	-	3	5	
I <sub>CC3</sub>	Stand-by current	1) S-S <sub>2</sub> ≤ 0.2V, other inputs=0 ~ S-V <sub>cc</sub> 2) S-S <sub>1</sub> ≥ S-V <sub>cc</sub> - 0.2V, S-S <sub>2</sub> ≥ S-V <sub>cc</sub> - 0.2V other inputs=0 ~ S-V <sub>cc</sub>	-20 ~ +85°C	-	-	40	µA
			-20 ~ +40°C	-	-	5	
			+25°C	-	0.3	2	
I <sub>CC4</sub>	Stand-by current	S-S <sub>1</sub> =V <sub>IH</sub> or S-S <sub>2</sub> =V <sub>IL</sub> , other inputs=0 ~ S-V <sub>cc</sub>	-	-	0.33	mA	

\* -3.0V in case of AC ( Pulse width ≤ 30ns )

### CAPACITANCE (T<sub>a</sub>=-20 ~ 85°C, V<sub>cc</sub>=2.7V ~ 3.6V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
C <sub>I</sub>	Input capacitance	V <sub>I</sub> =GND, V <sub>I</sub> =25mVrms, f=1MHz			7	pF
C <sub>O</sub>	Output capacitance	V <sub>O</sub> =GND, V <sub>O</sub> =25mVrms, f=1MHz			9	pF

Note 1: Direction for current flowing into an IC is positive (no mark).

2: Typical value is V<sub>cc</sub> = 3V, T<sub>a</sub> = 25°C





# PRELIMINARY

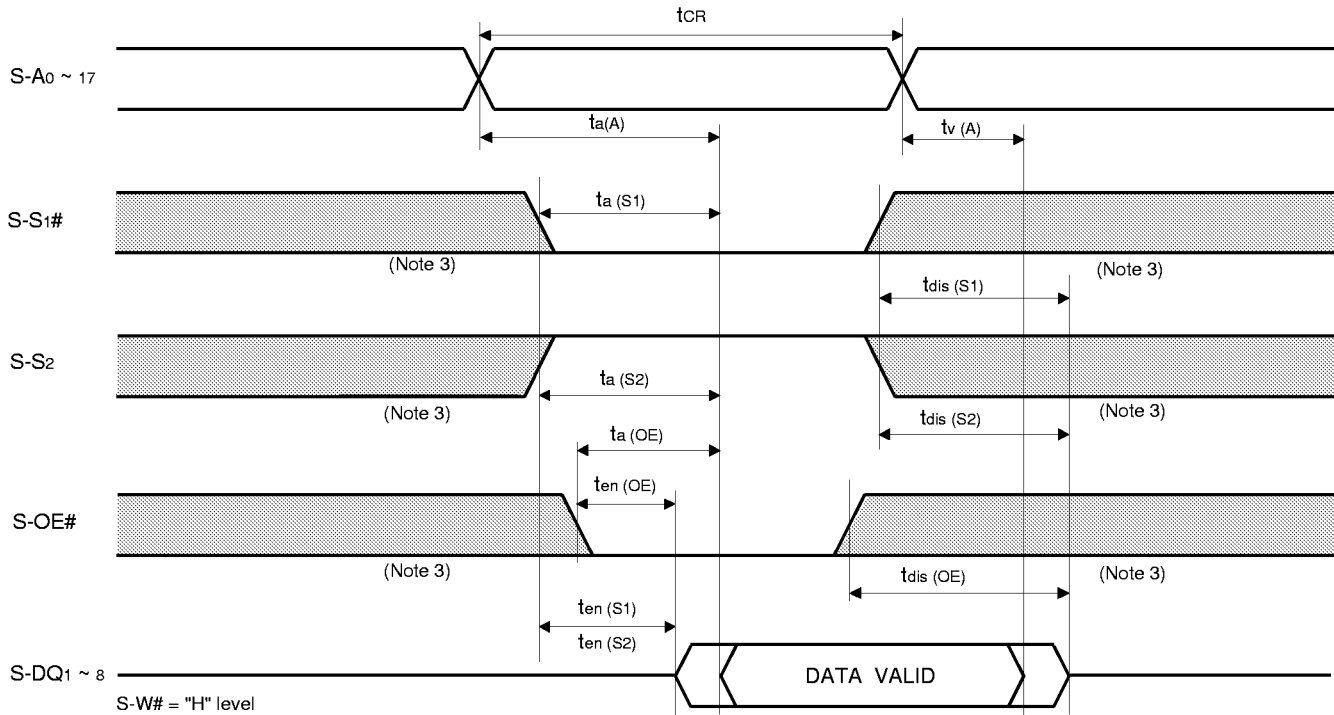
Notice : This is not a final specification.  
Some parametric limits are subject to change.

## MITSUBISHI LSIs M6MFB/T16S2TP

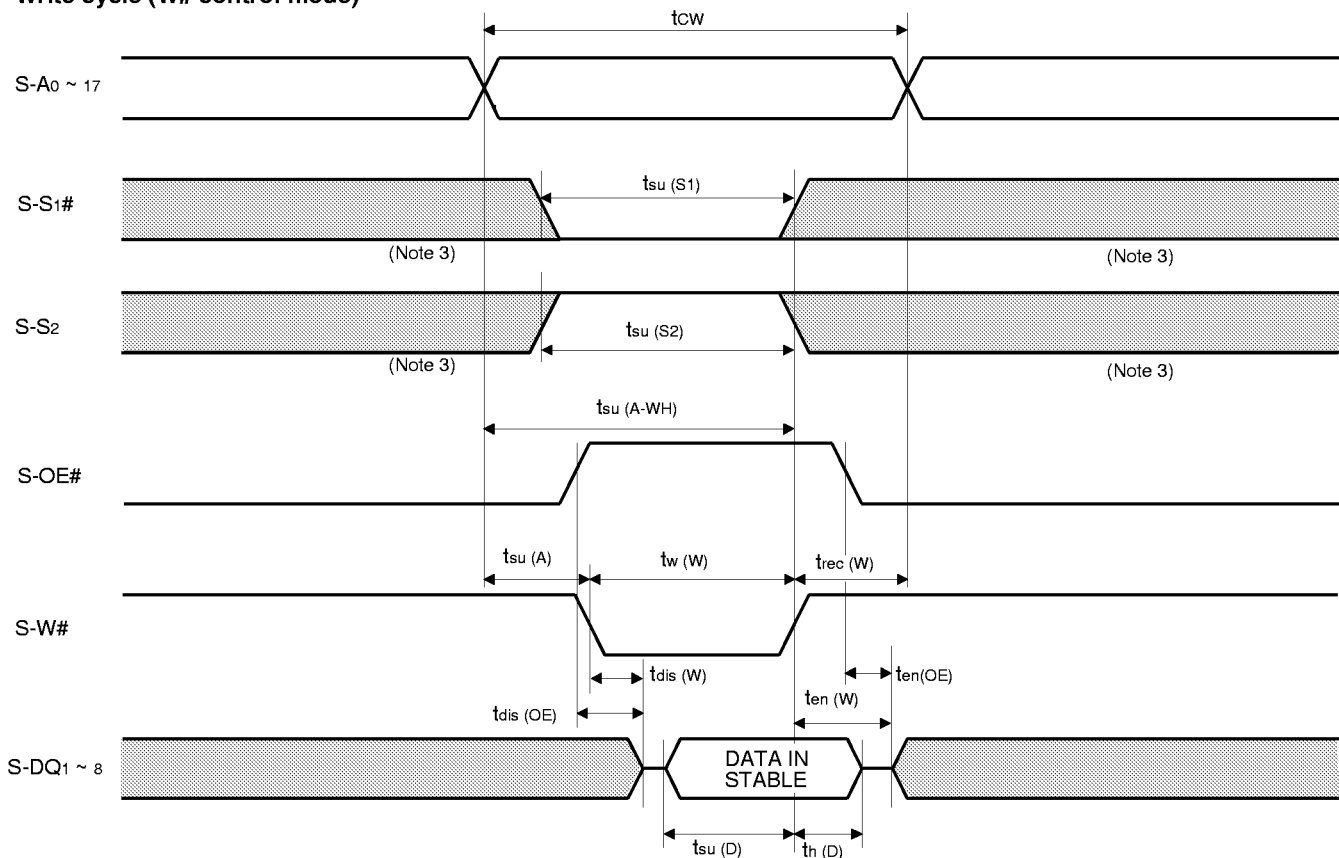
2097152-BIT (256k x 8-BIT)  
CMOS STATIC RAM

### (4) TIMING DIAGRAMS

#### Read cycle



#### Write cycle (W# control mode)



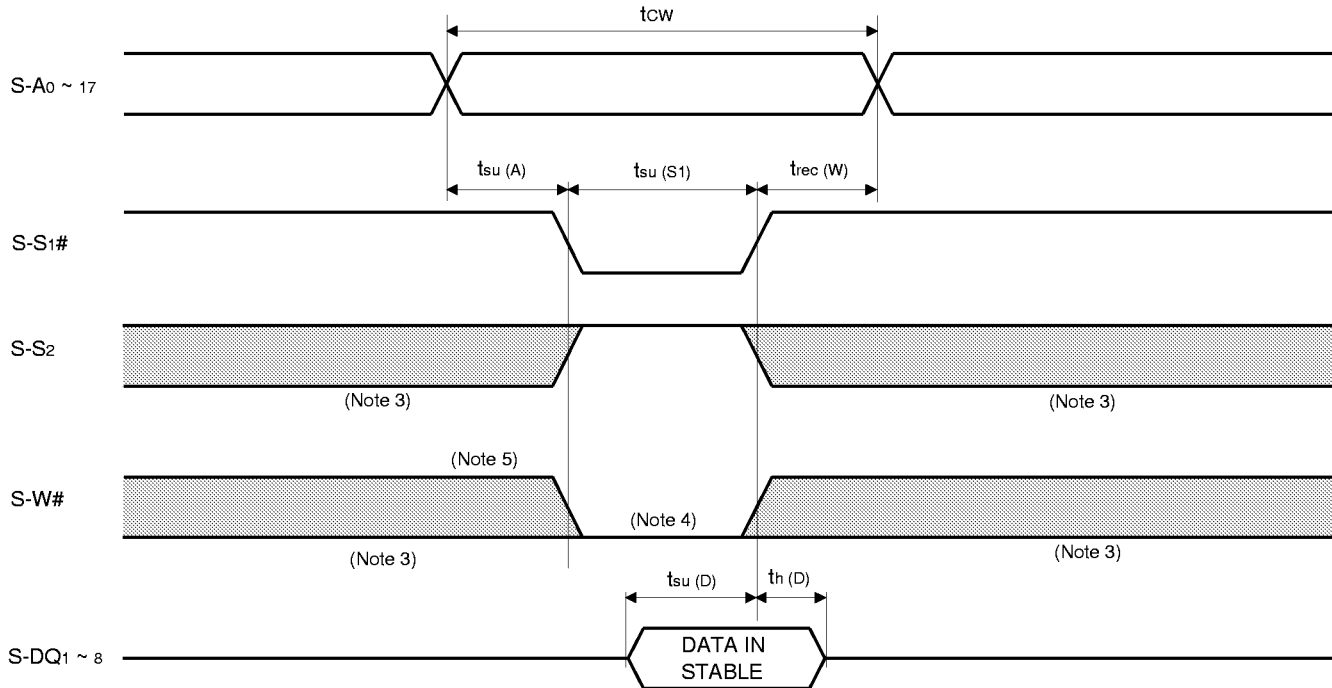
# PRELIMINARY

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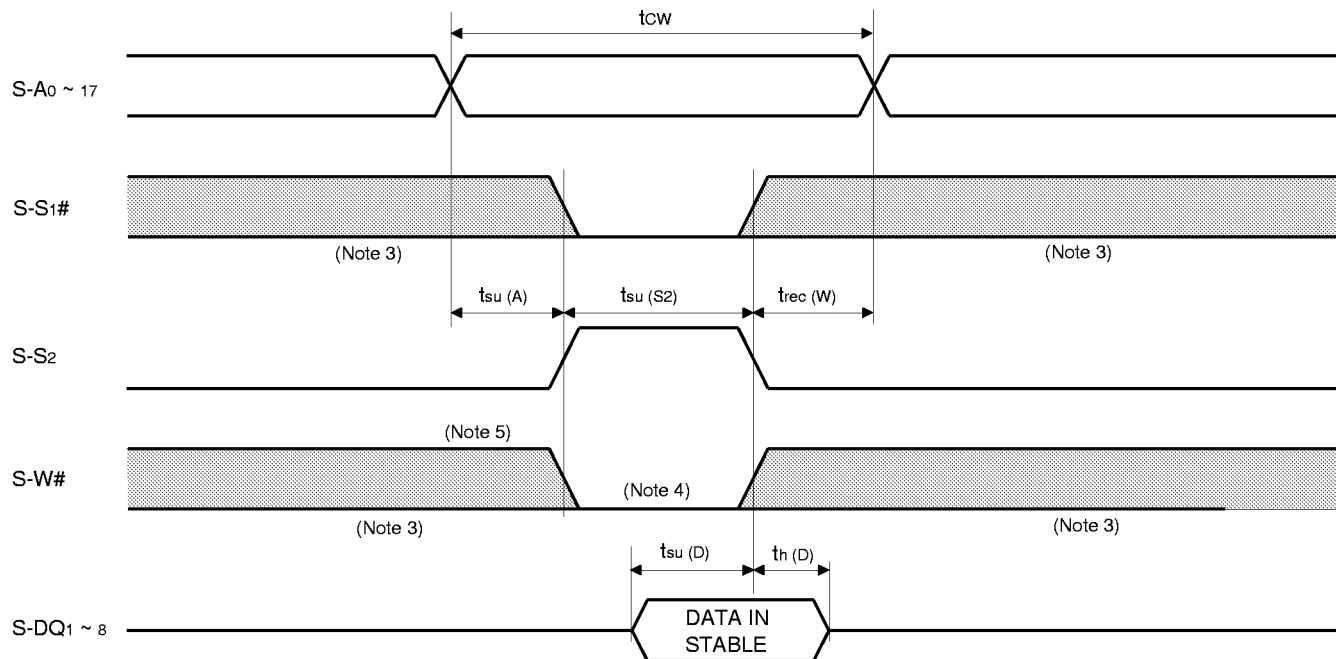
## MITSUBISHI LSIs M6MFB/T16S2TP

2097152-BIT (256k x 8-BIT)  
CMOS STATIC RAM

### Write cycle ( S1# control mode)



### Write cycle (S2 control mode)



Note 3: Hatching indicates the state is "don't care".

4: Writing is executed while S-S2 high overlaps S-S1# and S-W# low.

5: When the falling edge of S-W# is simultaneously or prior to the falling edge of S-S1# or rising edge of S-S2, the outputs are maintained in the high impedance state.

6: Don't apply inverted phase signal externally when DQ pin is output mode.

# PRELIMINARY

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## MITSUBISHI LSIs M6MFB/T16S2TP

2097152-BIT (256k x 8-BIT)  
CMOS STATIC RAM

### POWER DOWN CHARACTERISTICS

#### (1) ELECTRICAL CHARACTERISTICS (Ta = -20 ~ 85°C, unless otherwise noted)

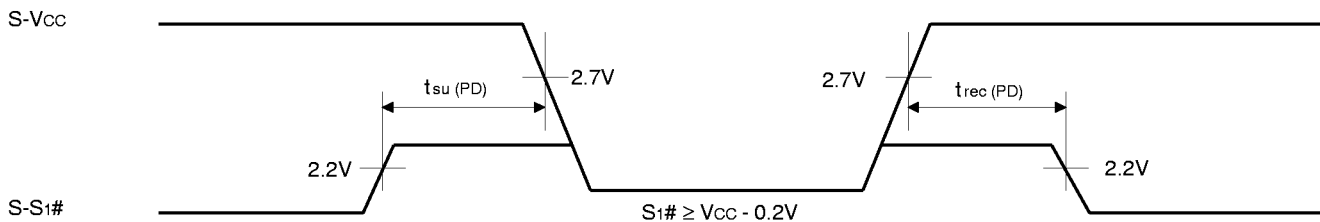
Symbol	Parameter	Test conditions	Limits			Unit	
			Min	Typ	Max		
V <sub>CC</sub> (PD)	Power down supply voltage		2			V	
V <sub>I</sub> (S1#)	Chip select input S-S1#		2.0			V	
V <sub>I</sub> (S2)	Chip select input S-S2				0.2	V	
I <sub>CC</sub> (PD)	Power down supply current	S-V <sub>CC</sub> = 3.0V 1) S-S <sub>2</sub> ≤ 0.2V, other inputs = 0 ~ S-V <sub>CC</sub> 2) S <sub>1</sub> # ≥ S-V <sub>CC</sub> - 0.2V, S <sub>2</sub> ≥ S-V <sub>CC</sub> - 0.2V other inputs = 0 ~ S-V <sub>CC</sub>	-20~+85°C			30	μA
			-20~+40°C			3	
			+25°C		0.3	1	

#### (2) TIMING REQUIREMENTS (Ta = -20 ~ 85°C, unless otherwise noted)

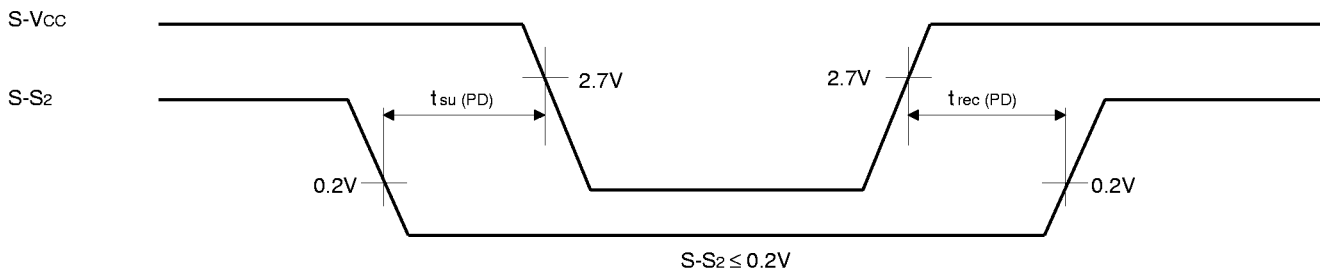
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t <sub>su</sub> (PD)	Power down set up time		0			ns
t <sub>rec</sub> (PD)	Power down recovery time		5			ms

#### (3) POWER DOWN CHARACTERISTICS

##### S1# control mode



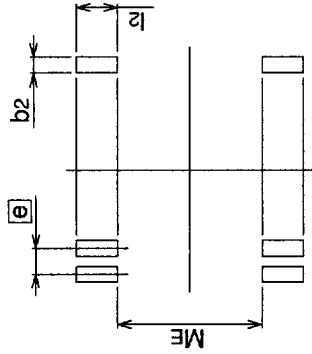
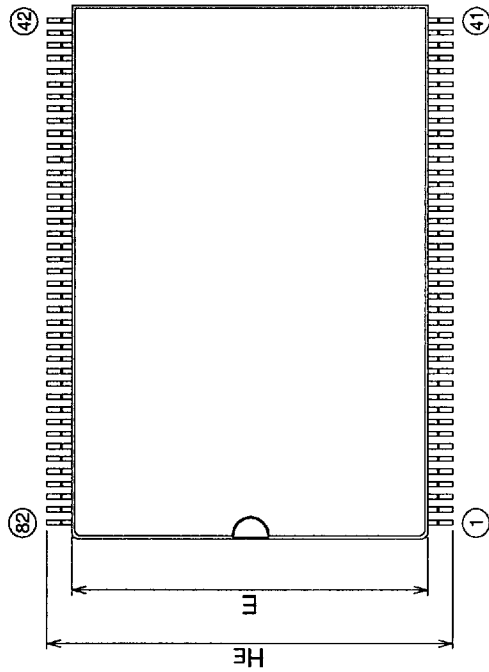
##### S2 control mode



# 82PTA-B

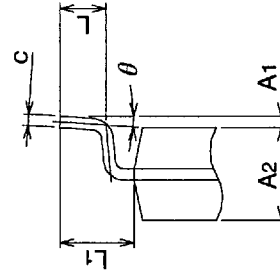
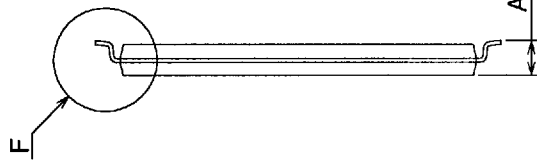
# Plastic 82pin 11.5mm TSOP (II)

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
-	-	0.47	Alloy 42



Recommended Mount Pad

Symbol	Dimension in Millimeters		
	Min	Norm	Max
A	-	-	1.2
A1	0.05	0.125	0.2
A2	-	1.0	-
b	0.11	0.16	0.26
c	0.105	0.125	0.175
D	16.9	17	17.1
E	11.4	11.5	11.6
e	-	0.4	-
HE	12.9	13.1	13.3
L	0.4	0.5	0.6
L1	-	0.8	-
y	-	-	0.08
θ	0°	-	10°
ME	-	11.7	-
l2	0.9	-	-
b2	-	-	-



Detail F

