

# MN863584-D

## 1. TYPE

Gate driver IC with 244-pin output for TFT LCD

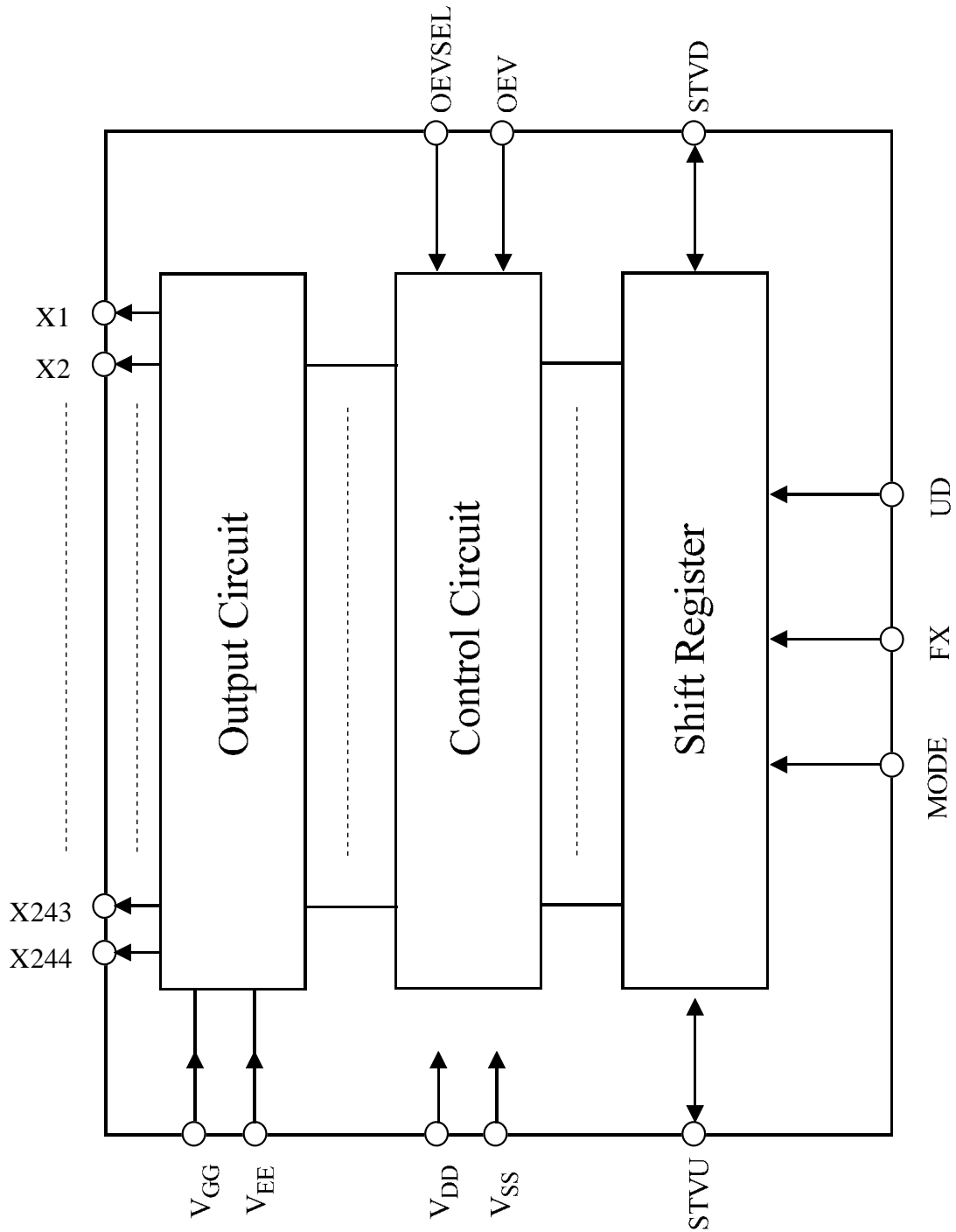
## 2. OVERVIEW

- \* Number of output channels : 244 outputs
- \* Driver operating frequency : 500 kHz max.
- \* LCD drive voltage :  $V_{EE} + 40$  V max.
- \* Driver output level : Binary

## 3. FEATURE

- Incorporating a bidirectional shift register function.

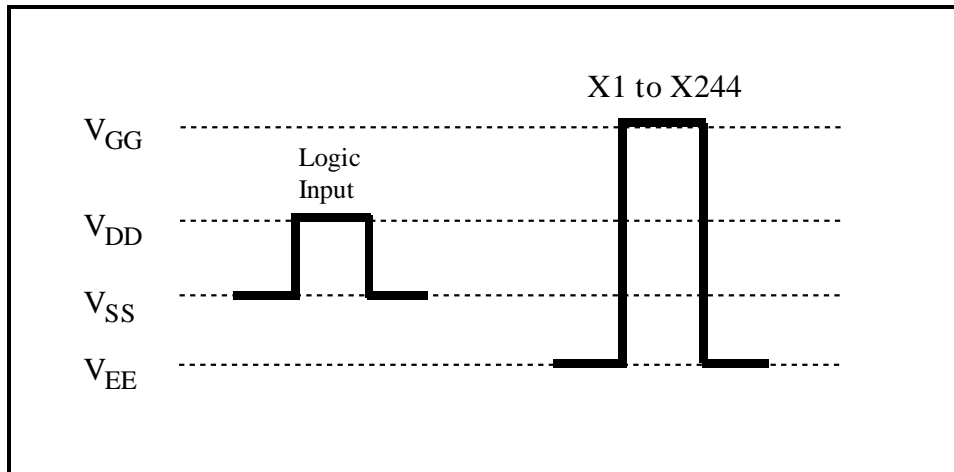
### 4. BLOCK DIAGRAM



## 5. FUNCTIONS

### 5-1) LCD Drive Voltage

Negative LCD drive voltage output is possible on the basis of the logic ground voltage,  $V_{SS}$ .



### 5-2) Operation Mode Selection

#### MODE="H": Positive Logic

The start pulse is fetched at the FX rising edge and the data is shifted.

The carry pulse synchronizes with the FX falling edge.

The high-level start pulse corresponds to the  $V_{GG}$  display voltage.

#### MODE="L": Negative Logic

The start pulse is fetched at the FX falling edge and the data is shifted at the rising edge.

The display voltage will be output only when the FX level is high.

The carry pulse synchronizes with the FX rising edge.

The low-level start pulse corresponds to the  $V_{GG}$  display voltage.

5-3) Selection of Shift Direction and Number of Outputs

The shift direction can be set with UD input.

244-output mode

UD	Start Pulse	Data Shift Direction	Carry Pulse
UD="H"	STVD	X1 → 1X2 → X3 . . . X242 → X243 → X244	STVU
UD="L"	STVU	X244 → X243 → X242 . . . X3 → X2 → X1	STVD

5-4) Non-Display Function

OEVSSEL \ OEV	OEV="H"	OEV="L"
OEVSSEL="H"	ALL V <sub>EE</sub> output	Normal output
OEVSSEL="L"	Normal output	ALL V <sub>EE</sub> output

Set the OEVSSEL to high level and apply high-level input to the OEV. Alternatively, set the OEVSSEL to low level and apply low-level input to the OEV. Then all the outputs will be set to non-display level regardless of the data in the shift register. This function operates without being synchronized with the FX. The above will not reset the shift data.

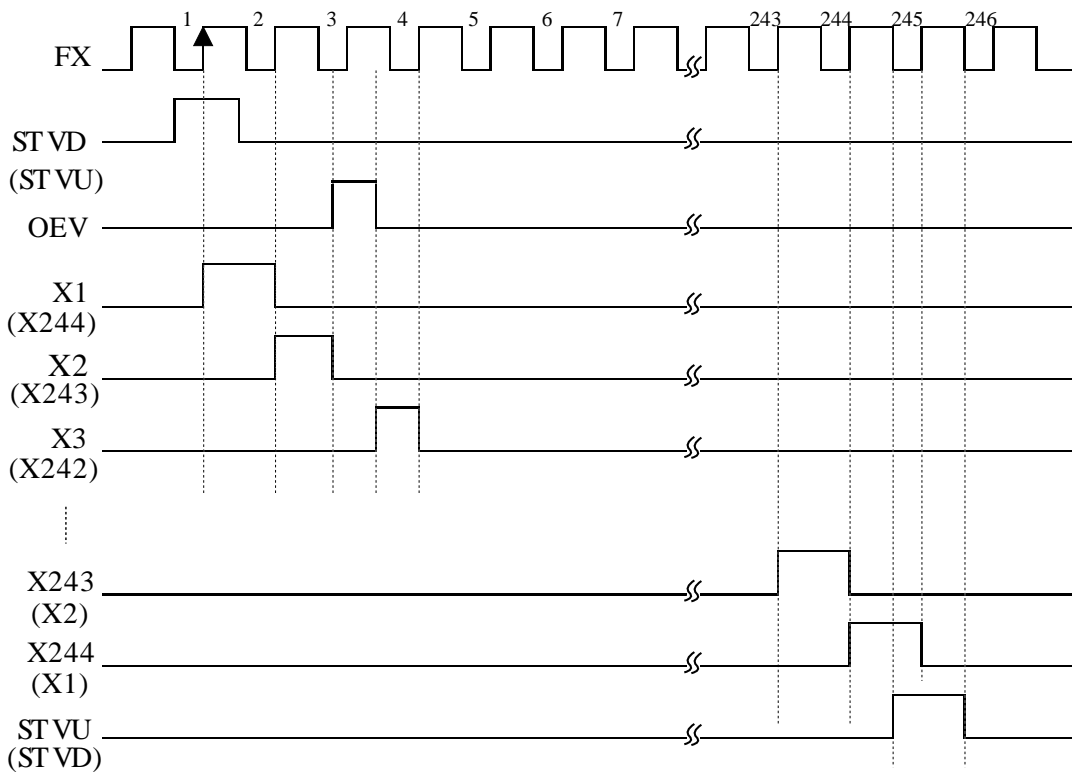
## 6. PIN DESCRIPTIONS

Pin Name	I/O	Function	Description	
FX	I	Shift register clock input pin	Shift clock of the internal shift register	
UD	I	Input pin for selecting the right shift or left shift direction	UD="H": X1 → X244 UD="L": X244 → X1	
STVD / STVU	I/O	Start pulse input and carry pulse output pins		
			STVD	STVU
			UD="H"	Input
UD="L"	Output	Input		
OEVSSEL	I	Input pin for selecting OEVSSEL	OEVSSEL="H": OEVSSEL=Active high OEVSSEL="L": OEVSSEL=Active low	
OEVSSEL	I	Input pin for selecting input polarity	When OEVSSEL and OEVSSEL pins are set to high level or low level, the corresponding LCD drive output pins will be at the level of OFF-potential ( $V_{EE}$ ) without being synchronized with the FX regardless of the contents of the data in the shift register. Not reset.	
MODE	I	Input pin for selecting MODE	MODE="H": Positive-logic operation MODE="L": Negative-logic operation	
X1 to X244	O	LCD drive output pins	$V_{GG}$ or $V_{EE}$ voltage level is output according to OEVSSEL, OEVSSEL, and FX inputs and the data in the shift register.	
$V_{GG}$	Power supply	LCD drive output power supply LCD drive power supply 1	Power supply for the level shifter and output buffer This power supply drives LCD.	
$V_{EE}$	Power supply	$V_{GG}$ systemground LCD drive power supply 2	Ground Provides this pin with LCD drive voltage.	
$V_{DD}$	Power supply	Logic power supply	Power supply for the logic circuit	
$V_{SS}$	Power supply	$V_{DD}$ systemground	Low level reference voltage for logic	
COM1 to COM4		Through wiring pins	Pins which have same name at the input side and output side are connected. They are not connected to a circuit.	
dummy1 to dummy8		Dummy pads	Dummy pads only located. They are not connected to a circuit.	

## 7. BASIC WAVEFORM

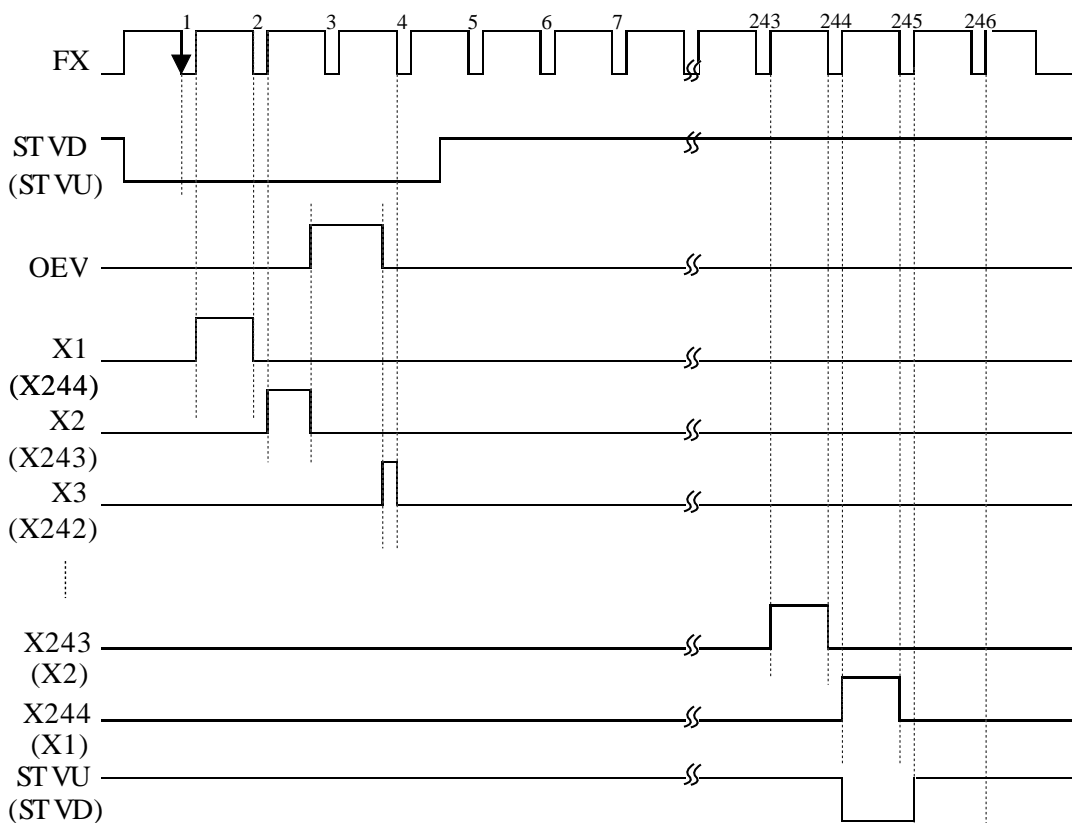
When MODE="H," OEVSEL="H," and UD="H"

( ): UD="L"



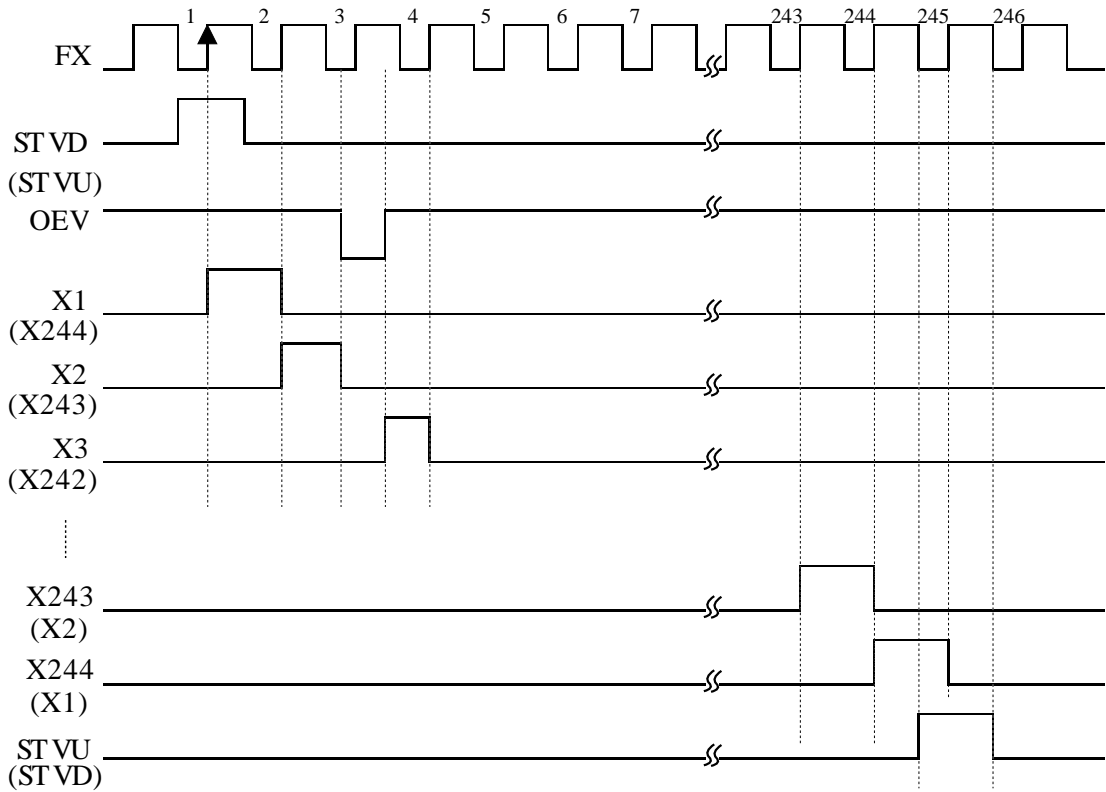
When MODE="L," OEVSEL="H," and UD="H"

( ): UD="L"



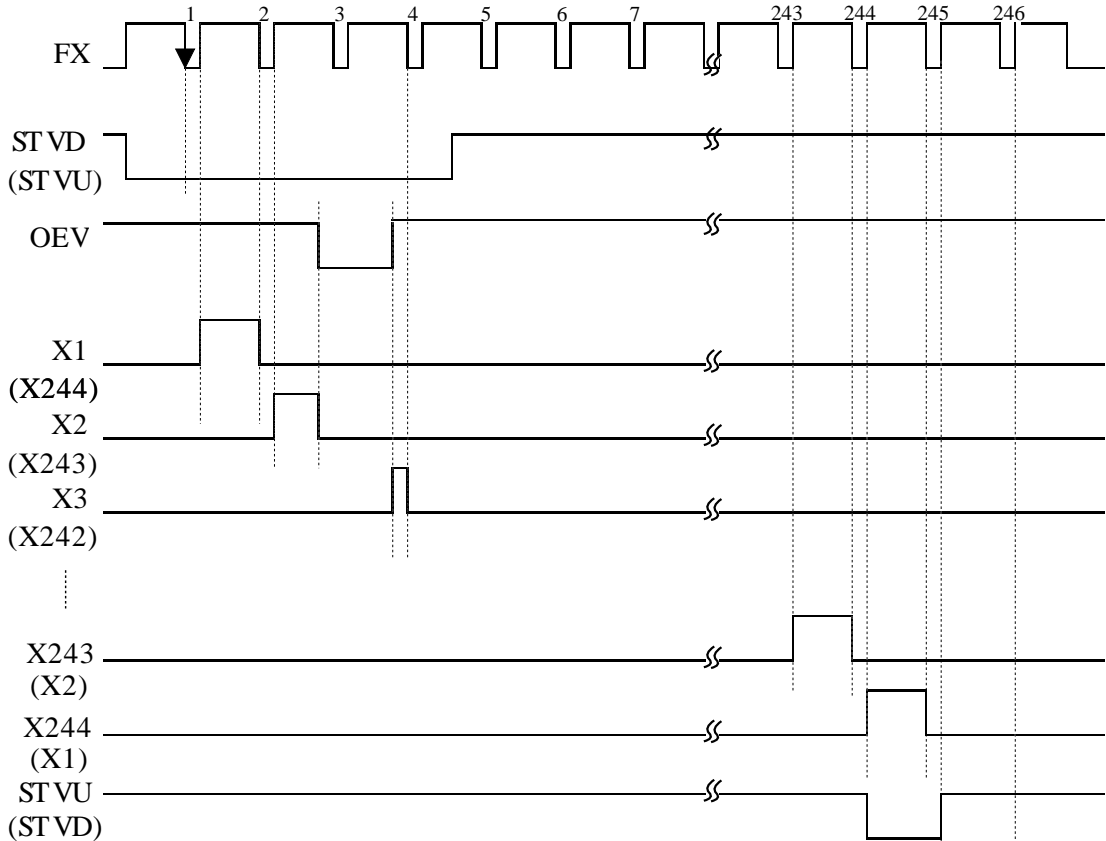
When MODE="H," OEVSEL="L," and UD="H"

( ) : UD="L"



When MODE="L," OEVSEL="L," and UD="H"

( ) : UD="L"



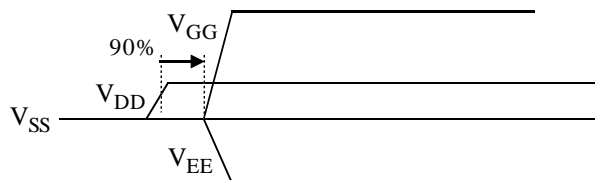
PRODUCT STANDARDS

A. ABSOLUTE MAXIMUM RATINGS

$V_{SS}=0\text{ V}$

Parameter	Symbol	Rating	Unit	
A1	Supply voltage 1	$V_{DD}$	-0.3 to +7.0	V
A2	Supply voltage 2	$V_{GG}$	-0.3 to +44	V
A3	Supply voltage 3	$V_{EE}$	$V_{GG}-44$ to +0.3	V
A4	Digital input voltage	$V_I$	-0.3 to $V_{DD}+0.3$	V
A5	Operating storage temperature	$T_{opr}$	-30 to +85	°C
A6	Operating ambient temperature	$T_a$	-20 to +75	°C
A7	Storage temperature	$T_{stg}$	-55 to +120	°C

- Note 1) The absolute maximum ratings are the limit values beyond which the IC may be broken. They don't assure operation.
- Note 2) The operating storage temperature is the temperature range beyond which the IC may be broken. They don't assure operation.
- Note 3) The values specified in the *Product Standards* are guaranteed on condition that the IC is applied to the manufacturer's standard packages.
- Note 4) Set the drive voltage to satisfy the following condition when the IC is turned on and turned off and while the IC is operating.  
 $V_{EE} \leq V_{GG}$
- Note 5) If voltage is improperly applied to the IC when the IC is turned on, a high current may flow to the IC, and the IC may be totally broken.  
 When turning on the IC, apply  $V_{DD}$  first. Then apply  $V_{EE}$ ,  $V_{GG}$ , and the logic signal after  $V_{DD}$  has risen to 90% of the set value.  
 The  $V_{GG}$  input,  $V_{EE}$  input, and logic signal input can be turned on in any order, provided that the following conditions are satisfied for the protection of the  $V_{GG}$  power supply.  
 A) The IC is in normal operation at the rising edge of  $V_{GG}$  (i.e., the  $V_{GG}$  output is selected for only a single output) or all the outputs are in  $V_{EE}$  output condition.  
 B) All the inputs are not open and are grounded by a low impedance path until each power supply and the logic signal rise.



- Note 6) Activate the OEV, however, if the  $V_{DD}$ ,  $V_{EE}$ , and  $V_{GG}$  power supplies are turned on simultaneously.



**B. OPERATING CONDITIONS**

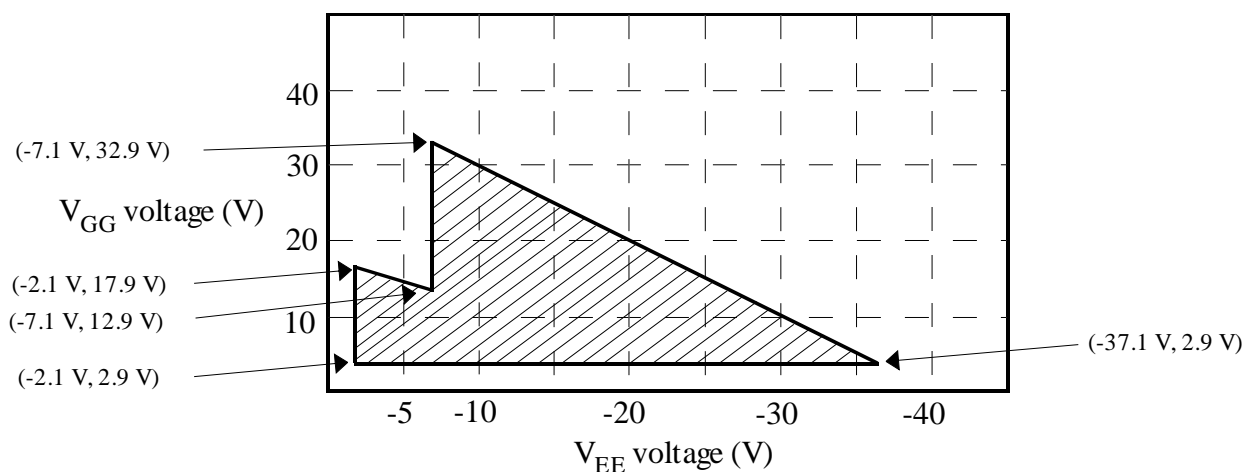
$T_a = -20^{\circ}\text{C}$  to  $+75^{\circ}\text{C}$   $V_{SS} = 0\text{ V}$

Parameter	Symbol	Condi-tions	Rating			Unit
			Min	Typ	Max	
B1	Operating supply voltage 1	$V_{DD}$	2.6	2.9	3.6	V
B2	Operating supply voltage 2	$V_{GG}-V_{EE}$	10		40	V
B3	Operating supply voltage 3	$V_{GG}$	$V_{DD}$		$V_{EE}+40$	V
B4	Operating supply voltage 4	$V_{EE}$	$V_{GG}-40$		$V_{DD}-10$	V

\* The delay time of driving output is not guaranteed in the following conditions.

Symbol	Rating			Unit
	Min	Typ	Max	
$V_{DD}$	2.6	2.9	3.6	V
$V_{GG}$	$V_{DD}$		$V_{EE}+20$	V
$V_{EE}$	$V_{GG}-10$		$V_{DD}-5$	V

Operating voltage range of  $V_{EE}$  and  $V_{GG}$  when  $V_{DD} = 2.9\text{ V}$



- The values specified in the *Product Standards* are guaranteed on condition that the IC is applied to the manufacturer's standard packages.

### C. DC CHARACTERISTICS

#### (1) DC Characteristics

 $T_a = 25^\circ\text{C}$   $V_{SS} = 0\text{ V}$ 

Parameter	Symbol	Conditions	Rating			Unit	
			Min	Typ	Max		
C1	Operating supply current ( $V_{DD}$ )	$I_{DD}$	$f_{FX} = 20.0\text{ kHz}$ $V_{DD} = 3.3\text{ V}$ $V_{EE} = -15\text{ V}$ $V_{GG} = 15\text{ V}$ No-load output			50	$\mu\text{A}$
C2	Operating supply current ( $V_{GG}$ )	$I_{GG}$				300	$\mu\text{A}$
C3	Quiescent supply current ( $V_{DD}$ )	$I_{DS}$	In standby mode, $V_{DD} = 3.3\text{ V}$ $V_{EE} = -15\text{ V}$ $V_{GG} = 15\text{ V}$			10	$\mu\text{A}$
C4	Quiescent supply current ( $V_{GG}$ )	$I_{GS}$				10	$\mu\text{A}$

 $T_a = 25^\circ\text{C}$   $V_{SS} = 0\text{ V}$ 

Parameter	Symbol	Condi- tions	Rating			Unit	
			Min	Typ	Max		
1) Input pins (RL, FX, OEV, OEVSEL, MODE)							
C5	High-level input voltage	$V_{IH1}$		$0.8 \times 1.65$		$V_{DD}$	V
C6	Low-level input voltage	$V_{IL1}$		0		$0.2 \times 1.65$	V
C7	Input leakage current	$I_{LI1}$		-10		10	$\mu\text{A}$
2) I/O pins (STVD, STVU)							
C8	High-level input voltage	$V_{IH3}$		$0.8 \times 1.65$		$V_{DD}$	V
C9	Low-level input voltage	$V_{IL3}$		0		$0.2 \times 1.65$	V
C10	High-level output voltage	$V_{OH}$	-100 $\mu\text{A}$	$V_{DD} - 0.4$			V
C11	Low-level output voltage	$V_{OL}$	100 $\mu\text{A}$			0.4	V

- The values specified in the *Product Standards* are guaranteed on condition that the IC is applied to the manufacturer's standard packages.

$T_a = 25\text{ }^\circ\text{C}$   $V_{SS} = 0\text{ V}$ 

Parameter	Symbol	Conditions	Rating			Unit	
			Min	Typ	Max		
3) LCD drive output pins (X1 to X244)							
C12	Output leakage current	$V_{LO1}$		-50		50	$\mu\text{A}$
C13	Output ON-state resistance	$R_{ON-V_{GG}}$	$V_{GG}=15\text{ V}$ $V_{EE}=-15\text{ V}$ $V_{OM}=V_{GG}-0.5\text{ V}$ $V_{OM}$ is the voltage that is applied to X1 to X244 pins.		600	1000	$\Omega$
		$R_{ON-V_{OFF}}$	$V_{GG}=15\text{ V}$ $V_{EE}=-15\text{ V}$ $V_{OM}=V_{EE}+0.5\text{ V}$ $V_{OM}$ is the voltage that is applied to X1 to X244 pins.		400	1000	$\Omega$
4) Through wiring (COM1 to COM4)							
C14	wiring resistance	$R_{com}$				10	$\Omega$

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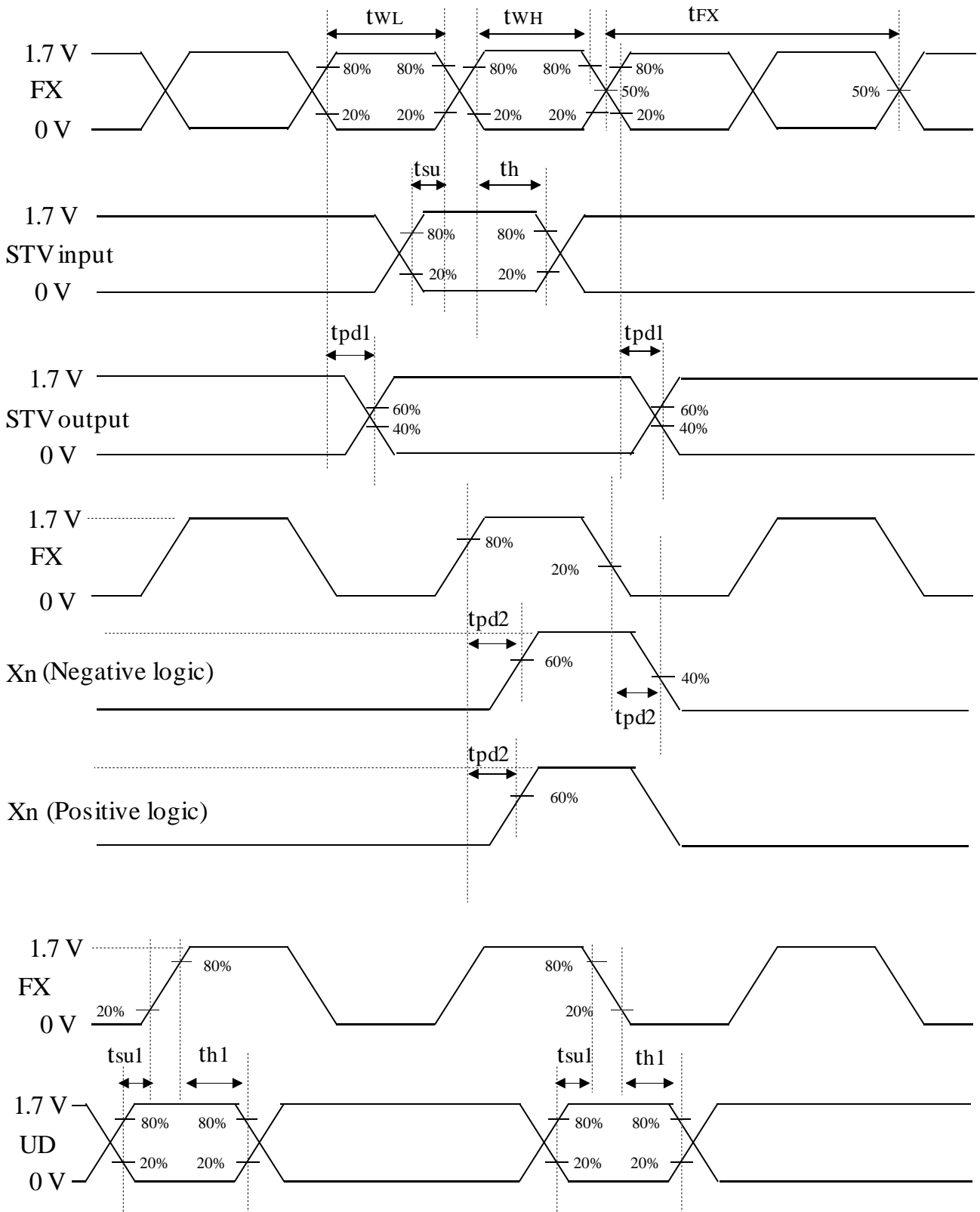
## (2) AC Characteristics

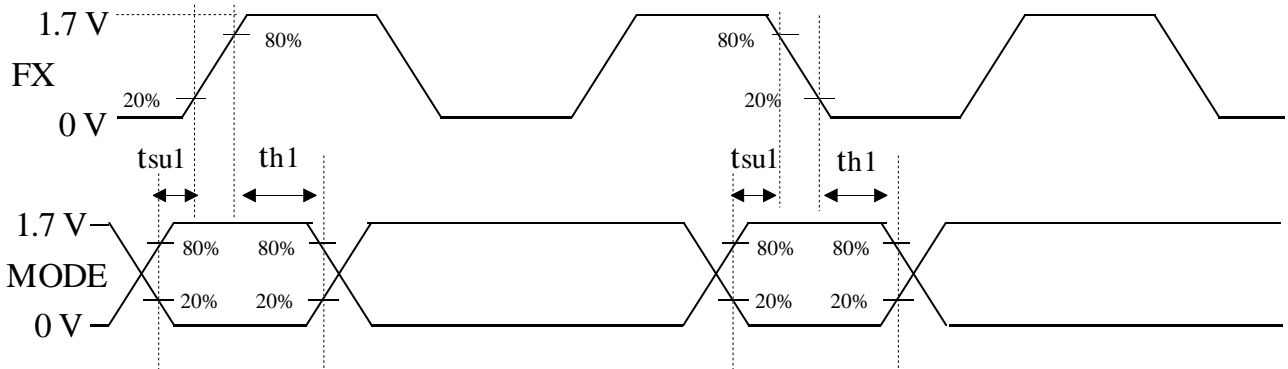
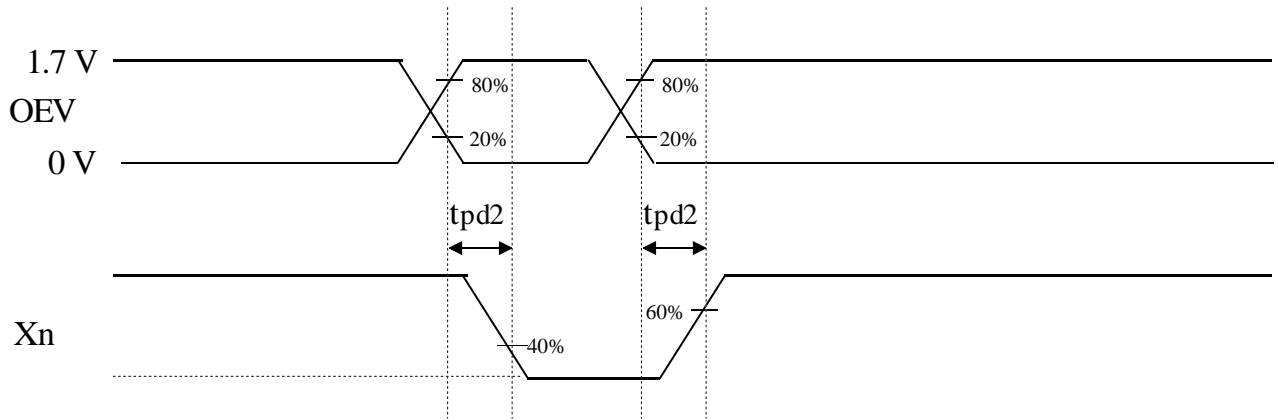
$T_a = 25^\circ\text{C}$   $V_{SS} = 0\text{ V}$

Parameter		Symbol	Conditions	Rating			Unit
				Min	Typ	Max	
C15	Clock cycle	$t_{FX}$		2			$\mu\text{s}$
C16	Clock high-level pulse width	$t_{WH}$		500			ns
C17	Clock low-level pulse width	$t_{WL}$		500			ns
C18	STV data setup time	$t_{su}$		100			ns
C19	STV data hold time	$t_h$		300			ns
C20	UD setup time	$t_{su1}$		100			ns
C21	UD hold time	$t_{h1}$		300			ns
C22	MODE setup time	$t_{su1}$		300			ns
C23	MODE hold time	$t_{h1}$		300			ns
C24	STV output delay time	$t_{pd1}$	$C_L = 50\text{ pF}$			350	ns
C25	Xn output delay time	$t_{pd2}$	$C_L = 500\text{ pF}$			1	$\mu\text{s}$

- The values specified in the *Product Standards* are guaranteed on condition that the IC is applied to the manufacturer's standard packages.

AC Characteristics Timing Chart





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