

RAA207700GBM/7701GBM/7702GBM

Synchronous Buck Regulator with Internal Power MOSFETs

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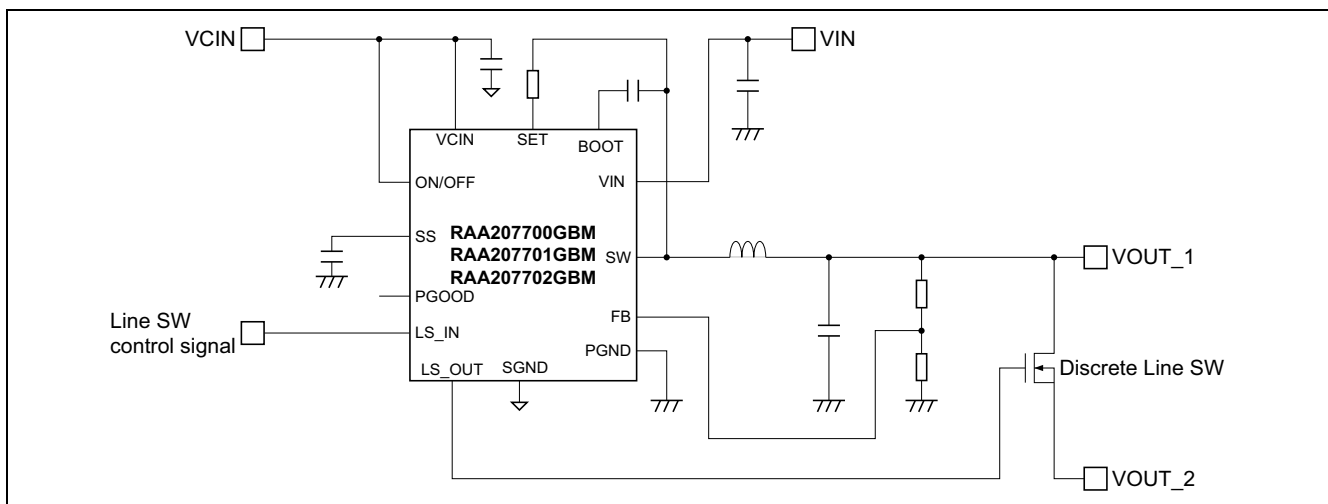
Description

The RAA207700GBM is monolithic synchronous buck regulator with power MOSFETs in extremely small package. The RAA207700GBM delivers high output current by small $R_{ds(on)}$ Power MOSFETs. Constant on time control architecture provides fast transient response, and minimize external components. The RAA207700GBM operates skip mode at light load, it provides high efficiency in all load condition. Three current ability products can be selected.

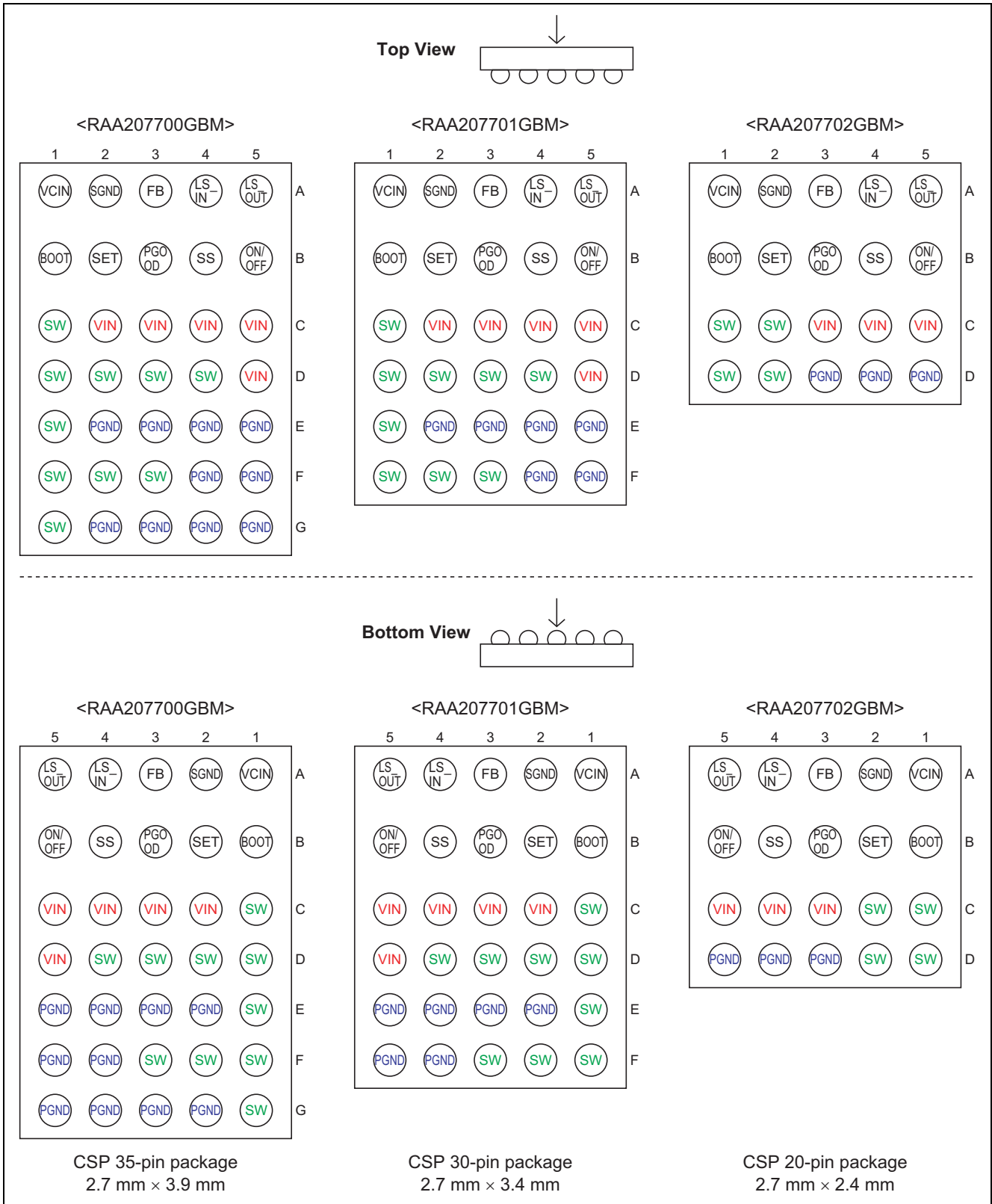
Features

- Wide input voltage range: 3 V to 16 V
- Constant-On-Time control
- Built-in power MOSFETs suitable for PC, Server application
- Very low stand-by current: 0.1 μ A (typ.)
- Very low quiescent current :320 μ A (typ. at no load)
- Switching frequency: Adjustable up to 2 MHz
- High average output current, up to 15 A (7700GBM), 10 A (7701GBM), 5 A (7702GBM)
- Controllable driver: Remote on/off
- Power Good function
- Over current protection/Over voltage protection/Thermal shutdown function
- Built-in bootstrapping diode
- Soft Start period adjustable
- Enhanced light load mode function for higher efficiency
- High drivability built-in line switch driver for low-loss line switch driving
- Extremely small chip size package with solder bump
- Pb-Free/Halogen-Free

Application Circuit



Pin Arrangement

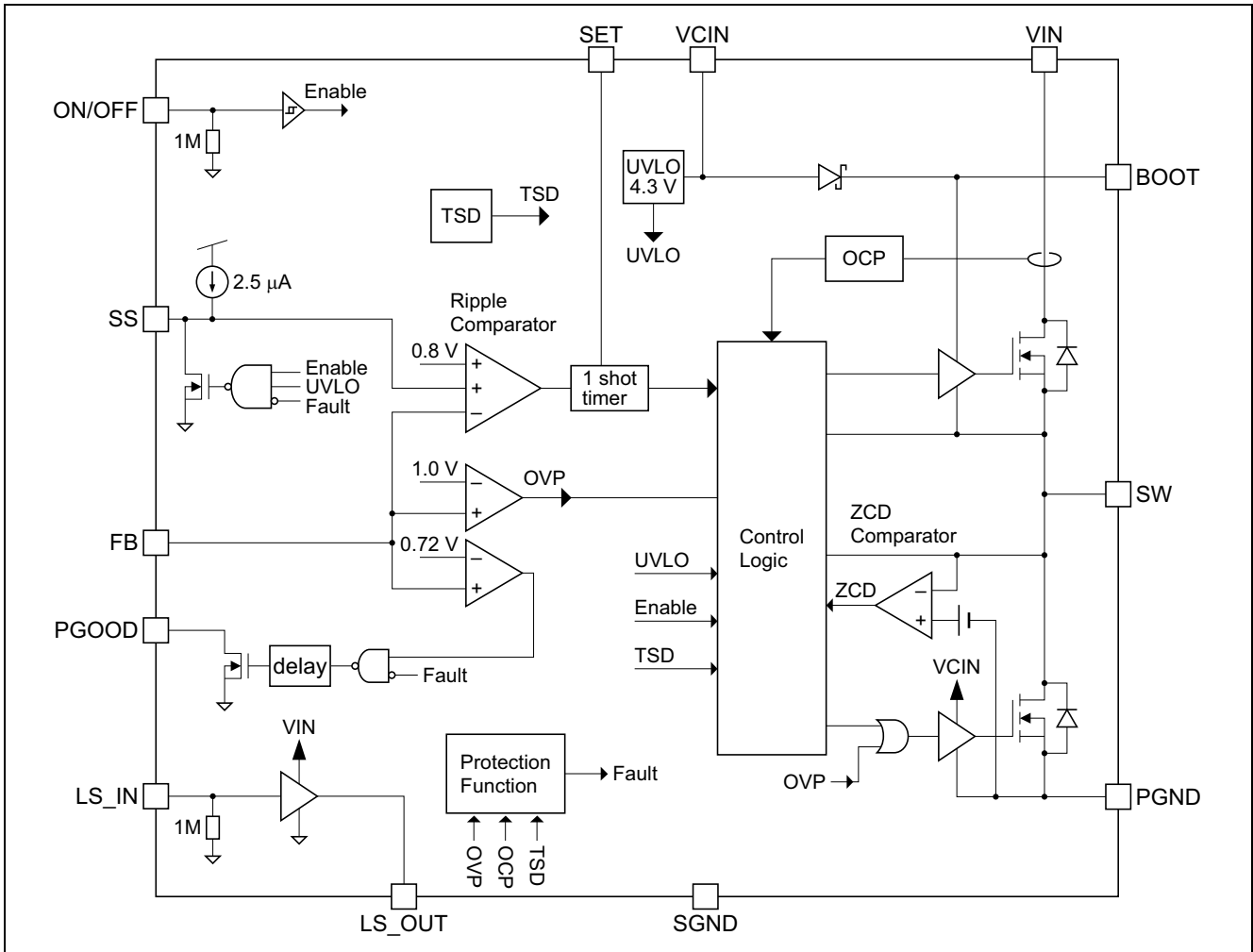


Pin Description

Pin Name	Pin No.	Description	Remarks
VCIN	1A	Controller input voltage (+5 V input)	Controller supply input
SGND	2A	Controller analog GND	Should be connected to PGND on PCB pattern
FB	3A	Feedback voltage input pin	
LS_IN	4A	Line SW driver control pin	
LS_OUT	5A	Line SW driver output pin	
BOOT	1B	Bootstrap voltage pin	To be supplied +5 V through integrated SBD
SET	2B	Constant on time program pin	Tie resistor between SW and SET
PGOOD	3B	Power good indicator pin	Pull low when No Good (open drain output)
SS	4B	Soft start period program pin	Tie capacitor between SS and SGND
ON/OFF	5B	Operation enable pin	Operation stop when L signal asserted
VIN	—	Input voltage	
SW	—	Switching node	
PGND	—	Power ground	Should be connected to SGND on PCB pattern

Note: Pin assign of 1A-5A & 1B-5B is common through RAA207700GBM, RAA207701GBM and RAA207702GBM.

Block Diagram



1. Truth table for the ON/OFF pin

ON/OFF Input	Driver Chip Status
"L"	Shutdown (operation STOP)
"Open"	Shutdown (operation STOP)
"H"	Enable (Normal operation)

2. Truth table for Line Switch driver

LS_IN Input	LS_OUT Status
"L"	GND
"Open"	GND
"H"	VIN

Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Ratings	Unit	Notes
Input voltage	VIN	-0.3 to +20	V	1
Switch node voltage	SW	20(DC), 23(<10 ns)	V	1
BOOT voltage	VBOOT	25(DC), 28(<10 ns)	V	1, 2
Controller voltage	VCIN	-0.3 to +6	V	1
Input pin voltage (FB, LS_IN)	V _{INPUT}	-0.3 to VCIN +0.3	V	1, 3
ON/OFF voltage	V _{ON/OFF}	-0.3 to VIN	V	1
SET voltage	V _{SET}	-0.3 to VIN	V	1
PGOOD voltage	V _{PGOOD}	-0.3 to VIN	V	1
PGOOD sink current	I _{PGOOD}	+2	mA	4
Operating junction temperature	T _{j-opr}	-40 to +125	°C	
Storage temperature	T _{stg}	-55 to +150	°C	

Notes: 1. Rated voltages are relative to voltages on the SGND and PGND pins.

2. BOOT – VCIN < 20 V

3. VCIN + 0.3 V < 6 V

4. For rated current, (+) indicates inflow to the chip.

Recommended Operating Condition

Item	Symbol	Ratings	Unit	Remarks
Input voltage	VIN	3 to 16	V	
Controller voltage	VCIN	4.5 to 5.5	V	
Continuous output current	I _{OUT}	0 to 15 0 to 10 0 to 5	A	15 A: RAA207700GBM 10 A: RAA207701GBM 5 A: RAA207702GBM

Electrical Characteristics

(Ta = 25°C, VCIN = 5 V, VIN = 12 V, SW = 0 V, unless otherwise specified)

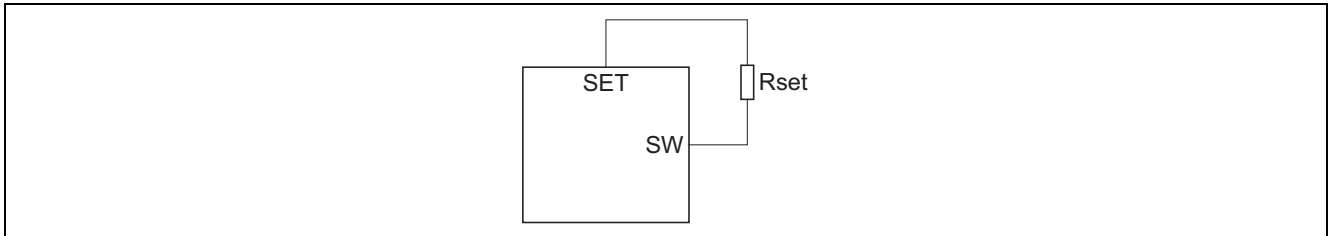
Item	Symbol	Min	Typ	Max	Unit	Test Conditions	
Supply	VCIN start threshold	VH	—	4.3	4.5	V	
	VCIN shutdown threshold in CCM	VL	3.6	3.8	—	V	
	VCIN shutdown threshold in ELL mode	V _{LCCM}	—	3.0	3.6	V	In ELL mode (DCM, f _{sw} < 100 kHz)
	VCIN operating current (RAA207700GBM)	I _{CIN}	—	40	—	mA	f _{sw} = 1 MHz, Ton = 200 ns
	VCIN operating current (RAA207701GBM)	I _{CIN}	—	35	—	mA	
	VCIN operating current (RAA207702GBM)	I _{CIN}	—	20	—	mA	
	VCIN quiescent current	I _q	—	320	400	μA	Output = no load, ELL mode
	VCIN disable current	I _{CIN-DISBL}	—	0.1	5	μA	ON/OFF = 0 V, LS_IN = 0 V
	VIN disable current	I _{IN-DISBL}	—	0.1	5	μA	ON/OFF = 0 V, LS_IN = 0 V
Remote on/off	Disable level	V _{DISBL}	—	—	0.6	V	3.3 / 5.0 V interface
	Enable level	V _{ENBL}	2.0	—	—	V	3.3 / 5.0 V interface
	Pull-down resistance	R _{DISBL}	0.7	1	1.3	MΩ	ON/OFF = 1 V
Line_SW input	Line SW off level	V _{LSIN_OFF}	—	—	0.6	V	3.3 / 5.0 V interface
	Line SW on level	V _{LSIN_ON}	2.0	—	—	V	3.3 / 5.0 V interface
	Pull-down resistance	R _{LS_IN}	0.7	1	1.3	MΩ	LS_IN = 1 V
Line_SW output	Line SW on output voltage	V _{LSW_ON}	VIN-0.5	VIN	—	V	LS_IN = 5 V
	Line SW off output voltage	V _{LSW_OFF}	—	—	0.1	V	LS_IN = 0 V
	Line SW on source current	I _{LSW_SOURCE}	—	25	—	mA	VIN = 12 V, LS_IN = 5 V
	Line SW off sink current	I _{LSW_SINK}	—	25	—	mA	VIN = 12 V, LS_IN = 0 V
	Line SW on propagation delay	T _{PLSWON}	—	300	—	ns	LSIN to LSOUT rising
	Line SW off propagation delay	T _{PLSWOFF}	—	300	—	ns	LSIN to LSOUT falling
	Line SW drive current of VIN	I _{IN-LS}	—	8	20	μA	LS_IN = 5 V
FB	Comparator threshold voltage	V _{FB_COMP}	792	800	808	mV	
	FB input current	I _{FB_IN}	-0.1	0	+0.1	μA	FB = 1 V
Power good indicator	Rising threshold on FB	V _{PG_rise}	0.67	0.72	0.77	V	
	Power good hysteresis	dV _{PG}	—	50	—	mV	
	Power good resistance	R _{PG}	0.25	0.5	1	kΩ	FB = 0 V
Soft start	Soft start bias current	I _{SS}	1.8	2.5	3.2	μA	
Over voltage protection	OVP trip voltage on FB	V _{OVP}	0.95	1.00	1.05	V	
Over current protection	OCP trip current (RAA207700GBM)	I _{OCP}	16.0	20.0	24.0	A	Fixed internally *1
	OCP trip current (RAA207701GBM)	I _{OCP}	12.0	15.0	18.0	A	Fixed internally *1
	OCP trip current (RAA207702GBM)	I _{OCP}	6.4	8.0	9.6	A	Fixed internally *1
Over temperature protection	TSD trip temperature	T _{TSD}	130	150	—	°C	*1
	Temperature hysteresis	T _{hys}	—	30	—	°C	*1

Note: *1 Not directly tested. Assured by related characteristics test.

Description of Operation

The RAA207700GBM operates as voltage-ripple based constant on time control architecture. Converter output is controlled by output voltage ripple which is determined by inductor ripple current and ESR & ESL of output capacitor. Each switching cycle starts High-side MOSFET turn on which time is decided by 1 shot timer. After High-side MOSFET turns off, Low side turns on, and it keeps until FB voltage becomes lower than reference voltage. In light load condition, Low-side MOSFET on time is decided by inductor zero current.

Switching Frequency, Constant on Time Setting



Switching Frequency in CCM mode is determined by following equation.

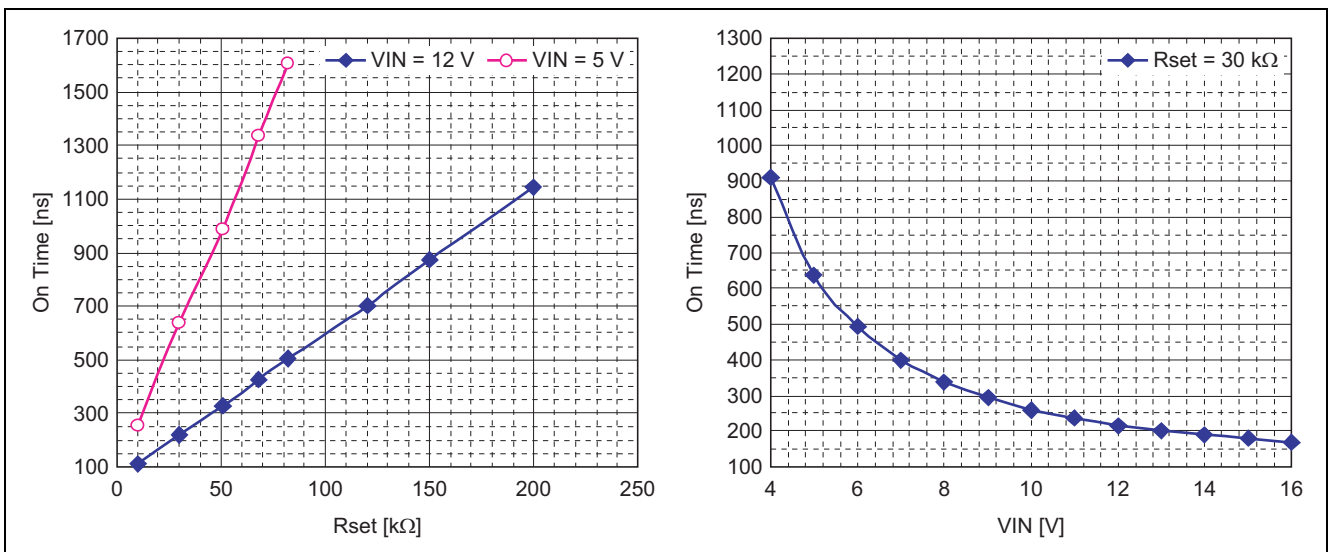
$$\text{Switching Frequency: } (V_{out}/V_{in}) \cdot (1/t_{on}) \text{ [Hz]}$$

Here, t_{on} is High-side MOS on time, and it is determined by following equation.

$$\text{On time pulse: } (50 \text{ pF} \cdot 1 \text{ V} / V_{in} - 2.0 \text{ V}) \cdot R_{set} + 50 \text{ ns [s]}$$

From above equation, constant on time is change depend on V_{in} , so switching frequency is almost constant when V_{IN} change. This architecture is suitable for battery application. From the above equation, R_{set} is calculated by

$$R_{set: } (V_{out} / (V_{in} \cdot F_{sw}) - 50 \text{ ns}) \cdot (V_{in} - 2.0 \text{ V}) / (50 \text{ pF} \cdot 1 \text{ V}) \text{ [}\Omega\text{]}$$



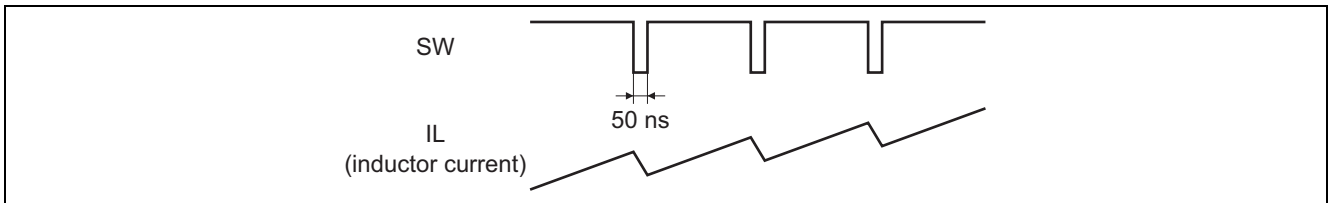
Maximum Duty Cycle Operation

Maximum duty cycle is restricted by following equation.

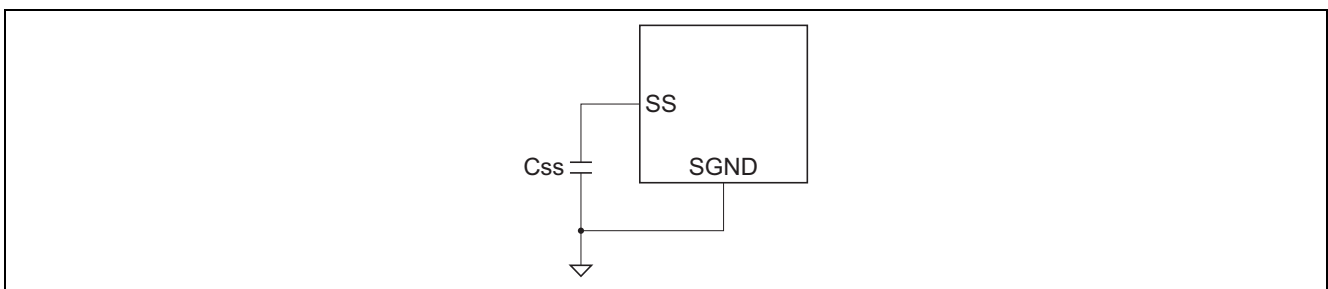
$$\text{Max. duty: } 1 - (50 \text{ ns} \cdot F_{sw})$$

Here, F_{sw} is switching frequency.

If FB voltage does not reach reference voltage after the High-side MOSFET turn on time is expired, Low-side MOSFET turns on 50 ns, and next switching cycle starts. Especially, this condition occurs when output load transient state.



Soft Start



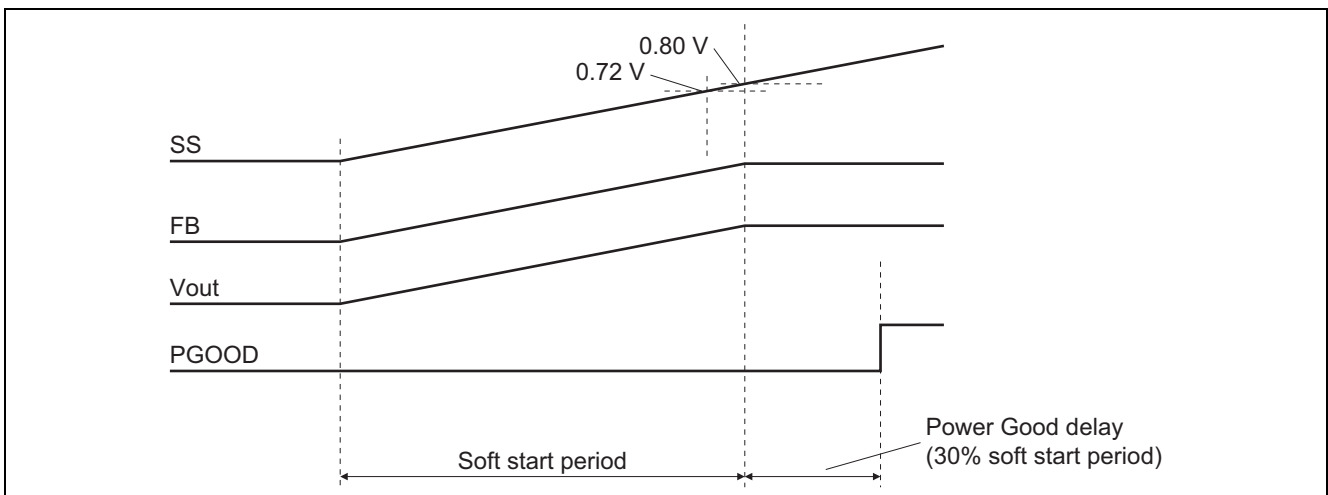
Soft start ramp period is adjustable by external capacitor (C_{ss}) selection. When converter start operating, $2 \mu\text{A}$ current from SS pin charges capacitor between SS and GND. Soft start period is determined by following equation.

$$\text{Soft Start period: } C_{ss} \cdot 0.8 \text{ V} / 2.5 \mu\text{A [s]}$$

Here, 0.8 V is internal reference voltage V_{ref} . IC operates diode emulation mode at Soft start period, so it can prevent from reverse current when pre-bias condition. Soft start restarts when Enable signal re-entered, and after OCP, OVP, TSD, UVL release condition.

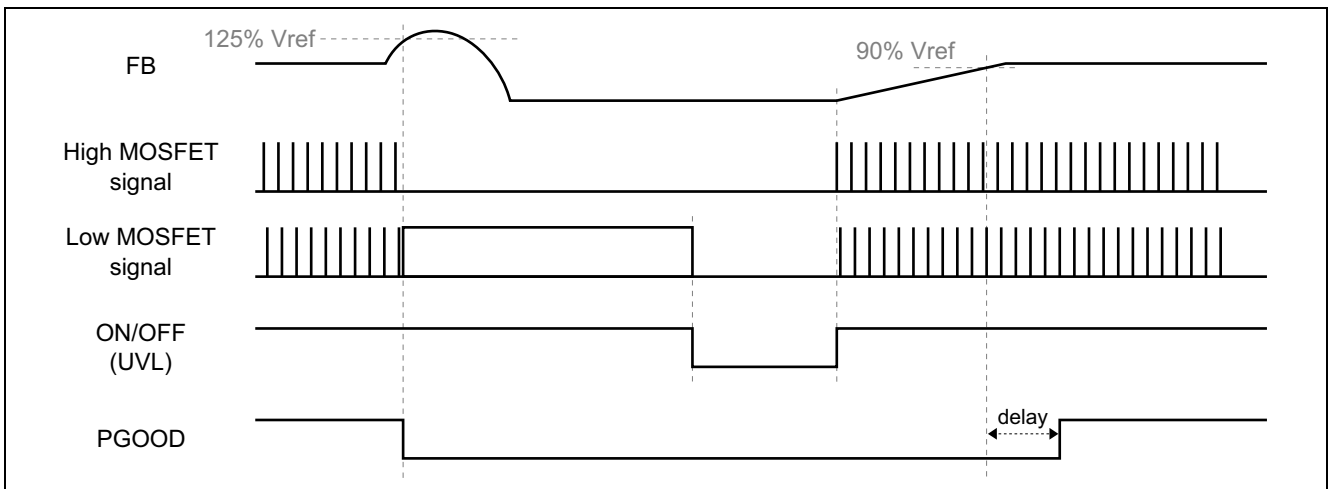
Power Good Indicator

Power good indicator is useful for controlling multi-converter systems for sequential start up and shut down. FB voltage is monitored continuously by power good comparator. The power good comparator compares FB pin and 90% internal reference voltage (0.72 V). When FB reaches reference voltage, PGOOD pin becomes high impedance after internal delay (30% of soft start period). Under the fault condition (UVLO, OVP, OCP, TSD), PGOOD pin is pulled low.



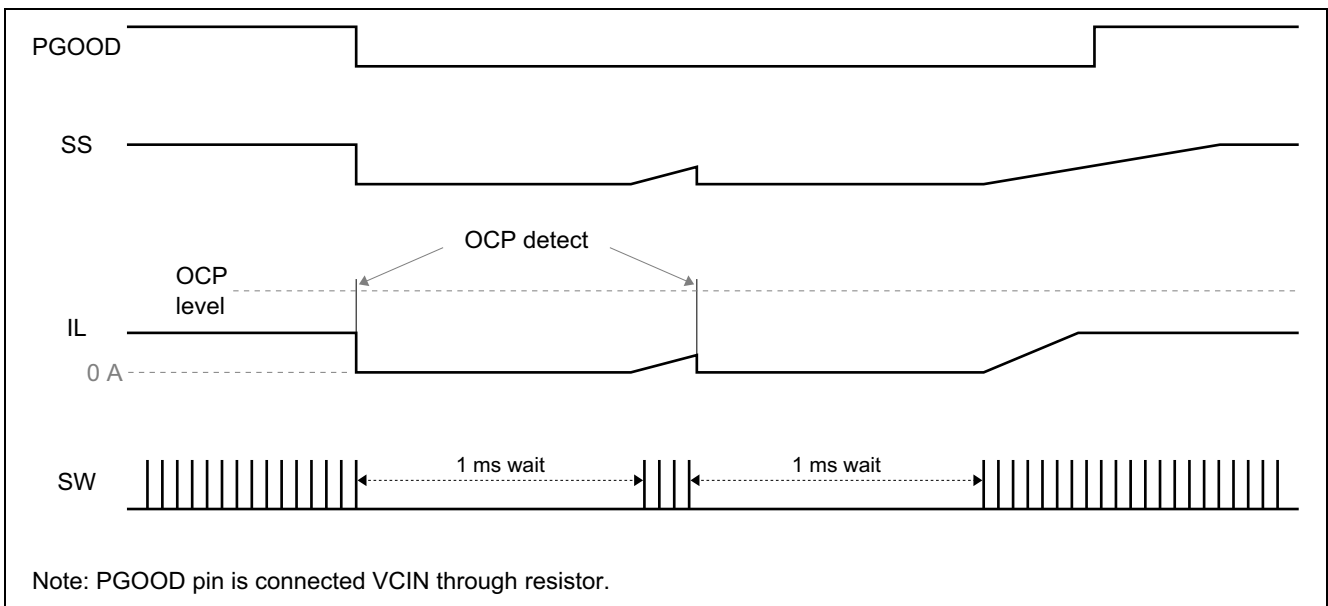
Over Voltage Protection (OVP)

When FB voltage exceeds 125% of reference voltage (1.00 V), switching stops immediately and latched Low-side MOSFET on state in order to pull the output voltage. To leave the OVP condition, VCIN needs to be pulled under the UVLO level, and re-enter the signal.



Over Current Protection (OCP)

OCP detection circuit monitors high-side MOSFET drain-source current. When the current exceeds fixed level eight time, IC starts hiccup operation. In the hiccup operation, switching stops and operate 1 ms timer. After 1 ms timer is expired, IC operates again from soft start state. If IC detect OCP in the soft start circuit, hiccup operation start again.



Thermal Shutdown (TSD)

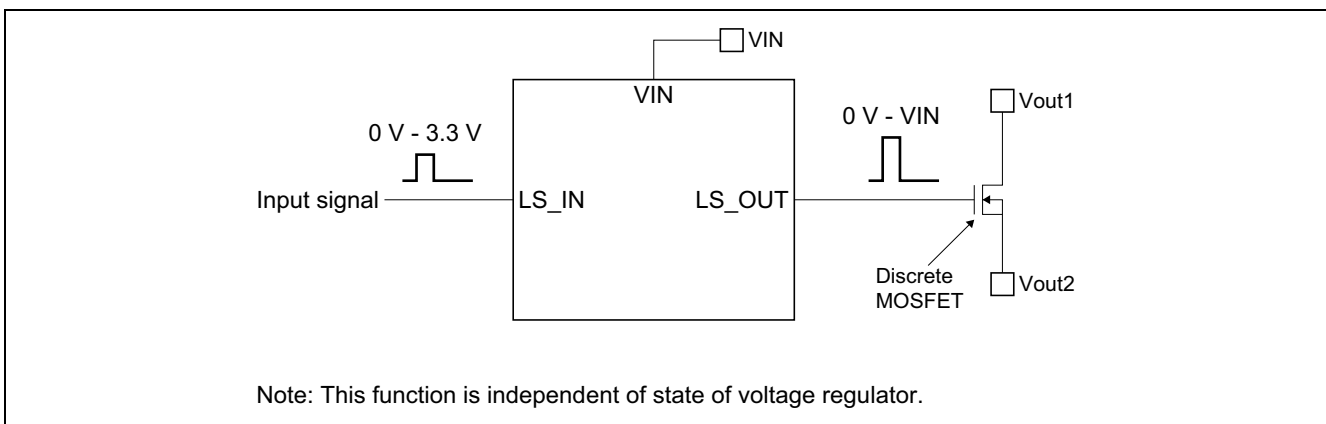
Thermal sensor monitors junction temperature of IC. When junction temperature exceeds 150°C, switching stops. After junction temperature become 125°C, IC restart switching from soft start (Non-latched function).

Enhanced Light Load Function (ELL)

IC operates diode emulation mode in light load condition. To enhance light load efficiency, IC detects light load condition automatically, and operate as Enhanced Light Load mode (ELL). In ELL mode, bias current of IC becomes small, so this function can improve the efficiency.

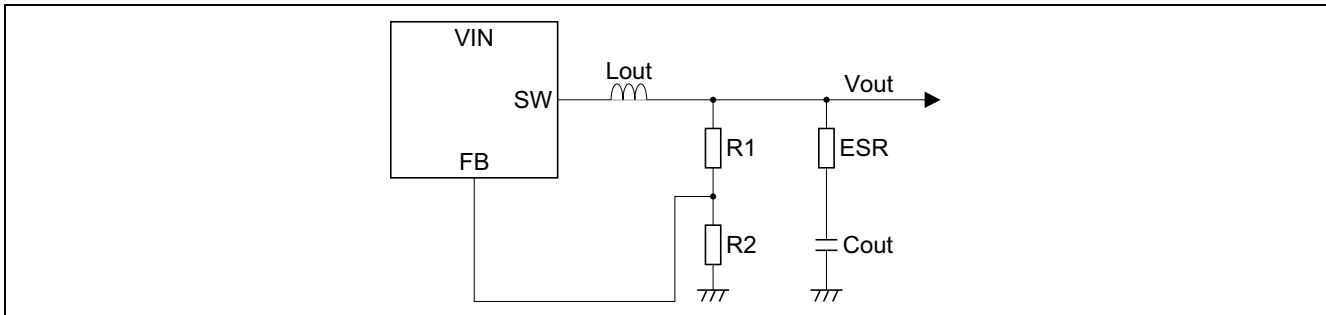
Line Switch Driver

The RAA207700GBM/7701GBM/7702GBM incorporates high drivability built in line switch driver. The line switch driver can drives large gate capacitance MOSFET with low power consumption. (Typical 8 μA at Vin = 12 V)
Line switch driver operates independent of voltage regulator’s state.



Stability Criteria, Output Voltage Setting for High ESR Output Capacitor

Small output ripple voltage makes control loop unstable in constant on time architecture. Ripple voltage needs to be larger than 15 mV on FB pin. When using high ESR (>50 mΩ) capacitor such as Electrolytic capacitor, Polymer aluminum capacitor for output capacitor, ripple voltage on FB pin will be more than 15 mV.



Stability criteria

From loop stability analysis, constant on time control system must satisfy below equation.

$$\text{Stability criteria: } ESR \cdot C_{out} > t_{on} / 2$$

Here, t_{on} is constant on time. If the system cannot satisfy above equation, subharmonic oscillation will occur.

Vout setting

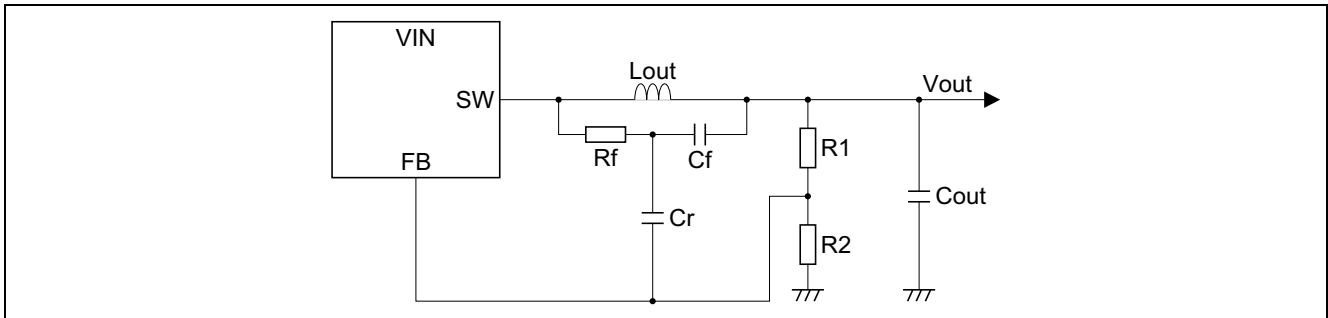
FB comparator compares FB voltage and internal accurate reference voltage (0.8 V). Feedback loop controls FB voltage to match the reference voltage. Therefore, output voltage is set by following equation.

$$V_{out}: 0.8 \text{ V} \cdot (R1+R2) / R2$$

Here, R1 and R2 is output voltage divider resistor (refer to above figure). However, ripple voltage on FB pin affects FB voltage, so Vout slightly shifts from setting value. If the system needs high accuracy, adjust Vout by changing R1, R2 value.

Operating with Small ESR Output Capacitor

When using low-ESR output capacitor like MLCC, voltage ripple on output voltage node is very small. So voltage ripple needs to be enhanced by additional components. Recommended ripple enhance method is like below figure.



Ripple injection on FB pin

R_f and C_f make ripple voltage using inductor DCR ripple. C_r is used for AC ripple injection to FB pin. Ripple voltage between R_f and C_f is described by following equation.

$$V_{\text{ripple}}: (V_{\text{IN}} - V_{\text{OUT}}) \cdot t_{\text{on}} / (R_f \cdot C_f)$$

Make sure above ripple voltage is larger than 15 mV.

Stability criteria

From loop stability analysis of above circuit configuration, the system must satisfy below equation.

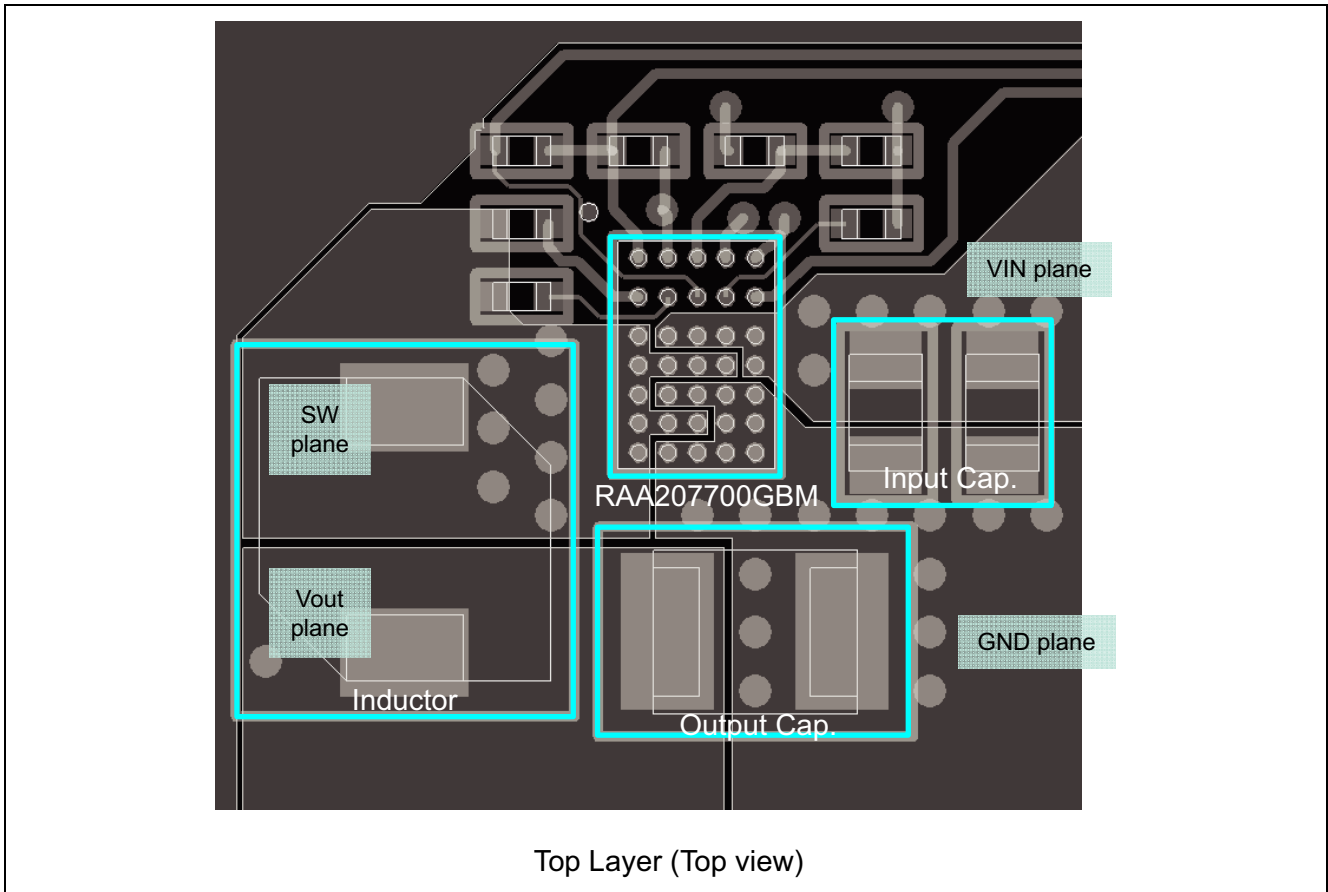
$$\text{Stability criteria: } L_{\text{out}} \cdot C_{\text{out}} / (R_f \cdot C_f) > t_{\text{on}} / 2$$

If the system cannot satisfy above equation, subharmonic oscillation will occur.

Vout setting

Output voltage setting is basically same concept as high ESR capacitor use case. Ripple voltage from injection circuit affects FB voltage, so it need to be adjust R_1 , R_2 for high accuracy system.

Board Layout Example (RAA207700GBM)



Representative Inductors

Maker	Inductance [μ H]	$\Delta L/L_0 = 20\%$ Change [A]	Dimensions [mm]
NEC Tokin MPC series	0.42	20.0	6.7 × 8.0 × 4.0
	0.60	19.0	6.7 × 8.0 × 5.0
	0.88	24.0	10.0 × 11.5 × 4.0
	1.0	25.0	10.0 × 11.7 × 5.5
ALPS Green Device GLMC series	0.47	13.9 * ¹	6.5 × 7.4 × 3.0
	1.0	10 * ¹	6.5 × 7.4 × 3.0
	1.5	8.8 * ¹	6.5 × 7.4 × 3.0
TOKO FDVE0630 series	0.33	15.9	6.7 × 7.4 × 3.0
	0.47	15.6	6.7 × 7.4 × 3.0
	0.75	10.9	6.7 × 7.4 × 3.0
	1.0	9.5	6.7 × 7.4 × 3.0
TDK SPM5030 series	0.35	14.9	5.0 × 5.2 × 3.0
	0.47	11.0	5.0 × 5.2 × 3.0
	0.75	9.7	5.0 × 5.2 × 3.0

Note: *¹ 30% change

- Small size inductor for RAA207702GBM

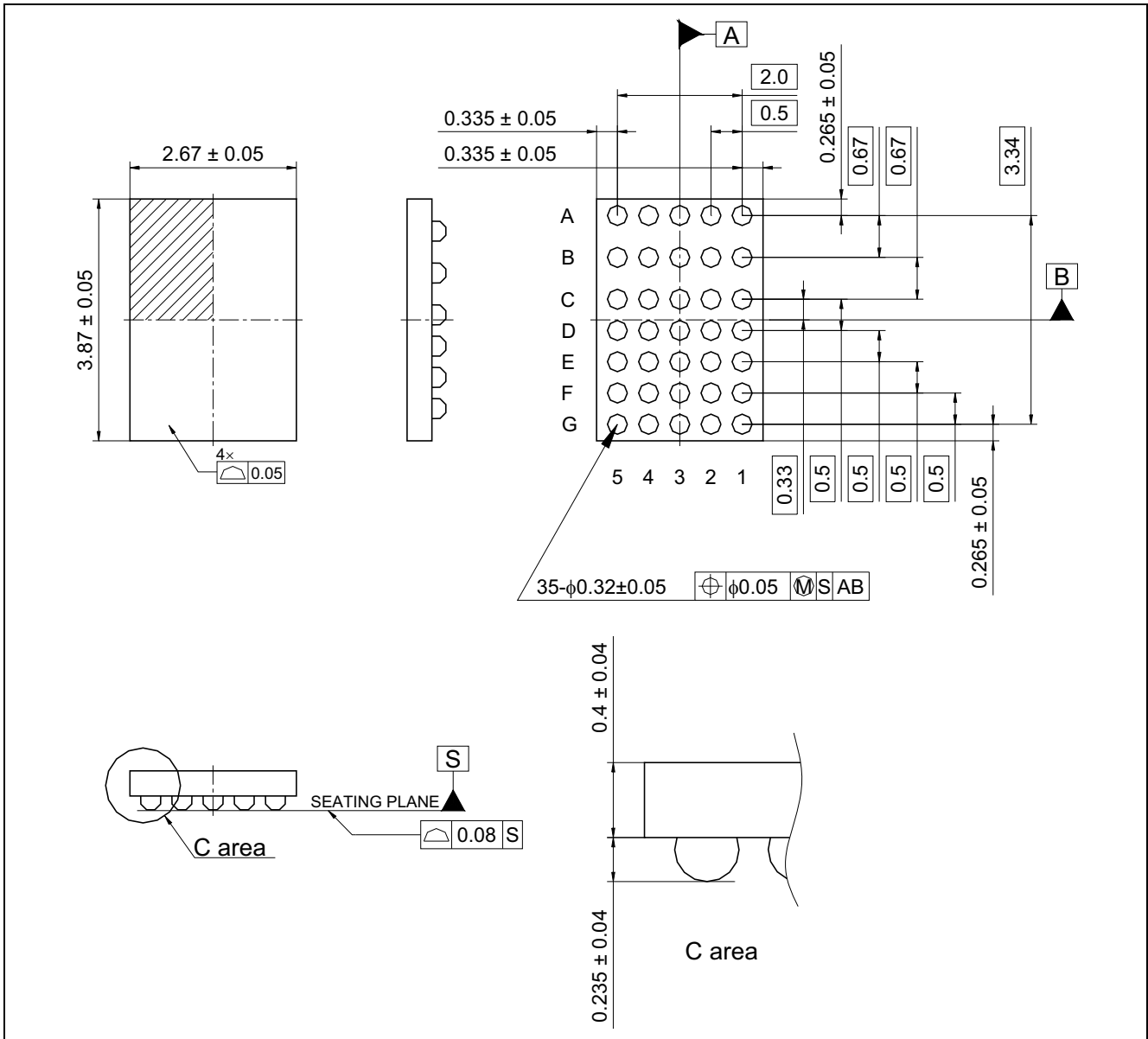
Maker	Inductance [μ H]	$\Delta L/L_0 = 30\%$ Change [A]	Dimensions [mm]
TOKO FDSD0420 series	0.68	8.3	4.2 × 4.2 × 2.0
	1.0	6.8	4.2 × 4.2 × 2.0
	1.5	5.7	4.2 × 4.2 × 2.0
TDK SPM4012 series	0.47	8.3	4.4 × 4.1 × 1.2
	1.0	4.8	4.4 × 4.1 × 1.2

Representative Output Capacitors

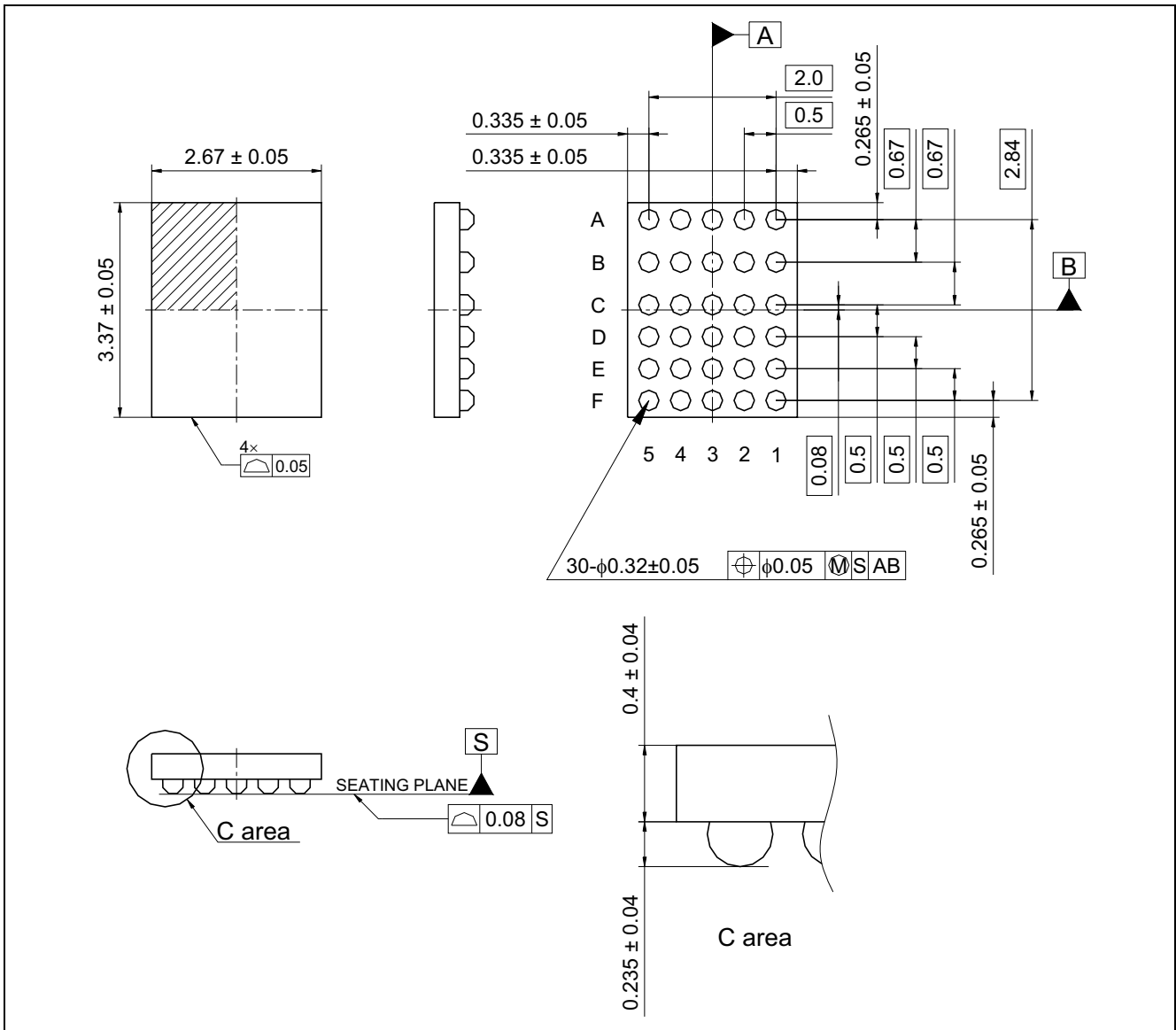
Maker	Maximum Voltage [V]	Capacitance [μ F]
Sanyo POSCAP series	2.0 to 10	47 to 330
Sanyo OS-CON series	2.0 to 10	47 to 330
Murata MLCC series	6.3 to 10	22 to 47
TDK MLCC series	6.3 to 10	22 to 47
TAIYO YUDEN MLCC series	6.3 to 10	22 to 47

Package Dimensions

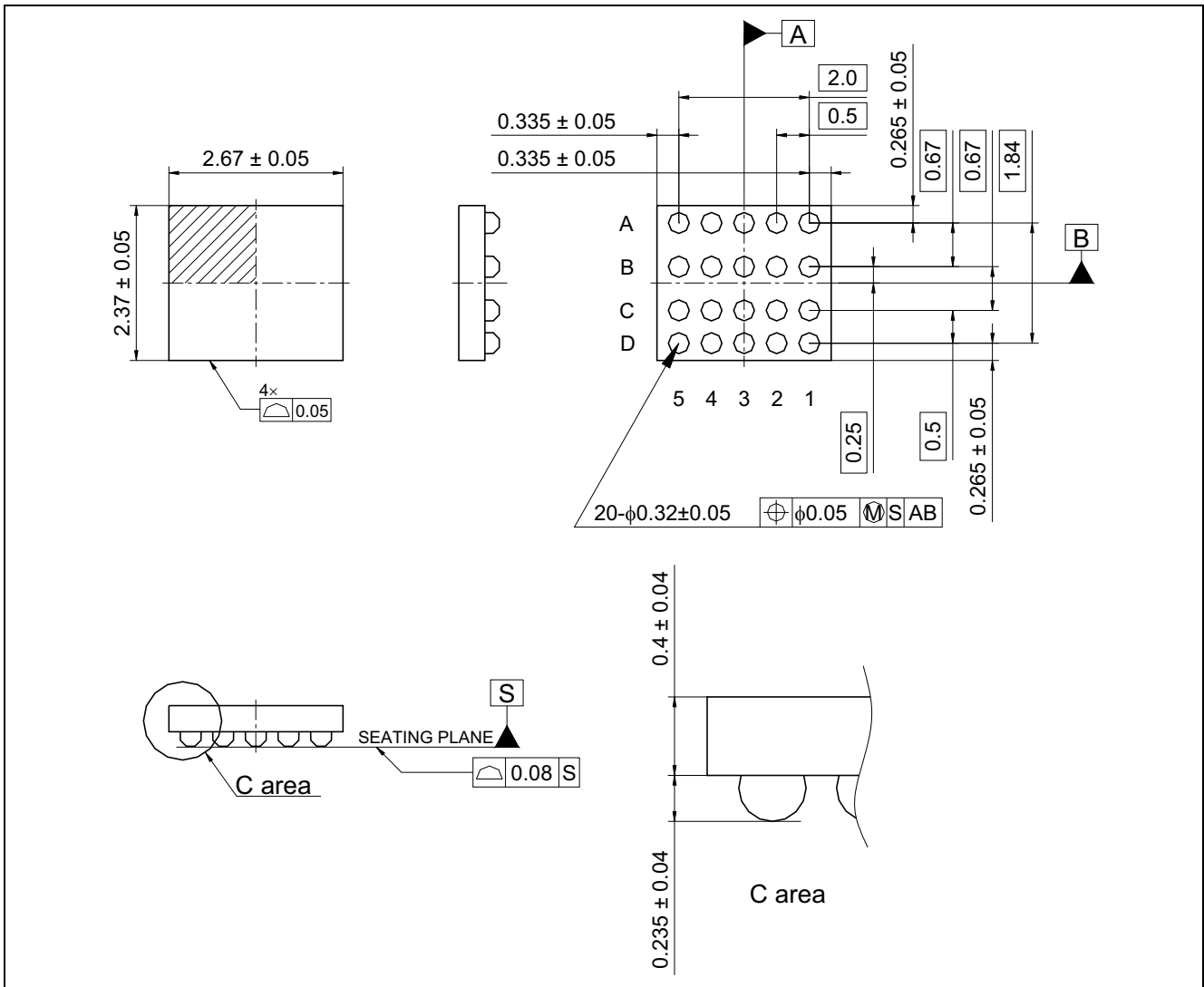
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Tel: +1-408-588-6000, Fax: +1-408-588-6130

Renesas Electronics Canada Limited
1101 Nicholson Road, Newmarket, Ontario L3Y 9C3, Canada
Tel: +1-905-898-5441, Fax: +1-905-898-3220

Renesas Electronics Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K.
Tel: +44-1628-651-700, Fax: +44-1628-651-804

Renesas Electronics Europe GmbH
Arcadiastrasse 10, 40472 Düsseldorf, Germany
Tel: +49-211-65030, Fax: +49-211-6503-1327

Renesas Electronics (China) Co., Ltd.
7th Floor, Quantum Plaza, No.27 ZhiChunLu Haidian District, Beijing 100083, P.R.China
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

Renesas Electronics (Shanghai) Co., Ltd.
Unit 204, 205, AZIA Center, No.1233 Lujiazui Ring Rd., Pudong District, Shanghai 200120, China
Tel: +86-21-5877-1818, Fax: +86-21-6887-7858 / -7898

Renesas Electronics Hong Kong Limited
Unit 1601-1613, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong
Tel: +852-2886-9318, Fax: +852 2886-9022/9044

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Tel: +886-2-8175-9600, Fax: +886 2-8175-9670

Renesas Electronics Singapore Pte. Ltd.
80 Bendemeer Road, Unit #06-02 Hyflux Innovation Centre Singapore 339949
Tel: +65-6213-0200, Fax: +65-6213-0300

Renesas Electronics Malaysia Sdn.Bhd.
Unit 906, Block B, Menara Amcorp, Amcorp Trade Centre, No. 18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: +60-3-7955-3390, Fax: +60-3-7955-9510

Renesas Electronics Korea Co., Ltd.
11F., Samik Laved. or Bldg., 720-2 Yeoksam-Dong, Kangnam-Ku, Seoul 135-080, Korea
Tel: +82-2-558-3737, Fax: +82-2-558-5141