RECONFIGURABLE array STORE (RaS)

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GENERAL DESCRIPTION:

The Reconfigurable array Store (RaS) is an application specific memory chip for the a66xxx family of array processing devices. The RaS can be used to implement data and coefficient RAM's of DaSP/PaC single buffered recursive, I/O buffered recursive, frequency domain filtering and cascaded memory architectures.

The RaS has been optimized for use in 'dual mode' DaSP/PaC system that require memories of 2K complex words or less. For these systems, the RaS provides all of the memory and 'glue' logic reducing the system chip count and board area requirements. The result is a compact, flexible, highly integrated system for FFT-based applications.

Systems which require more that 2K complex words should consider using the a664xx family of memory modules.

The RaS is available in a 144 PGA package at 30MHz and 40MHz in commercial versions; 30MHz in industrial and extended temperature versions; and 30MHz in MIL-883C.

RELATED PRODUCTS:

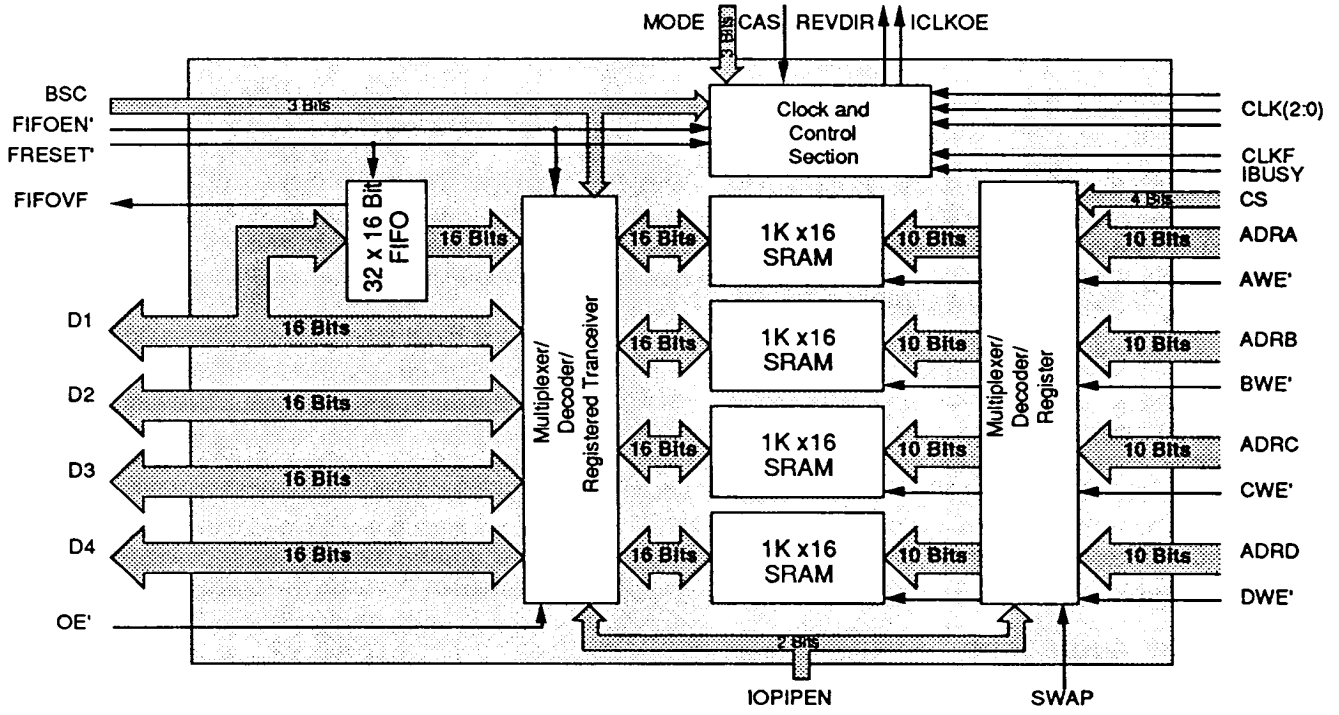
Digital array Signal Processor (DaSP): a66110/111
Programmable array Controller (PaC): a66210/211
DaSP/PaC Memory Modules: a664xx

FEATURES:

- 64K bit RAM configurable as 2x1Kx32, 2x2Kx16, 1x2Kx32, or 4x1Kx16 bit memories
- 32x16 bit FIFO to facilitate operation with real-time input data
- Complete memory and control logic solution for 'dual mode' DaSP / PaC systems under 2K complex words
- Integrated address-based chip selects for memory depths up to 8K
- 144 pin ceramic PGA package
- 3W maximum power dissipation

APPLICATIONS:

- Radar
- Sonar
- EW/ECM
- Digital Radio
- Test Instruments
- Medical Instruments
- Spectrum Analyzers
- Transmultiplexing
- Image Processing
- Image Compression
- Image Reconstruction
- Spread Spectrum Communications



FUNCTIONAL OVERVIEW:

The Reconfigurable array Store (RaS) is an application specific memory chip for DaSP/PaC systems. A detailed functional description of the RaS can be found in the **RaS User's Guide**.

Architecture

As shown in the block diagram on page 1, the core of the RaS chip consists of four quadrants ('quads') of single port 1Kx16 bit memories. The organization of the memory quads is selected via the MODE(2:0) control inputs to be two 1Kx32 bit memories, two 2Kx16 bit memories, one 2Kx32 bit memory, or four 1Kx16 bit memories.

The quads can be internally connected to four 16bit, bidirectional data busses labeled D1, D2, D3, and D4. The data busses are generally connected to the DaSP's D1/D2, D3/D4, or XD1/XD2 busses, or to the user's system-level input and output busses. The data bus connections to the quads are determined by the BSC(2:0) and CAS control inputs.

The addresses to the quads are input via the ADRA, ADRB, ADRC, and ADRD busses along with four write enables AWE', BWE', CWE', DWE' inputs. These busses are generally connected to the PaC's address busses. The internal connections to the quads are determined by the MODE(2:0) and SWAP control inputs.

In certain modes, address bits are compared against the CS(3:0) inputs to generate internal memory 'chip' selects. This feature allows RaS chips to be stacked to form deeper memories without external chip select logic. All addresses and write enables are registered on-chip prior to being fed to the memories.

Three clocks (CLK(2:0)) are provided to clock data in and out of the quads and the input FIFO. These clocks are used internally to register data, addresses, and write enables. The MODE(2:0), CAS, and BSC(2:0) inputs determine how the clocks are assigned inside the chip.

The RaS also contains a 32 word by 16bit FIFO for use in buffering real time input data. The FIFO's input is connected to data bus D1 and can only be used in 16bit RaS memory configurations. Data is clocked into the FIFO via CLK(2) and clocked out of the FIFO via CLKF which is generally connected to the master FIFO clock: ICLKOE. The RaS creates ICLKOE from an internally gated version of CLK(1) based on CAS and BSC(2).

Memory Configurations

The RaS provides seven different memory configurations, each of which is designed with specific applications in mind.

The MODE(2:0) pins determine the RaS memory configuration. These configurations support the construction of the following DaSP/PaC memory architectures:

(1) Single processor, non-I/O buffered, recursive system with coefficient memory and two data memories.
(2) Single processor, I/O buffered, recursive system with coefficient memory and four data memories.
(3) Single processor, I/O buffered, recursive system with coefficient memory, four data memories, and two overlap memories for frequency domain filtering.
(4) Multi-processor, I/O buffered, cascaded / recursive system with coefficient memory.
(5) Multi-processor, I/O buffered, cascaded / recursive system with coefficient memory and two overlap memories.

The architecture supported by each mode is described below:

MODE 0: Two 1Kx32 memories
Used as data memory in 'core' system, or as the inner memory pairs in cascaded systems.

MODE 1: Two 1Kx32 memories
Used as the output memory pair in cascaded systems, or as double buffered coefficient memory.

MODE 2: Four 1Kx16 memories
Used as the real or imaginary data memories in I/O buffered, recursive systems, or as real or imaginary data in the first stage of an 1K or smaller cascaded system.

MODE 3: Two 1Kx32 memories
Used as the overlap memories.

MODE 4: Two 2Kx16 memories
Used as the real or imaginary input memory pair in I/O buffered systems.

MODE 5: Two 2Kx16 memories
Used as the real or imaginary ouput memory pair in I/O buffered, recursive systems.

MODE 6: One 2Kx32 memory
Used as 'dual ported' coefficient memory.

Memory Bus and Clock Connections

In each of the modes, the BSC(2:0) and CAS control inputs determine the connection between a memory 'quad' and a data bus, the direction of the data bus, and the clock that controls the memory access cycle. The SWAP control input determines the connection between a memory 'quad' and an address bus. BSCs that associate a memory with an 'inner' system memory (as opposed to an input or output memory) overide the pipeline control pins and force all data and addresses to be pipelined.

A complete list of bus and clock connections for each mode appears in Tables 1-13.

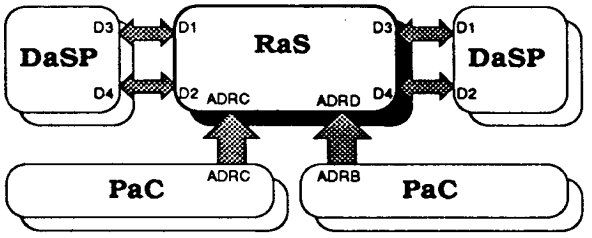


Figure 1: Mode 0 (dual 1Kx32) cascaded architecture

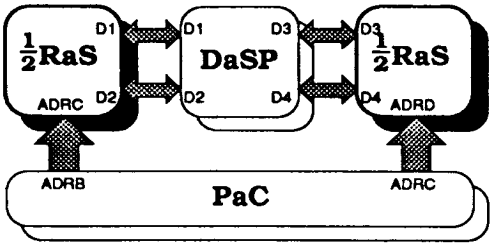


Figure 2: Mode 0 (dual 1Kx32) recursive architecture

Data Bus Connections for MODE 0 (CAS = 1)

BSC	MEMORY "C1" DBUS	I/O	PIPE	CLK	MEMORY "B2" DBUS	I/O	PIPE	CLK	REV DIR	ICLK OE
x00	D1:D2	I	P	1	D3:D4	O	P	0	0	n/a
x01	D1:D2	O	P	1	D3:D4	I	P	0	1	n/a
x10	D3:D4	O	P	0	D1:D2	I	P	1	0	n/a
x11	D3:D4	I	P	0	D1:D2	O	P	1	1	n/a

'P' means data and address busses are unconditionally pipelined
'C0' means pipeline mode depends on the state of IOP(0)
'C1' means pipeline mode depends on the state of IOP(1)

Address Bus Connections for MODE 0 (CAS = 1)

SWAP	MEMORY "C1" ABUS	SELECT	WE	MEMORY "B2" ABUS	SELECT	WE
0	ADRC	CS(2)&[ADRA(1:0)=CS(1:0)]	CWE	ADRD	CS(3)&[ADRB(1:0)=CS(1:0)]	DWE
1	ADRD	CS(3)&[ADRB(1:0)=CS(1:0)]	DWE	ADRC	CS(2)&[ADRA(1:0)=CS(1:0)]	CWE

Table 1: Mode 0 (dual 1Kx32) cascaded architecture

Data Bus Connections for MODE 0 (CAS = 0)

BSC	MEMORY "B" DBUS	I/O	PIPE	CLK	MEMORY "C" DBUS	I/O	PIPE	CLK	REV DIR	ICLK OE
000	D1:D2	O	P	1	D3:D4	I	P	1	0	0
001	D1:D2	I	P	1	D3:D4	O	P	1	1	0
011	D1:D2	I	C0	2	D3:D4	O	C1	0	0	1
100	D3:D4	O	C1	0	D1:D2	I	C0	2	0	1
010	D1:D2	O	P	1	D3:D4	I	P	1	0	0
101	D1:D2	I	P	1	D3:D4	O	P	1	1	0
111	D1:D2	I	C0	2	D3:D4	O	C1	0	0	1
110	D3:D4	O	C1	0	D1:D2	I	C0	2	0	1

Address Bus Connections for MODE 0 (CAS = 0)

SWAP	MEMORY "B" ABUS	SELECT	WE	MEMORY "C" ABUS	SELECT	WE
0	ADRC	CS(2)&[ADRA(1:0)=CS(1:0)]	CWE	ADRD	CS(3)&[ADRB(1:0)=CS(1:0)]	DWE
1	ADRD	CS(3)&[ADRB(1:0)=CS(1:0)]	DWE	ADRC	CS(2)&[ADRA(1:0)=CS(1:0)]	CWE

Table 2: Mode 0 (dual 1Kx32) recursive architecture

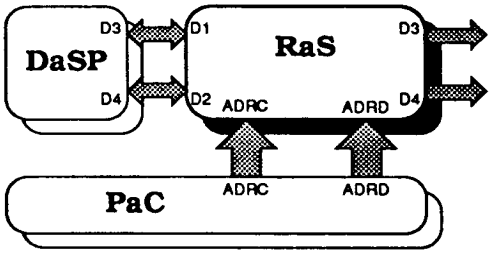


Figure 3: Mode 1 (dual 1Kx32) cascaded architecture

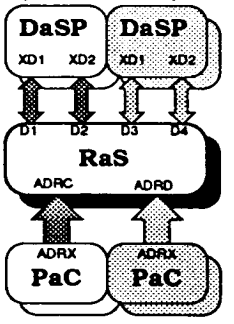


Figure 4: Mode 1 (dual 1Kx32) auxiliary architecture

Data Bus Connections for MODE 1 (CAS = 1)

BSC	MEMORY "C" DBUS	I/O	PIPE	CLK	MEMORY "D" DBUS	I/O	PIPE	CLK	REV DIR	ICLK OE
x00	D1:D2	I	P	1	D3:D4	O	C1	0	n/a	n/a
x01	D1:D2	O	P	1	D3:D4	O	C1	0	n/a	n/a
x10	D3:D4	O	C1	0	D1:D2	I	P	1	n/a	n/a
x11	D3:D4	O	C1	0	D1:D2	O	P	1	n/a	n/a

Address Bus Connections for MODE 1 (CAS = 1)

SWAP	MEMORY "C" ABUS	SELECT	WE	MEMORY "D" ABUS	SELECT	WE
0	ADRC	CS(2)&[ADRA(1:0)=CS(1:0)]	CWE	ADRD	CS(3)&[ADRB(1:0)=CS(1:0)]	DWE
1	ADRD	CS(3)&[ADRB(1:0)=CS(1:0)]	DWE	ADRC	CS(2)&[ADRA(1:0)=CS(1:0)]	CWE

Table 3: Mode 1 (dual 1Kx32) cascaded architecture

Data Bus Connections for MODE 1 (CAS = 0)

BSC	MEMORY "X0" DBUS	I/O	PIPE	CLK	MEMORY "X1" DBUS	I/O	PIPE	CLK	REV DIR	ICLK OE
000	D1:D2	O	C0	1	D3:D4	O	C1	0	n/a	n/a
001	D1:D2	O	C0	1	D3:D4	I	C1	0	n/a	n/a
010	D1:D2	I	C0	1	D3:D4	O	C1	0	n/a	n/a
011	D1:D2	I	C0	1	D3:D4	I	C1	0	n/a	n/a
100	D3:D4	O	C1	0	D1:D2	O	C0	1	n/a	n/a
101	D3:D4	I	C1	0	D1:D2	O	C0	1	n/a	n/a
110	D3:D4	O	C1	0	D1:D2	I	C0	1	n/a	n/a
111	D3:D4	I	C1	0	D1:D2	I	C0	1	n/a	n/a

Address Bus Connections for MODE 1 (CAS = 0)

SWAP	MEMORY "X0" ABUS	SELECT	WE	MEMORY "X1" ABUS	SELECT	WE
0	ADRC	CS(2)&[ADRA(1:0)=CS(1:0)]	CWE	ADRD	CS(3)&[ADRB(1:0)=CS(1:0)]	DWE
1	ADRD	CS(3)&[ADRB(1:0)=CS(1:0)]	DWE	ADRC	CS(2)&[ADRA(1:0)=CS(1:0)]	CWE

Table 4: Mode 1 (dual 1Kx32) auxiliary architecture

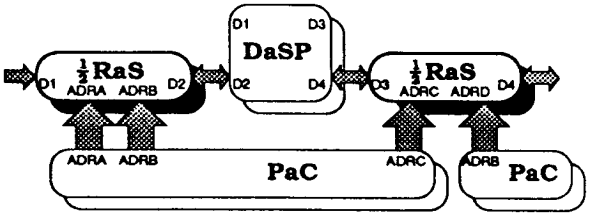


Figure 5: Mode 2 (quad 1Kx16) cascaded architecture

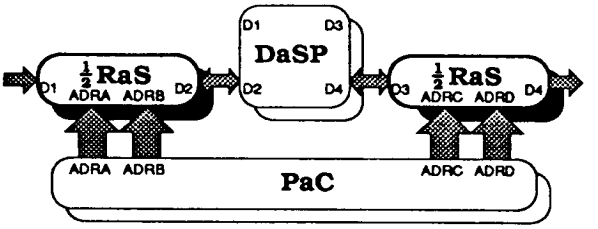


Figure 6: Mode 2 (quad 1Kx16) recursive architecture

Data Bus Connections for MODE 2 (CAS = 1)

BSC	MEMORY "A0" DBUS I/O PIPE CLK	MEMORY "B0" DBUS I/O PIPE CLK	MEMORY "C0" DBUS I/O PIPE CLK	MEMORY "B1" DBUS I/O PIPE CLK	REV DIR	ICLK OE
000	1/F I C0 2/F	D2 O P 1	D3 I P 1	D4 O P 0	0	+2
001	1/F I C0 2/F	D2 I P 1	D3 O P 1	D4 I P 0	1	+2
010	D2 O P 1	1/F I C0 2/F	D4 O P 0	D3 I P 1	0	+2
011	D2 I P 1	1/F I C0 2/F	D4 I P 0	D3 O P 1	1	+2
100	1/F I C0 2/F	D2 O P 1	D3 I P 1	D4 O P 0	0	+1
101	1/F I C0 2/F	D2 I P 1	D3 O P 1	D4 I P 0	1	+1
110	D2 O P 1	1/F I C0 2/F	D4 O P 0	D3 I P 1	0	+1
111	D2 I P 1	1/F I C0 2/F	D4 I P 0	D3 O P 1	1	+1

'1/F' means data is input on D1. If FIFOEN' is LOW, the FIFO is enabled and the memory quad is connected to the FIFO output
'2/F' means CLK(2) clocks data into D1. If the FIFO is enabled, CLKF is used to clock the data out of the FIFO and CLK(1) is used to clock address and data into the memory quad

Address Bus Connections for MODE 2 (CAS = 1)

SWAP	MEMORY "A0" ABUS	CS	WE	MEMORY "B0" ABUS	CS	WE	MEMORY "C0" ABUS	CS	WE	MEMORY "B1" ABUS	CS	WE
0	ADRA	CS(0)	AWE	ADRB	CS(1)	BWE	ADRC	CS(2)	CWE	ADRD	CS(3)	DWE
1	ADRB	CS(1)	BWE	ADRA	CS(0)	AWE	ADRD	CS(3)	DWE	ADRC	CS(2)	CWE

Table 5: Mode 2 (quad 1Kx16) cascaded architecture

Data Bus Connections for MODE 2 (CAS = 0)

BSC	MEMORY "A" DBUS I/O PIPE CLK	MEMORY "B" DBUS I/O PIPE CLK	MEMORY "C" DBUS I/O PIPE CLK	MEMORY "D" DBUS I/O PIPE CLK	REV DIR	ICLK OE
000	1/F I C0 2/F	D2 O P 1	D3 I P 1	D4 O C1 0	0	+2
001	1/F I C0 2/F	D2 I P 1	D3 O P 1	D4 O C1 0	1	+2
011	D2 O P 1	1/F I C0 2/F	D4 O C1 0	D3 I P 1	0	+2
100	D2 I P 1	1/F I C0 2/F	D4 O C1 0	D3 O P 1	1	+2
010	D4 O C1 0	1/F I C0 2/F	D3 O P 1	D2 I P 1	1	+2
101	D2 O P 1	D4 O C1 0	D3 I P 1	1/F I C02/F	0	+2
111	D4 O C1 0	1/F I C0 2/F	D3 I P 1	D2 O P 1	0	+2
110	D2 I P 1	D4 O C1 0	D3 O P 1	1/F I C02/F	1	+2

Address Bus Connections for MODE 2 (CAS = 0)

SWAP	MEMORY "A" ABUS	CS	WE	MEMORY "B" ABUS	CS	WE	MEMORY "C" ABUS	CS	WE	MEMORY "D" ABUS	CS	WE
0	ADRA	CS(0)	AWE	ADRB	CS(1)	BWE	ADRC	CS(2)	CWE	ADRD	CS(3)	DWE
1	ADRB	CS(1)	BWE	ADRA	CS(0)	AWE	ADRD	CS(3)	DWE	ADRC	CS(2)	CWE

Table 6: Mode 2 (quad 1Kx16) recursive architecture

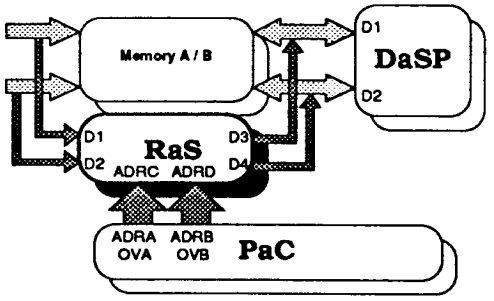


Figure 7: Mode 3 (dual 1Kx32) overlap architecture

Bus	State 0	1	2	3	4	0	1	2	3	4
D1:D2	X	X	*Memory A*		*A/OVA*	X	X	*Memory B*		*B/OVB*
D3:D4	X	X	*OVA*	*Memory B*		X	X	*OVB*	*Memory A*	

Table 7: Mode 3 (dual 1Kx32) overlap memory states

SWAP	BSC	STATE	MEMORY "OVA" DBUS I/O PIPE CLK ABUS	MEMORY "OVB" DBUS I/O PIPE CLK ABUS
0	00x	0-2	D3:D4 O P 1 ADRD	n/a n/a n/a n/a n/a
0	00x	3-4	D1:D2 I C0 0 ADRC	n/a n/a n/a n/a n/a
0	!00x	0-2	n/a n/a n/a n/a n/a	D3:D4 O P 1 ADRC
0	!00x	3-4	n/a n/a n/a n/a n/a	D1:D2 I C0 0 ADRD
1	xxx	0-2	n/a n/a n/a n/a n/a	D3:D4 O P 1 ADRD
1	xxx	3-4	n/a n/a n/a n/a n/a	D1:D2 I C0 0 ADRC

Table 8: Mode 3 (dual 1Kx32) overlap architecture

RaS Pin Name	DaSP Connection	PaC Connection	Memory Connection
ADRC(9:0)	nc	ADRA(9:0)	nc
ADRD(9:0)	nc	ADRB(9:0)	nc
D1/D2(15:0)	nc	nc	Dr /Di (15:0)
D3/D4(15:0)	D1/D2(15:0)	nc	nc
CWE	nc	OVAWE	nc
DWE	nc	OVBWE	nc
CS(2)	nc	OVACS	nc
CS(3)	nc	OVBCS	nc
FIFOEN	nc	EOPR	nc
IBUSY	nc	BOP	nc
REVDIR	nc	nc	ACS
ICLKOE	nc	nc	BCS
CLK(0)	nc	ICLK	nc
CLK(1)	CLKIN	CLKIN	nc

Table 9: Mode 3 Typical Pin Connections

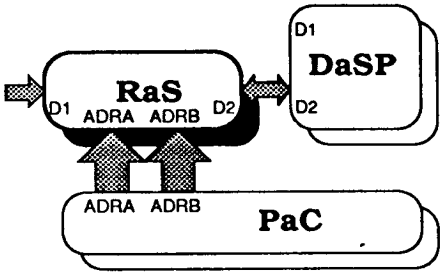


Figure 8: Mode 4 (dual 2Kx16) cascaded architecture

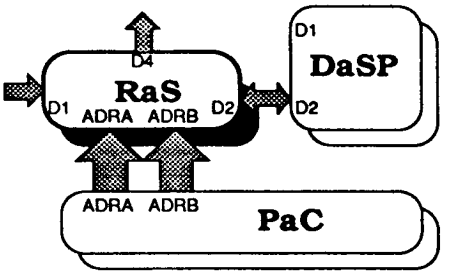


Figure 9: Mode 4 (dual 2Kx16) recursive architecture

Data Bus Connections for MODE 4 (CAS = 1)

BSC	MEMORY "A" DBUS	I/O	PIPE	CLK	MEMORY "B" DBUS	I/O	PIPE	CLK	REV DIR	ICLK OE
000	D1/F	I	C0	2/F	D2	O	P	1	0	+2
001	D1/F	I	C0	2/F	D2	I	P	1	1	+2
010	D2	O	P	1	D1/F	I	C0	2/F	0	+2
011	D2	I	P	1	D1/F	I	C0	2/F	1	+2
100	D1/F	I	C0	2/F	D2	O	P	1	0	+1
101	D1/F	I	C0	2/F	D2	I	P	1	1	+1
110	D2	O	P	1	D1/F	I	C0	2/F	0	+1
111	D2	I	P	1	D1/F	I	C0	2/F	1	+1

Address Bus Connections for MODE 4 (CAS = 1)

SWAP	MEMORY "A" ABUS	SELECT	WE	MEMORY "B" ABUS	SELECT	WE
0	A(2),C	CS(2)&[ADRA(1:0)=CS(1:0)]	CWE	B(2),D	CS(3)&[ADRB(1:0)=CS(1:0)]	DWE
1	B(2),D	CS(3)&[ADRB(1:0)=CS(1:0)]	DWE	A(2),C	CS(2)&[ADRA(1:0)=CS(1:0)]	CWE

Table 10: Mode 4 (dual 2Kx16) cascaded architecture

Data Bus Connections for MODE 4 (CAS = 0)

BSC	MEMORY "A" DBUS	I/O	PIPE	CLK	MEMORY "B" DBUS	I/O	PIPE	CLK	REV DIR	ICLK OE
000	D1/F	I	C0	2/F	D2	O	P	1	0	+2
001	D1/F	I	C0	2/F	D2	I	P	1	1	+2
011	D2	O	P	1	D1/F	I	C0	2/F	0	+2
100	D2	I	P	1	D1/F	I	C0	2/F	1	+2
010	D4	O	C1	0	D1/F	I	C0	2/F	1	+2
101	D2	O	P	1	D4	O	C1	0	0	+2
111	D4	O	C1	0	D1/F	I	C0	2/F	0	+2
110	D2	I	P	1	D4	O	C1	0	1	+2

Address Bus Connections for MODE 4 (CAS = 0)

SWAP	MEMORY "A" ABUS	SELECT	WE	MEMORY "B" ABUS	SELECT	WE
0	A(2),C	CS(2)&[ADRA(1:0)=CS(1:0)]	CWE	B(2),D	CS(3)&[ADRB(1:0)=CS(1:0)]	DWE
1	B(2),D	CS(3)&[ADRB(1:0)=CS(1:0)]	DWE	A(2),C	CS(2)&[ADRA(1:0)=CS(1:0)]	CWE

Table 11: Mode 4 (dual 2Kx16) recursive architecture

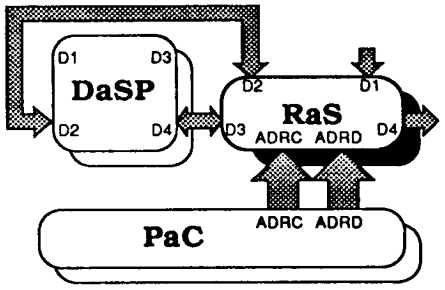


Figure 10: Mode 5 (dual 2Kx16) recursive architecture

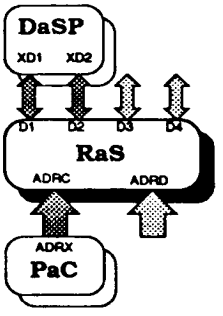


Figure 11: Mode 6 (2Kx32) auxiliary architecture

Data Bus Connections for MODE 5

BSC	MEMORY "C" DBUS	I/O	PIPE	CLK	MEMORY "D" DBUS	I/O	PIPE	CLK	REV DIR	ICLK OE
000	D3	I	P	1	D4	O	C1	0	0	+2
001	D3	O	P	1	D4	O	C1	0	1	+2
011	D4	O	C1	0	D3	I	P	1	0	+2
100	D4	O	C1	0	D3	O	P	1	1	+2
010	D3	O	P	1	D2	I	P	1	1	+2
101	D3	I	P	1	D1/F	I	C0	2/F	0	+2
111	D3	I	P	1	D2	O	P	1	0	+2
110	D3	O	P	1	D1/F	I	C0	2/F	1	+2

Address Bus Connections for MODE 5

SWAP	MEMORY "C" ABUS	SELECT	WE	MEMORY "D" ABUS	SELECT	WE
0	A(2),C	CS(2)&[ADRA(1:0)=CS(1:0)]	CWE	B(2),D	CS(3)&[ADRB(1:0)=CS(1:0)]	DWE
1	B(2),D	CS(3)&[ADRB(1:0)=CS(1:0)]	DWE	A(2),C	CS(2)&[ADRA(1:0)=CS(1:0)]	CWE

Table 12: Mode 5 (dual 2Kx16) recursive architecture

Data Bus Connections for MODE 6

BSC	MEMORY "X" DBUS	I/O	PIPE	CLK	REV DIR	ICLK OE
000	D1:D2	O	C0	1	n/a	n/a
001	D1:D2	O	C0	1	n/a	n/a
010	D1:D2	I	C0	1	n/a	n/a
011	D1:D2	I	C0	1	n/a	n/a
100	D3:D4	O	C1	2	n/a	n/a
101	D3:D4	I	C1	2	n/a	n/a
110	D3:D4	O	C1	2	n/a	n/a
111	D3:D4	I	C1	2	n/a	n/a

Address Bus Connections for MODE 6

SWAP	MEMORY "X" ADDRESS BUS	CHIP SELECT	WE
0	ADRA(2) , ADRC(9:0)	CS(2) & [ADRA(1:0) = CS(1:0)]	CWE
1	ADRB(2) , ADRD(9:0)	CS(3) & [ADRB(1:0) = CS(1:0)]	DWE

Table 13: Mode 6 (2Kx32) auxiliary architecture

ELECTRICAL CHARACTERISTICS

TEST LEVEL CODES	TEST LEVEL	TEST PROCEDURE
All electrical characteristics are subject to the following conditions:	I	100% production tested at the specified temperature.
All parameters having Min./Max. specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Assurance inspection. Any blank sections in the data columns indicates that the specification is not tested at the specified condition.	II	100% production tested at T_c = 25°C, and sample tested at the specified temperatures.
	III	QA sample tested only at the specified temperatures.
Unless otherwise noted, all tests are performed after device case reaches operating temperature.	IV	Parameter is guaranteed (but not tested) by design and characterization data.
	V	Parameter is a typical value for information purposes only.

a66311 COMMERCIAL ABSOLUTE MAXIMUM RATINGS (BEYOND WHICH DAMAGE MAY OCCUR)

Positive Supply Voltage .....-0.5V to 7.0V
DC Input Voltage .....-0.5V to 7.0V
DC Output Voltage (Applied in Hi-Z State) ..-0.5V to 7.0V
Low Level Output Current .....20 mA
Operating Case Temperature .....-55°C to +125°C
Storage Temperature .....-65°C to +150°C

Note:
Operation at any Absolute Maximum Rating is not implied. Ratings are provided for guidance purposes only and are not tested. Exposure to absolute maximum rating conditions over extended periods may affect device reliability.

a66311 COMMERCIAL TEMPERATURE RANGE[1]

DC ELECTRICAL PARAMETERS	TEST CONDITIONS	TEST LEVEL	a66311B MIN	a66311B TYP	a66311B MAX	a66311A MIN	a66311A TYP	a66311A MAX	UNITS
Input High Voltage(V_{IH})				2.0	V_{cc}		2.0	V_{cc}	V
Input Low Voltage(V_{IL})				0.8			0.8		V
Output High Voltage(V_{OH})	I_{OH}=-4.0mA			2.4			2.4		V
Output Low Voltage(V_{OL})	I_{OL}=4.0mA			0.4			0.4		V
Input High Leakage Current	V_{cc} Max			120			120		µA
Input Low Leakage Current	V_{cc} Max			-40			-40		µA
Hi-Z Output Leakage Current (Ioz)	V_{cc} Max, .6V <V_{OUT}<2.7V			20			20		µA
Operating Supply Current(I_{CC})	V_{cc} Max, f_{CI} Max			500			500		mA
CAPACITANCE									
Input Capacitance(C_{IN})	V_{CC} = 5V, T_C=25°C	V		10			10		pF
Output Capacitance(C_{OUT})	V_{CC} = 5V, T_C=25°C	V		10			10		pF

[1]**Test Conditions:**

T_C=0°C to +70°C, V_{CC} = 5V ± 5%, output load capacitance = 35 pF unless otherwise specified (T_C = case temperature).

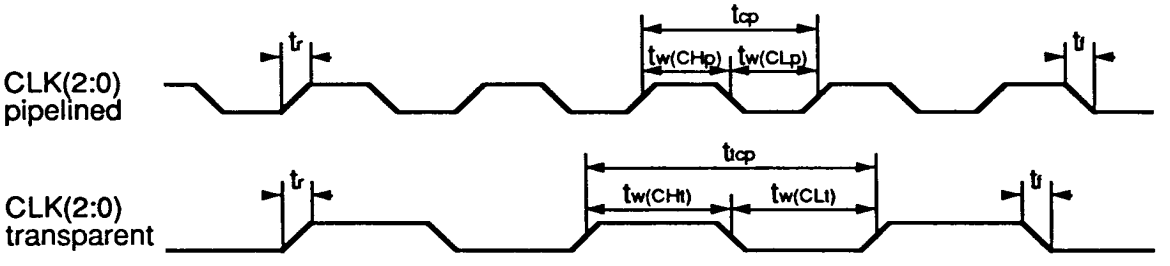
a66311 COMMERCIAL TEMPERATURE RANGE[1]

AC ELECTRICAL PARAMETERS		TEST CONDITIONS	TEST LEVEL	a66311B MIN	a66311B TYP	a66311B MAX	a66311A MIN	a66311A TYP	a66311A MAX	UNITS
CLK(2:0) Frequency	fci		I			30				MHz
	ftci		I			10				MHz
CLK(2:0) Period	tcp		I	33						nS
	ttcp		I	100						nS
CLK(2:0) Rise Time	tr		IV			10				nS
CLK(2:0) Fall Time	tf		IV			10				nS
CLK(2:0) Pulse Low	tw(CLp)		V	16						nS
	tw(CLt)		V	40						nS
CLK(2:0) Pulse High	tw(CHp)		V	16						nS
	tw(CHt)		V	40						nS
Address Set-up Time	tsu(Ap)		I	9						nS
	tsu(At)		I	9						nS
Address Hold Time	th(Ap)		I	0						nS
	th(At)		I	0						nS
Chip Select Set-up Time	tsu(Sp)		I	15						nS
	tsu(St)		I	15						nS
Chip Select Hold Time	th(Sp)		I	0						nS
	th(St)		I	0						nS
ADR Select Set-up Time	tsu(ASp)		I	25						nS
ADR Select Hold Time	th(ASp)		I	0						nS
Output Data Access Time	ta(Dp)		I	3		17				nS
	ta(Dt)		I			20				nS
Output Data Valid Time	tv(Dp)		IV	2						nS
	tv(Dt)		IV	3						nS
OE' to Data Driven	ten(E)		V	8		20				nS
OE' to Data High-Z	tdis(E)		V	8		35				nS
Input Data Set-up Time	tsu(Dp)		I	8						nS
	tsu(Dt)		I	20						nS
Input Data Hold Time	th(Dp)		I	0						nS
	th(Dt)		I	0						nS
WE' Set-up Time	tsu(Wp)		I	12						nS
	tsu(Wt)		I	20						nS
WE' Hold Time	th(Wp)		I	0						nS
	th(Wt)		I	0						nS

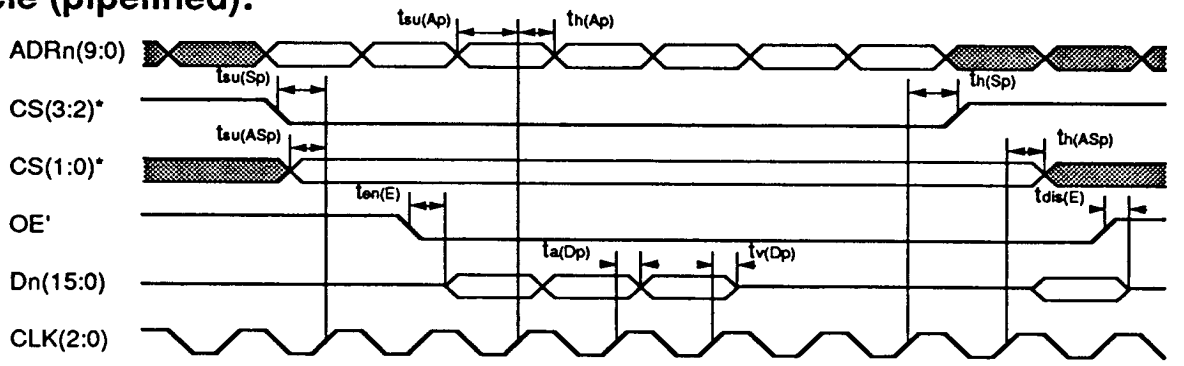
[1]Test Conditions:

T_c =0°C to +70°C, V_{cc} = 5V ± 5%, output load capacitance = 35 pF unless otherwise specified (T_c = case temperature).

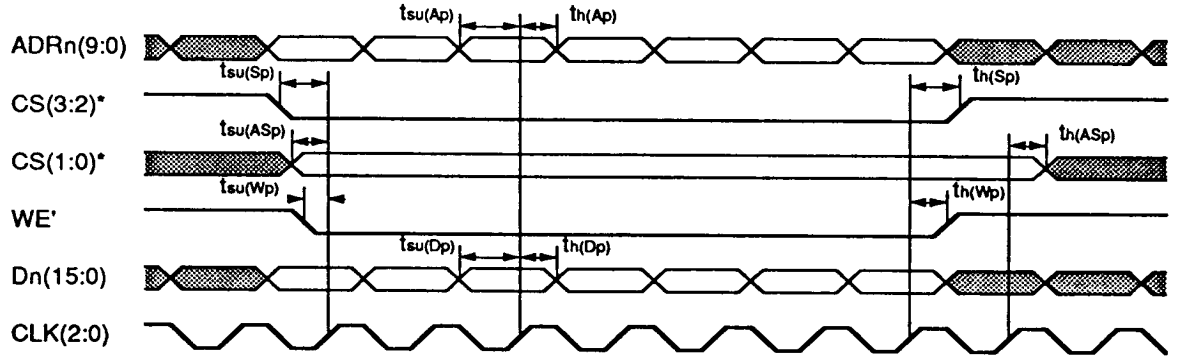
Clock Cycle:



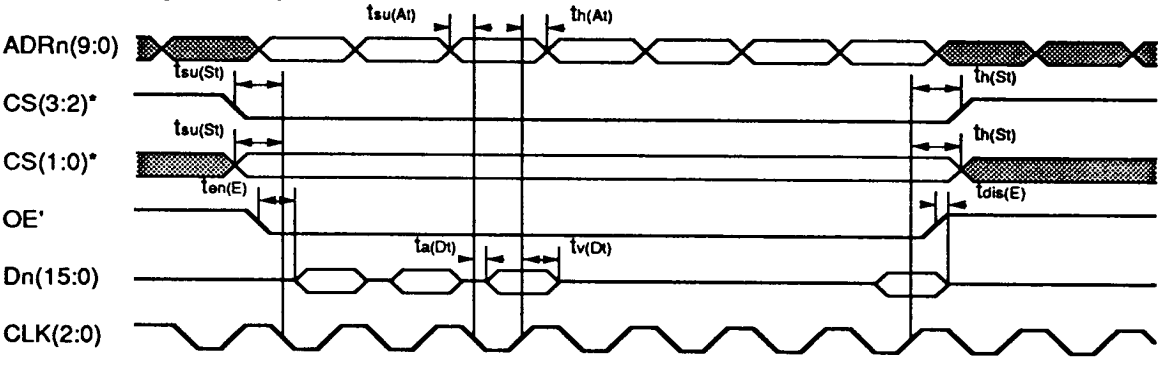
Read Cycle (pipelined):



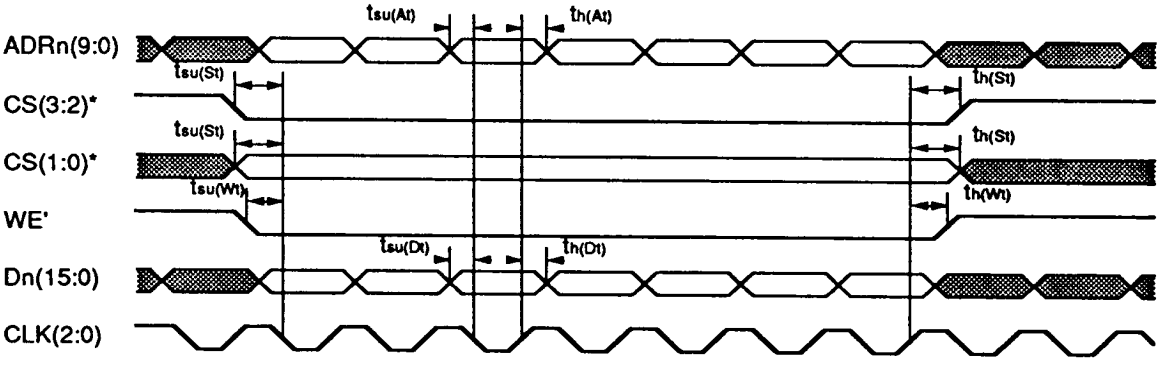
Write Cycle (no FIFO, pipelined):



Read Cycle (transparent):



Write Cycle (no FIFO, transparent):



* The CS(3:2) timing applies to CS(3:0) in MODE 2
* The CS(1:0) timing is not applicable to MODE 2

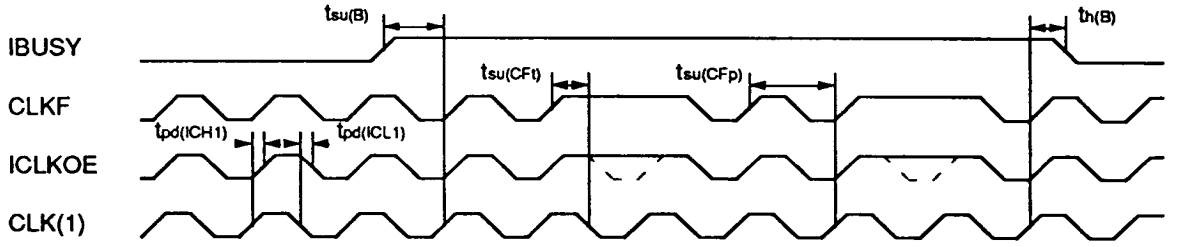
a66311 COMMERCIAL TEMPERATURE RANGE[1]

AC ELECTRICAL PARAMETERS		TEST CONDITIONS	TEST LEVEL	a66311B MIN	a66311B TYP	a66311B MAX	a66311A MIN	a66311A TYP	a66311A MAX	UNITS
IBUSY Set-up Time	tsu(B)		I	15						nS
IBUSY Hold Time	th(B)		I	0						nS
CLK(1) to ICLKOE High	tpd(ICH1)		I			16				nS
	tpd(ICH2)		I			16				nS
CLK(1) to ICLKOE Low	tpd(ICL1)		I			16				nS
	tpd(ICL2)		I			16				nS
CLKF Set-up Time	tsu(CFp)		I	10						nS
	tsu(CFt)		I	20						nS

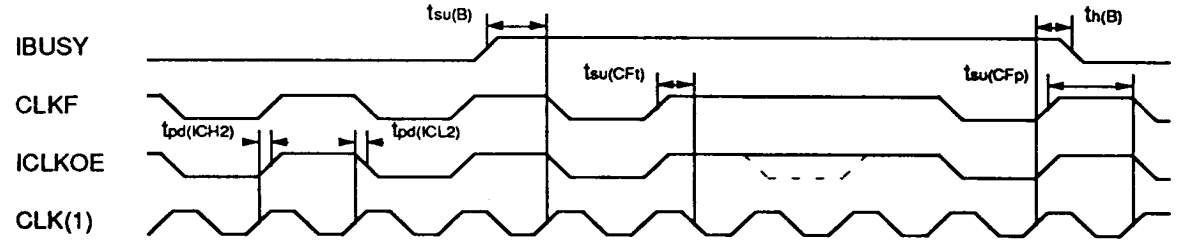
[1]**Test Conditions:**

T_c=0°C to +70°C, V_{cc} = 5V ± 5%, output load capacitance = 35 pF unless otherwise specified (T_c = case temperature).

FIFO Clock Generator (÷1 Mode):



FIFO Clock Generator (÷2 Mode):



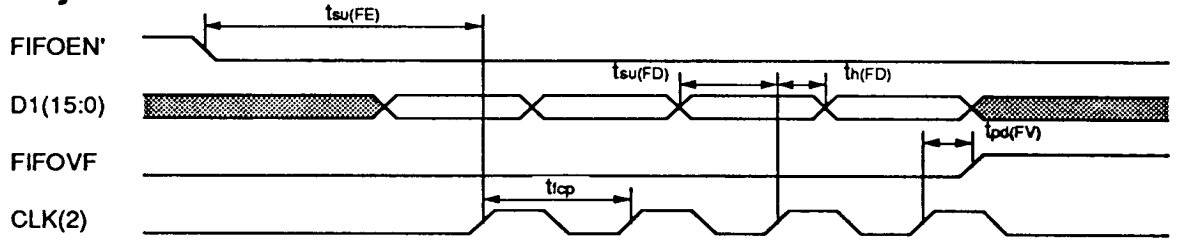
a66311 COMMERCIAL TEMPERATURE RANGE[1]

AC ELECTRICAL PARAMETERS		TEST CONDITIONS	TEST LEVEL	a66311B MIN	a66311B TYP	a66311B MAX	a66311A MIN	a66311A TYP	a66311A MAX	UNITS
FIFO CLK(2) Period	t_{fcp}		I	33						nS
CLK(2) to FIFOVF Delay	$t_{pd(FV)}$		I			10				nS
FIFOEN Set-up Time	$t_{su(FE)}$		I	20						nS
FIFO Input Data Set-up	$t_{su(FD)}$		I	8						nS
FIFO Input Data Hold	$t_{h(FD)}$		I	4						nS

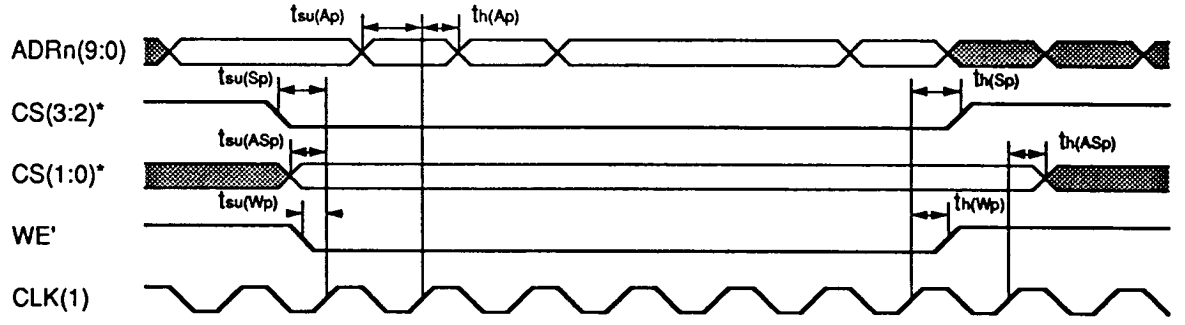
[1]**Test Conditions:**

T_c=0°C to +70°C, V_{cc} = 5V ± 5%, output load capacitance = 35 pF unless otherwise specified (T_c = case temperature).

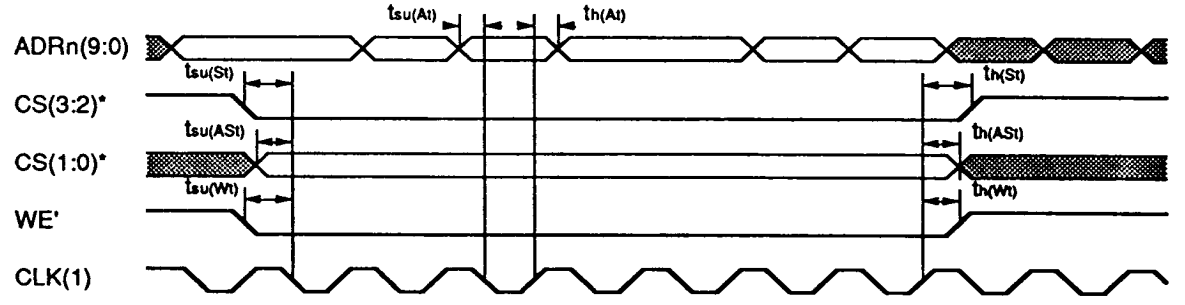
FIFO Input Cycle:



FIFO Output Cycle (pipelined):



FIFO Output Cycle (transparent):



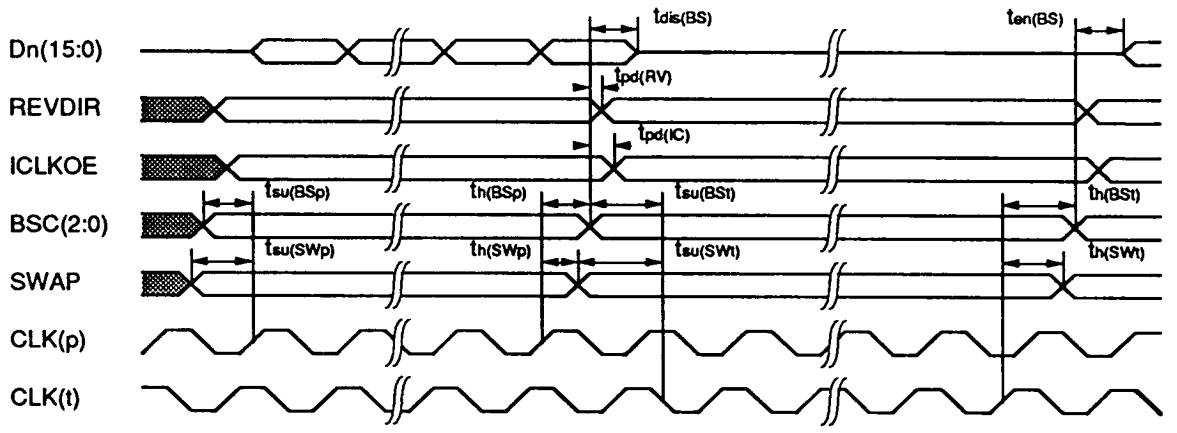
a66311 COMMERCIAL TEMPERATURE RANGE[1]

AC ELECTRICAL PARAMETERS		TEST CONDITIONS	TEST LEVEL	a66311B MIN	a66311B TYP	a66311B MAX	a66311A MIN	a66311A TYP	a66311A MAX	UNITS
BSC(2:0) Set-up Time	$t_{su(BSp)}$		I	50						nS
	$t_{su(BSt)}$		I	30						nS
BSC(2:0) Hold Time	$t_{h(BSp)}$		I	30						nS
	$t_{h(BSt)}$		I	0						nS
SWAP Set-up Time	$t_{su(SWp)}$		I	15						nS
	$t_{su(SWt)}$		I	15						nS
SWAP Hold Time	$t_{h(SWp)}$		I	0						nS
	$t_{h(SWt)}$		I	0						nS
BSC to REVDIR Delay	$t_{pd(RV)}$		I			35				nS
BSC to ICLKOE Delay	$t_{pd(IC)}$		I			35				nS
BSC to Data Driven	$t_{en(BS)}$		IV	10						nS
BSC to Data High-Z	$t_{dis(BS)}$		IV			50				nS

[1]Test Conditions:

T_c =0°C to +70°C, V_{cc} = 5V ± 5%, output load capacitance = 35 pF unless otherwise specified (T_c = case temperature).

BSC and SWAP Timing:



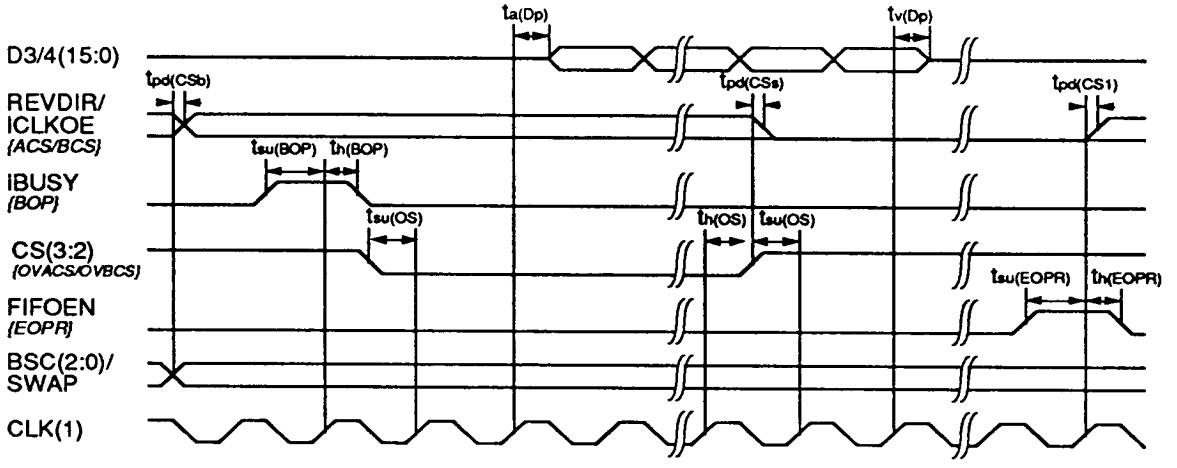
a66311 COMMERCIAL TEMPERATURE RANGE[1]

AC ELECTRICAL PARAMETERS	TEST CONDITIONS	TEST LEVEL	a66311B MIN	a66311B TYP	a66311B MAX	a66311A MIN	a66311A TYP	a66311A MAX	UNITS
IBUSY{BOP} Set-up Time $t_{su(BOP)}$		I	10						nS
IBUSY {BOP} Hold Time $t_{h(BOP)}$		I	0						nS
CS(3:2) {OVA/BCS} Setup $t_{su(OS)}$		I	25						nS
CS(3:2) {OVA/BCS} Hold $t_{h(OS)}$		I	0						nS
FIFOEN {EOPR} Set-up $t_{su(EOPR)}$		I	15						nS
FIFOEN {EOPR} Hold $t_{h(EOPR)}$		I	0						nS
BSC to {ACS/BCS} Delay $t_{pd(CSb)}$		I			25				nS
CS(3:2) {ACS/BCS} Delay $t_{pd(CSs)}$		I			25				nS
CLK(1) to {ACS/BCS} $t_{pd(CS1)}$		I			25				nS

[1]Test Conditions:

T_c =0°C to +70°C, V_{cc} = 5V ± 5%, output load capacitance = 35 pF unless otherwise specified (T_c = case temperature).

MODE 3 Timing:



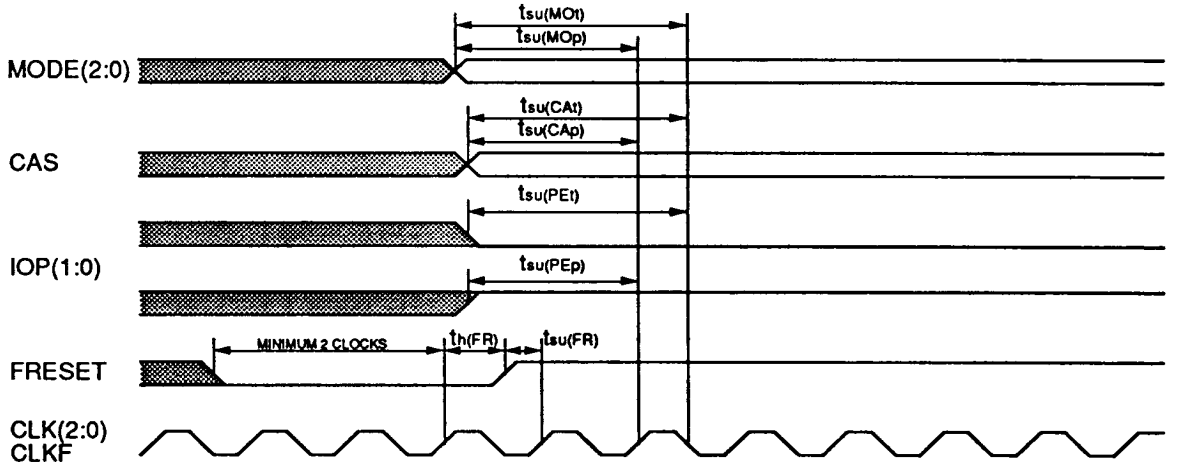
a66311 COMMERCIAL TEMPERATURE RANGE[1]

AC ELECTRICAL PARAMETERS		TEST CONDITIONS	TEST LEVEL	a66311B MIN	a66311B TYP	a66311B MAX	a66311A MIN	a66311A TYP	a66311A MAX	UNITS
MODE(2:0) Set-up Time	tsu(MOp)		IV	100						nS
	tsu(MOt)		IV	100						
CAS Set-up Time	tsu(CAp)		IV	100						nS
	tsu(CAt)		IV	100						
IOP(1:0) Set-up Time	tsu(PEp)		IV	100						nS
	tsu(PEt)		IV	100						
FRESET Set-up Time	tsu(FR)		IV	100						nS
FRESET Hold Time	th(FR)		IV	0						nS

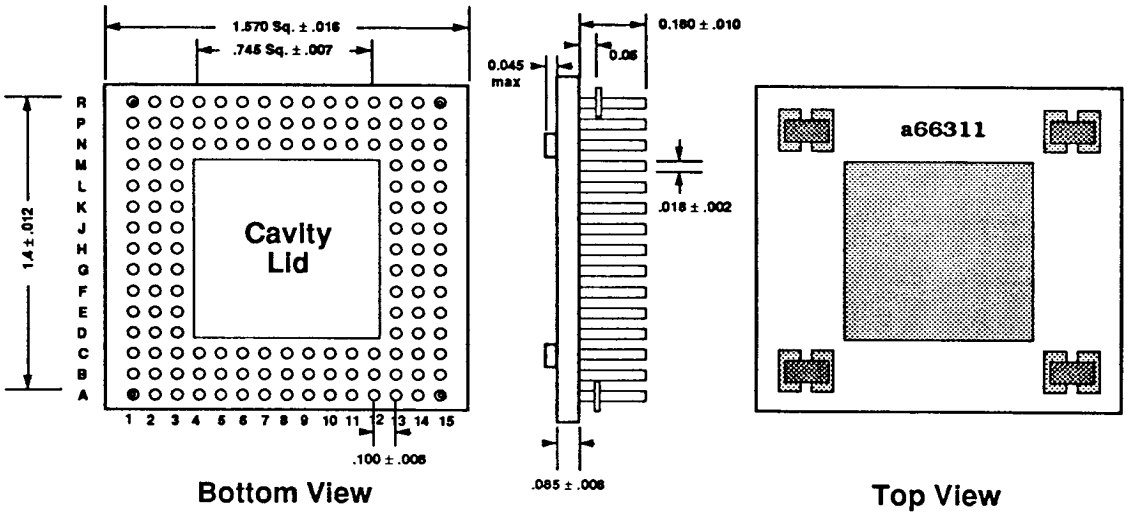
[1]Test Conditions:

T_c=0°C to +70°C, V_{cc} = 5V ± 5%, output load capacitance = 35 pF unless otherwise specified (T_c = case temperature).

Reset Timing:



a66311 Package Drawing:



Bottom View

Top View

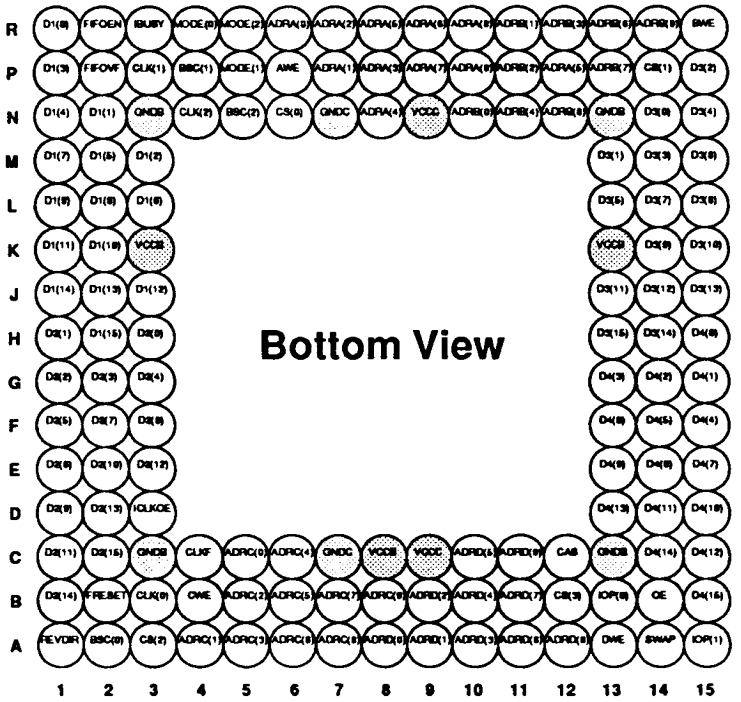
Notes:
Cavity down
100 mil pin spacing
All dimensions in inches

a66311 Pin Definitions:

PIN NAME	I/O TYPE	DESCRIPTION	NUMBEROF PINS USED
ADDRESS BUSES			
ADRA(9:0)	I	Memory Address Bus A	10
ADRB(9:0)	I	Memory Address Bus B	10
ADRC(9:0)	I	Memory Address Bus C	10
ADRD(9:0)	I	Memory Address Bus D	10
DATA BUSES			
D1(15:0)	I/O	Memory Data Port 1 (Connected to FIFO)	16
D2(15:0)	I/O	Memory Data Port 2	16
D3(15:0)	I/O	Memory Data Port 3	16
D4(15:0)	I/O	Memory Data Port 4	16
MEMORY STROBES			
AWE'	I	Memory A Write Enable	1
BWE'	I	Memory B Write Enable	1
CWE'	I	Memory C Write Enable	1
DWE'	I	Memory D Write Enable	1
IOP(1:0)	I	I/O Pipeline Enables	2
CS(3:0)	I	Chip Selects	4
OE'	I	Data Port Output Enable	1
FIFO CONTROLS			
FRESET'	I	FIFO Reset / Chip Reset	1
FIFOEN'	I	FIFO Enable (EOPR in Mode 3)	1
FIFOVF	O	FIFO Overflow	1
CLKF	I	FIFO Output Clock	1

PIN NAME	I/O TYPE	DESCRIPTION	NUMBEROF PINS USED
MEMORY CONFIGURATION CONTROL			
MODE(2:0)	I	Mode Control: Selects Memory Configuration	3
CAS	I	Cascaded Operation	1
SWAP	I	Address / Write Enable / Memory Select Control	1
BSC(2:0)	I	Bus Switch Code: Controls the Assignment of Data Ports and Clocks to Memories	3
TIMING CONTROLS			
CLK(2:0)	I	Memory and FIFO Clocks	3
IBUSY	I	Connect to PaC IBUSY (BOP Signal in Mode 3)	1
ICLKOE	O	Connect to PaC ICLK (DaSP OE' in Mode 0) (RAMB CS in Mode 3)	1
REVDIR	O	Connect to DaSP REVDIR (RAMA CS in Mode 3)	1
SUPPLY			
VCC	I	Voltage Supply	5
GND	I	Ground	6
TOTAL PINS USED ON THIS PACKAGE			**144**

a66311 Pinout:



a66311 Pin List:

SIGNAL	PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL	PIN
ADRA(9)	P10	ADRC(5)	B6	D1(7)	M1	D3(15)	H13	D4(7)	E15	MODE(1)	P5
ADRA(8)	R10	ADRC(4)	C6	D1(6)	L3	D3(14)	H14	D4(6)	F13	MODE(0)	R4
ADRA(7)	P9	ADRC(3)	A5	D1(5)	M2	D3(13)	J15	D4(5)	F14	CAS	C12
ADRA(6)	R9	ADRC(2)	B5	D1(4)	N1	D3(12)	J14	D4(4)	F15	SWAP	A14
ADRA(5)	R8	ADRC(1)	A4	D1(3)	P1	D3(11)	J13	D4(3)	G13	BSC(2)	N5
ADRA(4)	N8	ADRC(0)	C5	D1(2)	M3	D3(10)	K15	D4(2)	G14	BSC(1)	P4
ADRA(3)	P8	ADRD(9)	C11	D1(1)	N2	D3(9)	K14	D4(1)	G15	BSC(0)	A2
ADRA(2)	R7	ADRD(8)	A12	D1(0)	R1	D3(8)	L15	D4(0)	H15	CLK(2)	N4
ADRA(1)	P7	ADRD(7)	B11	D2(15)	C2	D3(7)	L14	AWE'	P6	CLK(1)	P3
ADRA(0)	R6	ADRD(6)	A11	D2(14)	B1	D3(6)	M15	BWE'	R15	CLK(0)	B3
ADRB(9)	R14	ADRD(5)	C10	D2(13)	D2	D3(5)	L13	CWE'	B4	IBUSY	R3
ADRB(8)	N12	ADRD(4)	B10	D2(12)	E3	D3(4)	N15	DWE'	A13	ICLKOE	D3
ADRB(7)	P13	ADRD(3)	A10	D2(11)	C1	D3(3)	M14	IOP(1)	A15	REVDIR	A1
ADRB(6)	R13	ADRD(2)	B9	D2(10)	E2	D3(2)	P15	IOP(0)	B13	VCCB	C8
ADRB(5)	P12	ADRD(1)	A9	D2(9)	D1	D3(1)	M13	CS(3)	B12	VCCB	K3
ADRB(4)	N11	ADRD(0)	A8	D2(8)	F3	D3(0)	N14	CS(2)	A3	VCCB	K13
ADRB(3)	R12	D1(15)	H2	D2(7)	F2	D4(15)	B15	CS(1)	P14	VCCC	C9
ADRB(2)	P11	D1(14)	J1	D2(6)	E1	D4(14)	C14	CS(0)	N6	VCCC	N9
ADRB(1)	R11	D1(13)	J2	D2(5)	F1	D4(13)	D13	OE'	B14	GNDB	C3
ADRB(0)	N10	D1(12)	J3	D2(4)	G3	D4(12)	C15	FRESET'	B2	GNDB	C13
ADRC(9)	B8	D1(11)	K1	D2(3)	G2	D4(11)	D14	FIFOEN'	R2	GNDB	N3
ADRC(8)	A7	D110)	K2	D2(2)	G1	D4(10)	D15	FIFOVF	P2	GNDB	N13
ADRC(7)	B7	D1(9)	L1	D2(1)	H1	D4(9)	E13	CLKF	C4	GNDC	C7
ADRC(6)	A6	D1(8)	L2	D2(0)	H3	D4(8)	E14	MODE(2)	R5	GNDC	N7

a66311 Ordering Information:

PART NUMBER	SPEED	PROCESSING	TEMPERATURE RANGE (case)	VOLTAGE RANGE	PINS	PACKAGE TYPE
a66311ACG	40MHz	Commercial	0° C to +70° C	4.75V to 5.25V	144	PGA
a66311BCG	30MHz	Commercial	0° C to +70° C	4.75V to 5.25V	144	PGA
a66311BIG	30MHz	Commercial	-40° C to +85° C	4.75V to 5.25V	144	PGA
a66311BEG	30MHz	Commercial	-55° C to +125° C	4.75V to 5.25V	144	PGA
a66311BMG	30MHz	MIL STD 883C	-55° C to +125° C	4.75V to 5.25V	144	PGA

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