

P-Channel 60-V (D-S) MOSFET

Key Features:

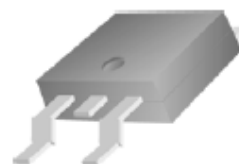
- Low $r_{DS(on)}$ trench technology
- Low thermal impedance
- Fast switching speed

Typical Applications:

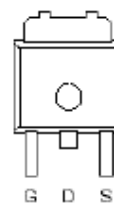
- PoE Power Sourcing Equipment
- PoE Powered Devices
- Telecom DC/DC converters
- White LED boost converters



RoHS
COMPLIANT
HALOGEN
FREE



TO-252



Top View

PRODUCT SUMMARY		
V_{DS} (V)	$r_{DS(on)}$ (m Ω)	I_D (A)
-60	17 @ $V_{GS} = -10V$	-44
	23 @ $V_{GS} = -4.5V$	-38

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)

Parameter	Symbol	Limit	Units
Drain-Source Voltage	V_{DS}	-60	V
Gate-Source Voltage	V_{GS}	± 20	
Continuous Drain Current	I_D	-44	A
Pulsed Drain Current ^b	I_{DM}	-150	
Continuous Source Current (Diode Conduction)	I_S	-48	A
Power Dissipation	P_D	50	W
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to 175	$^\circ\text{C}$

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Maximum	Units
Maximum Junction-to-Ambient ^a	$R_{\theta JA}$	40	$^\circ\text{C}/\text{W}$
Maximum Junction-to-Case	$R_{\theta JC}$	3	

Notes

- Surface Mounted on 1" x 1" FR4 Board, drain pad using 2 oz copper, value dependent on PC board thermal characteristics
- Pulse width limited by maximum junction temperature

Typical Electrical Characteristics

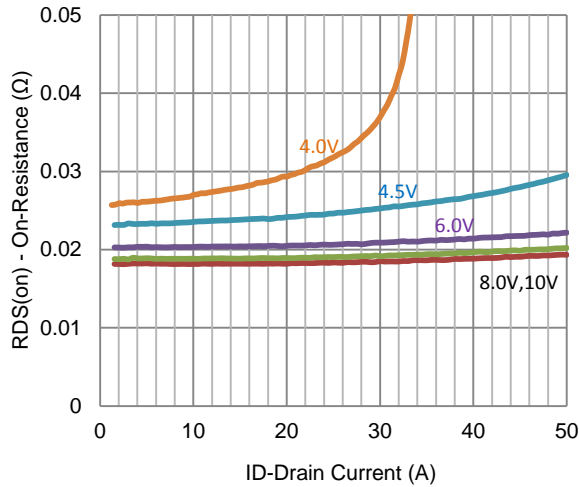
Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Static						
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250 \mu A$	-1			V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0 V, V_{GS} = \pm 20 V$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -48 V, V_{GS} = 0 V$			-1	uA
		$V_{DS} = -48 V, V_{GS} = 0 V, T_J = 55^\circ C$			-10	
On-State Drain Current	$I_{D(on)}$	$V_{DS} = -5 V, V_{GS} = -10 V$	-20			A
Drain-Source On-Resistance	$r_{DS(on)}$	$V_{GS} = -10 V, I_D = -22 A$			17	m Ω
		$V_{GS} = -4.5 V, I_D = -22 A$			23	
Forward Transconductance	g_{fs}	$V_{DS} = -15 V, I_D = -22 A$		8		S
Diode Forward Voltage	V_{SD}	$I_S = -24 A, V_{GS} = 0 V$		-0.9		V
Dynamic						
Total Gate Charge	Q_g	$V_{DS} = -30 V, V_{GS} = -10 V, I_D = -22 A$		83		nC
Gate-Source Charge	Q_{gs}			18		
Gate-Drain Charge	Q_{gd}			20		
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -30 V, R_L = 1.4 \Omega, I_D = -22 A,$ $V_{GEN} = -10 V, R_{GEN} = 6 \Omega$		11		nS
Rise Time	t_r			16		
Turn-Off Delay Time	$t_{d(off)}$			113		
Fall Time	t_f			42		
Input Capacitance	C_{iss}	$V_{DS} = -15 V, V_{GS} = 0 V, f = 1 MHz$		4654		pF
Output Capacitance	C_{oss}			526		
Reverse Transfer Capacitance	C_{rss}			347		

Notes

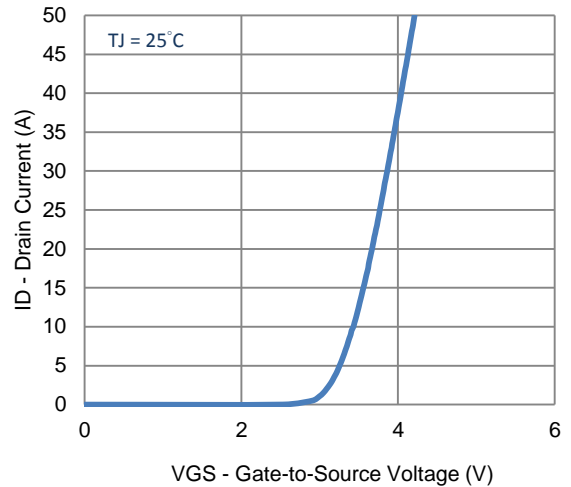
- Pulse test: PW \leq 300us duty cycle \leq 2%.
- Guaranteed by design, not subject to production testing.

Analog Power (APL) reserves the right to make changes without further notice to any products herein. APL makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does APL assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in APL data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. APL does not convey any license under its patent rights nor the rights of others. APL products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the APL product could create a situation where personal injury or death may occur. Should Buyer purchase or use APL products for any such unintended or unauthorized application, Buyer shall indemnify and hold APL and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that APL was negligent regarding the design or manufacture of the part. APL is an Equal Opportunity/Affirmative Action Employer.

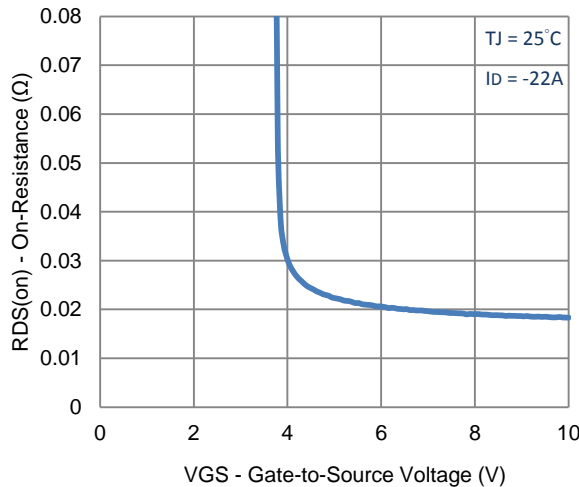
Typical Electrical Characteristics



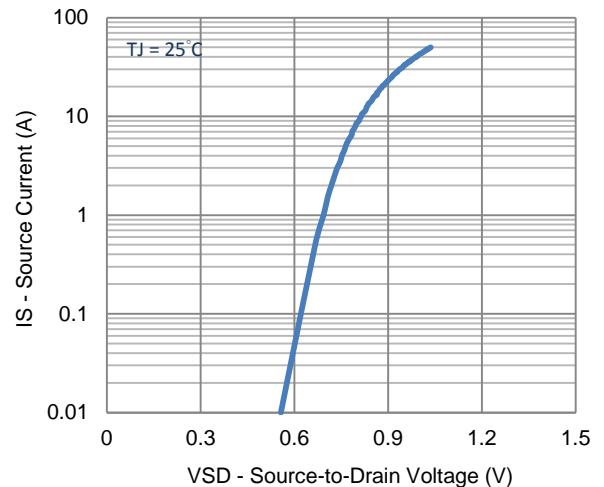
1. On-Resistance vs. Drain Current



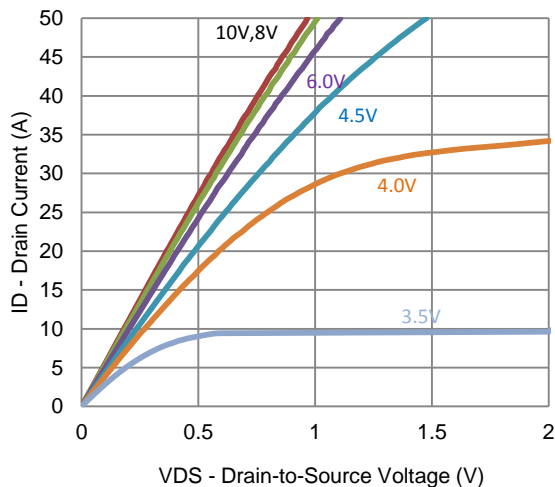
2. Transfer Characteristics



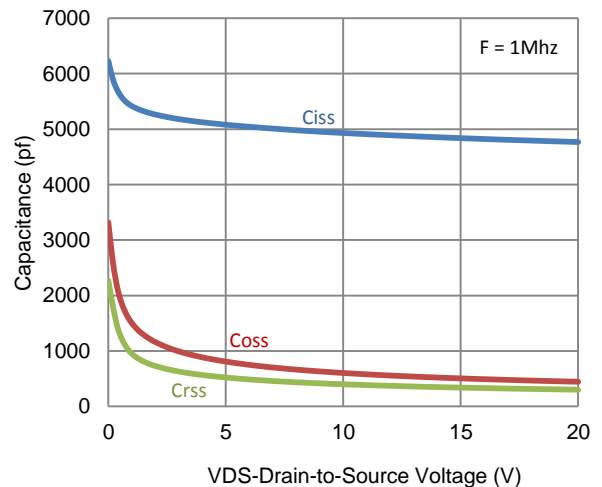
3. On-Resistance vs. Gate-to-Source Voltage



4. Drain-to-Source Forward Voltage

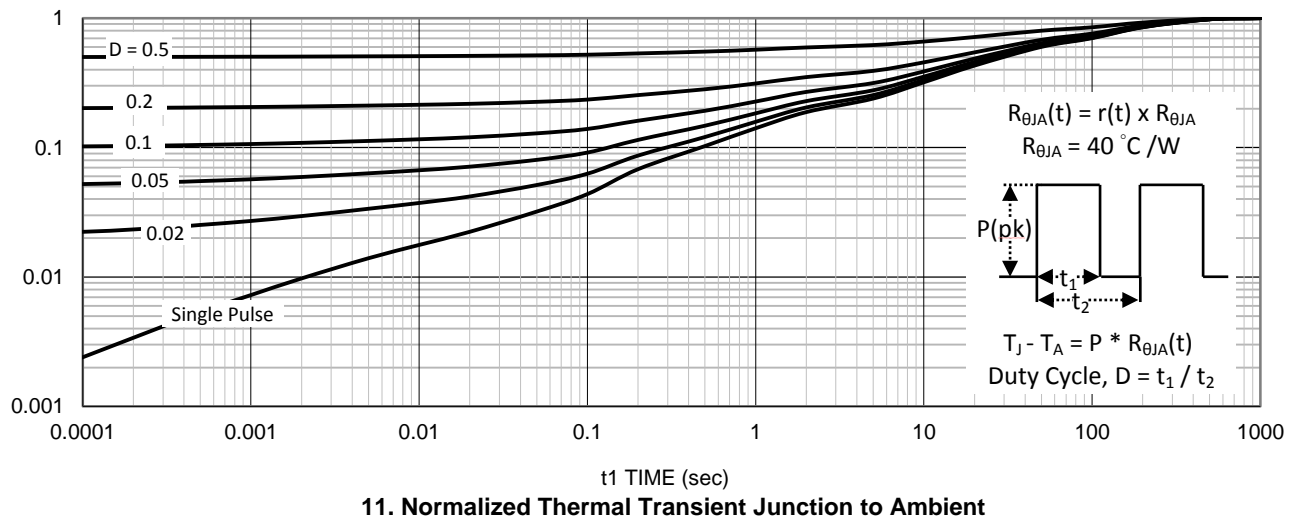
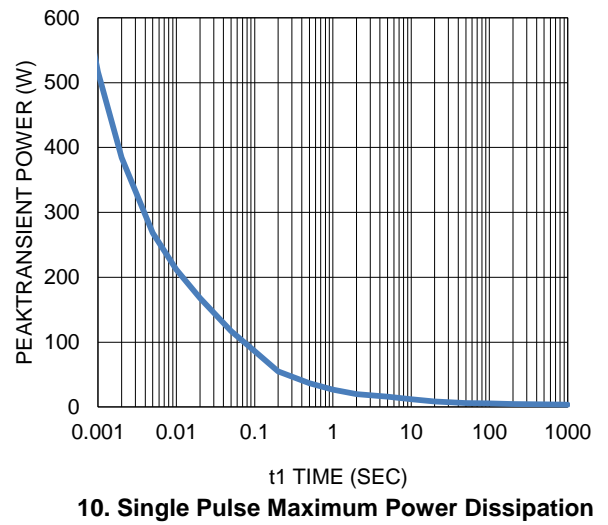
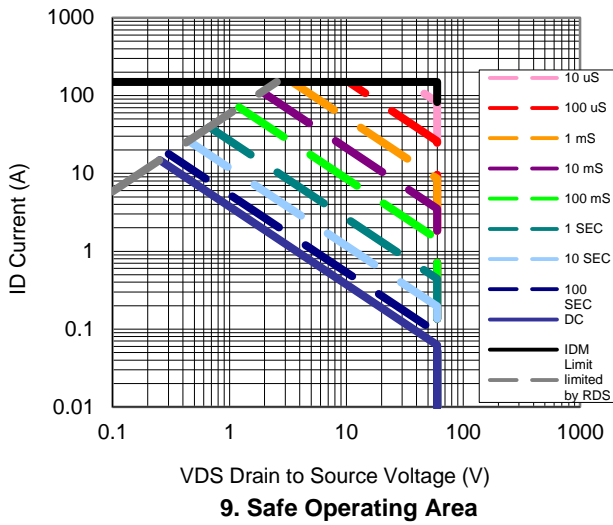
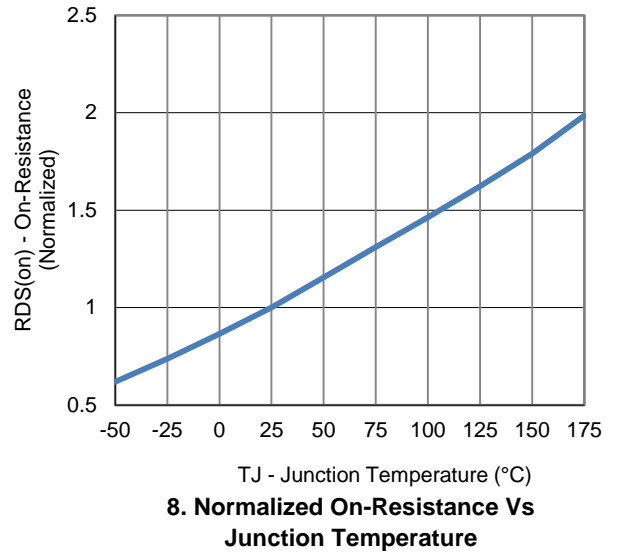
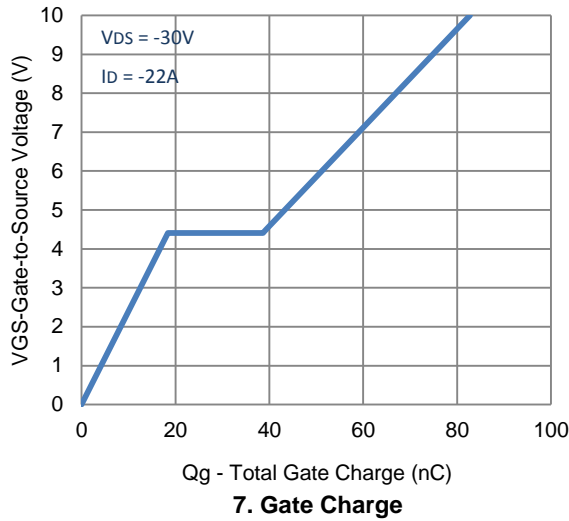


5. Output Characteristics

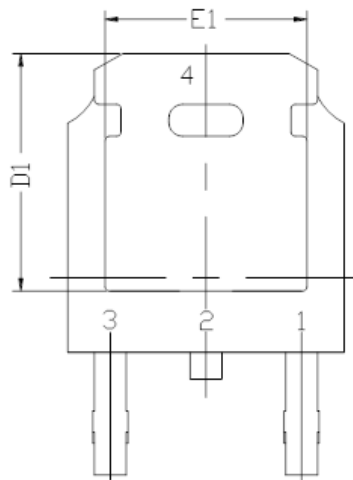
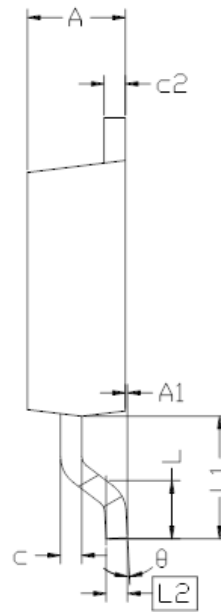
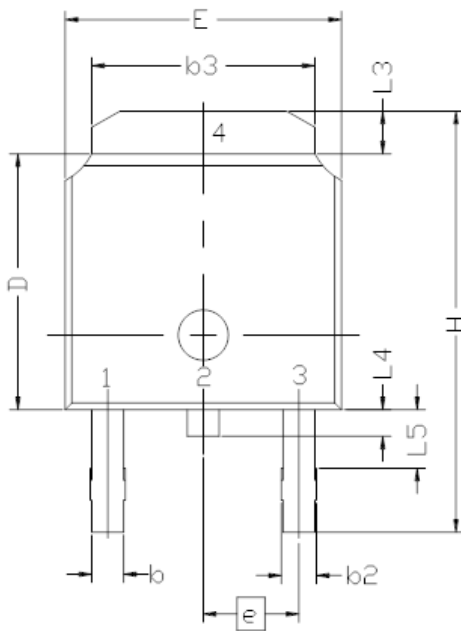


6. Capacitance

Typical Electrical Characteristics



Package Information



SYMBOL	DIMENSIONAL REQMTS		
	MIN	NOM	MAX
E	6.40	6.60	6.731
L	1.40	1.52	1.77
L1	2.743 REF		
L2	0.508 BSC		
L3	0.89	--	1.27
L4	0.64	--	1.01
L5	--	--	--
D	6.00	6.10	6.223
H	9.40	10.00	10.40
b	0.64	0.76	0.88
b2	0.77	0.84	1.14
b3	5.21	5.34	5.46
e	2.286 BSC		
A	2.20	2.30	2.38
A1	0	--	0.127
c	0.45	0.50	0.60
c2	0.45	0.50	0.58
D1	5.30	--	--
E1	4.40	--	--
θ	0°	--	10°

Note:

1. All Dimension Are In mm.
2. Package Body Sizes Exclude Mold Flash, Protrusion Or Gate Burrs. Mold Flash, Protrusion Or Gate Burrs Shall Not Exceed 0.10 mm Per Side.
3. Package Body Sizes Determined At The Outermost Extremes Of The Plastic Body Exclusive Of Mold Flash, Gate Burrs And Interlead Flash, But Including Any Mismatch Between The Top And Bottom Of The Plastic Body.