PLL

6

Contents

General Description

The PLL2013X is a Phase-Locked Loop (PLL) Frequency Synthesizer constructed in CMOS on single monolithic structure. The PLL macrofunctions provide frequency multiplication capabilities. The output clock frequency Fout is related to the reference input clock frequency Fin (XTALIN) by the following equation:

$$Fout = (m \times Fin) / (p \times 2^S)$$

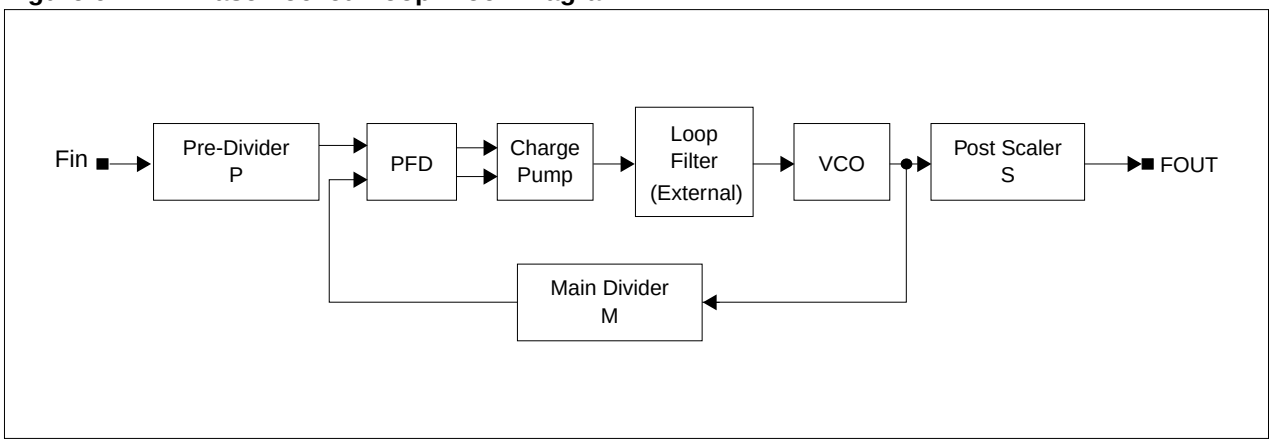
Where, Fout is the output clock frequency. Fin is the reference input clock frequency. m, p and s are the values for programmable dividers. PLL2013X consists of a Phase/Frequency Detector (PFD), a Charge Pump, an External Loop Filter, a Voltage Controlled Oscillator (VCO), a 6-bit Pre-divider, an 8-bit Main divider and a 2-bit Post Scaler as shown in Figure 6-1

Features

- 0.25μm CMOS device technology
- 2.5V single power supply
- Output frequency range: 20-170MHz
- Jitter: ±150 ps at 170MHz
- Duty ratio: 45% to 55% (All tuned range)
- Frequency changed by programmable dividers
- Provision for 14.318MHz crystal oscillator buffer (option)
- Lock detector (option)
- Power down mode

Block Diagram

Figure 6-1 Phase Locked Loop Block Diagram

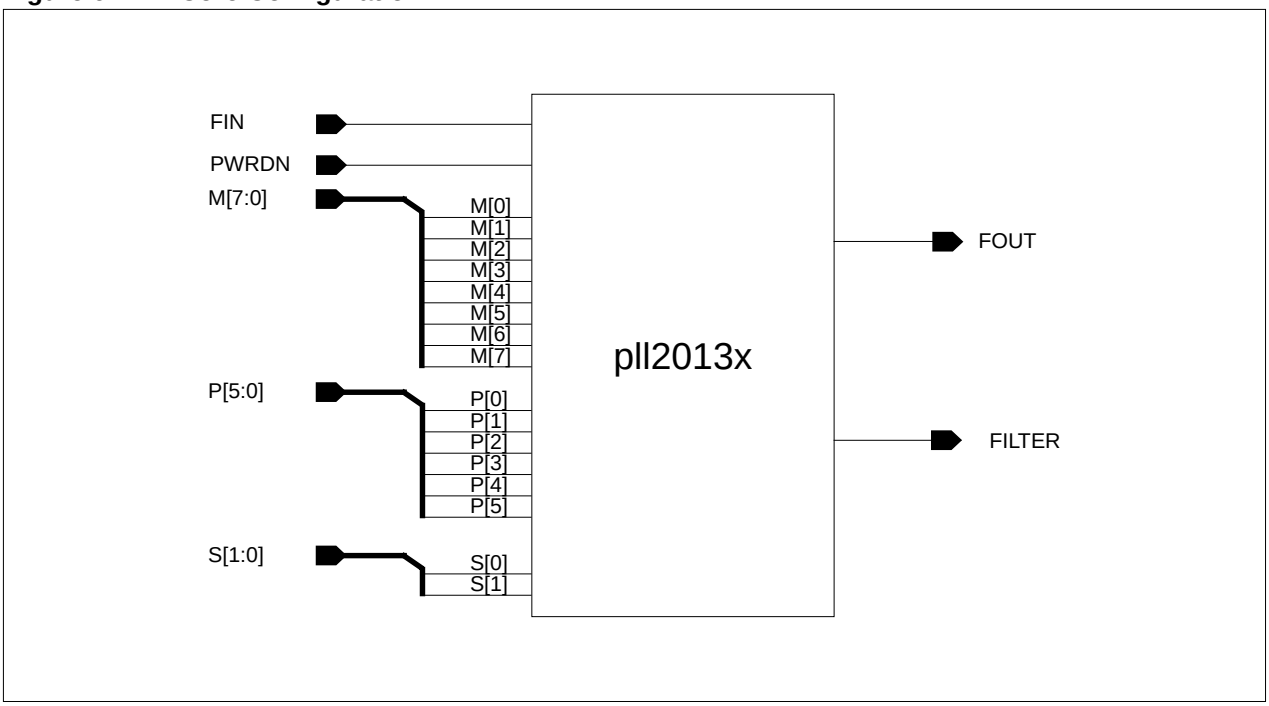


NOTE: X-tal oscillator and Lock detector are optional block. If customer concerns about this block - xtal buffer or lock detector, refer to next chapter.

Pin Description

NAME	I/O TYPE	I/O PAD	PIN DESCRIPTION
VDDD	Digital Power	vddd	Digital power supply
VSSD	Digital Ground	vssd	Digital ground
VDDA	Analog Power	vdda	Analog power supply
VSSA	Analog Ground	vssa	Analog ground
VBB	Analog sub bias /Digital sub bias	vbba	Analog / Digital sub bias
FIN	Digital Input	pic_bb	Reference Frequency Input
FILTER	Analog Output	poa_bb	Pump out is connected to Filter. A capacitor is connected between the pin and analog ground.
FOUT	Digital Output	pot8_bb	20MHz~170MHz clock output
PWRDN	Digital Input	pic_bb	FSPLL clock power down. - When PWRDN is High, PLL do not operate. - If PWRDN is not used, it should be tied to VSS.
P[5:0]	Digital Input	pic_bb	The values for 6bit programmable pre-divider.
M[7:0]	Digital Input	pic_bb	The values for 8bit programmable main divider.
S[1:0]	Digital Input	pic_bb	The values for 2bit programmable post scaler.

Figure 6-2 Core Configuration



Absolute Maximum Ratings (Ta=25°C)

Characteristics	Symbol	Value	Unit	Applicable Pin
Supply voltage	VDDD, VDDA	3.3	V	VDDD,VDDA,VSSD, VSSA,VBB
Voltage on any digital pin	Vin	VSSD-0.25 to VDDD+0.25	V	P[5:0],M[7:0],S[1:0] PWRDN
Operating temperature	Topr	0 to 70	°C	-
Storage temperature	Tstg	-45 to 125	°C	-

NOTES*:*

1. Absolute maximum rating specifies the values beyond which the device may be damaged permanently. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Each condition value is applied with the other values kept within the following operating conditions and function operation under any of these conditions is not implied.
2. All voltages are measured with respect to VSS unless otherwise specified.
3. 100pF capacitor is discharged through a 1.5kΩ resistor (human body model)

Recommended Operating Conditions

Characteristics	Symbol	Min	Typ	Max	Unit
Supply voltage	VDDD - VDDA	-0.1		+0.1	V
Oscillator frequency	Fosc		14.318		MHz
External loop filter capacitance	LF		820		pF
Operating temperature	Topr	0		70	°C

NOTE: It is strongly recommended that all the supply pins (VDDA, VDDD) be powered from the same operating supply voltage to avoid power latch-up.

DC Electrical Characteristics

Characteristics	Symbol	Min	Typ	Max	Unit
Operating voltage	VDDD/VDDA	2.375	2.5	2.625	V
Digital input voltage high	V_{IH}	2.0			V
Digital input voltage low	V_{IL}			0.8	V
Dynamic current	Idd			3	mA
Power down current	Ipd			50	µA

AC Electrical Characteristics

Characteristics	Symbol	Min	Typ	Max	Unit
Crystal frequency	F_{XTAL}		14.318		MHz
Input Frequency	F_{IN}	5		40	MHz
Output clock frequency	F_{OUT}	20		170	Mhz
Input clock duty cycle	T_{ID}	40		60	%
Output clock duty cycle (at 170MHz)	T_{OD}	45		55	%
Input glitch pulse width	T_{IGP}	1			ns
Locking time	T_{LT}			150	µs
Jitter, cycle to cycle	T_{JCC}	-150		+150	ps

NOTE: It is strongly recommended that input signal is not generated glitch, but if customer cannot help generating glitch, customer must carefully considerate the specification.

Functional Description

A PLL is the circuit synchronizing an output signal (generated by an VCO) with a reference or input signal in frequency as well as in phase.

In this application, it includes the following basic blocks.

— The voltage-controlled oscillator to generate the output frequency

— The divider P divides the reference frequency by p

— The divider M divides the VCO output frequency by m

— The divider S divides the VCO output frequency by s

— The phase frequency detector detects the phase difference between the reference frequency and the output frequency (after division) and controls the charge pump voltage.

— The loop filter removes the high frequency components in charge pump voltage and gives smooth and clean control to VCO

The m, p, s values can be programmed by 16bit digital data from the external source. So the PLL can be locked in the desired frequency.

$Fout = (m \times Fin) / (p \times s)$

where

$Fin = 14.318\ MHz,\ \ m = M + 8,\ \ p = P + 2,\ \ s = 2^S$

Table 6-1 Digital Data Format

Main Divider	Pre Divider	Post Scaler
M7, M6, M5, M4, M3, M2, M1, M0	P5, P4, P3, P2, P1, P0	S1, S0

NOTES:

1. S[1]-S[0]: Output frequency scaler
2. M[7]-M[0]: VCO frequency divider
3. P[5]-P[0]: Reference frequency input divider

OUTPUT FREQUENCY EQUATION & TABLE

Frequency equation: $F_{OUT} = \frac{(M+8)}{(P+2)\times 2^{S}} \times F_{IN}$

Table 6-2 Example of Divider Ratio

M7	M6	M5	M4	M3	M2	M1	M0	M	m(M+8)	S1	S0	2^S
0	1	0	1	0	1	0	1	85	93	0	0	1
P6	P5	P4	P3	P2	P1	P0	P	p(P+2)				
0	1	0	1	0	1	0	42	44				

CORE EVALUATION GUIDE

For the embedded PLL, we must consider the test circuits for the embedded PLL core in multiple applications. Hence the following requirements should be satisfied.

— The FILTER and FOUT pins must be bypassed for external test.
— For PLL test (below 2 examples), it is needed to control the dividers - M[7:0], P[5:0] and S[1:0] - that generate multiple clocks.

#1. Registers can be used for easy control of divider values.
#2. N sample bits of 16-bit divider pins can be bypassed for test using MUX.

Figure 6-3 PLL Functional Block Diagram

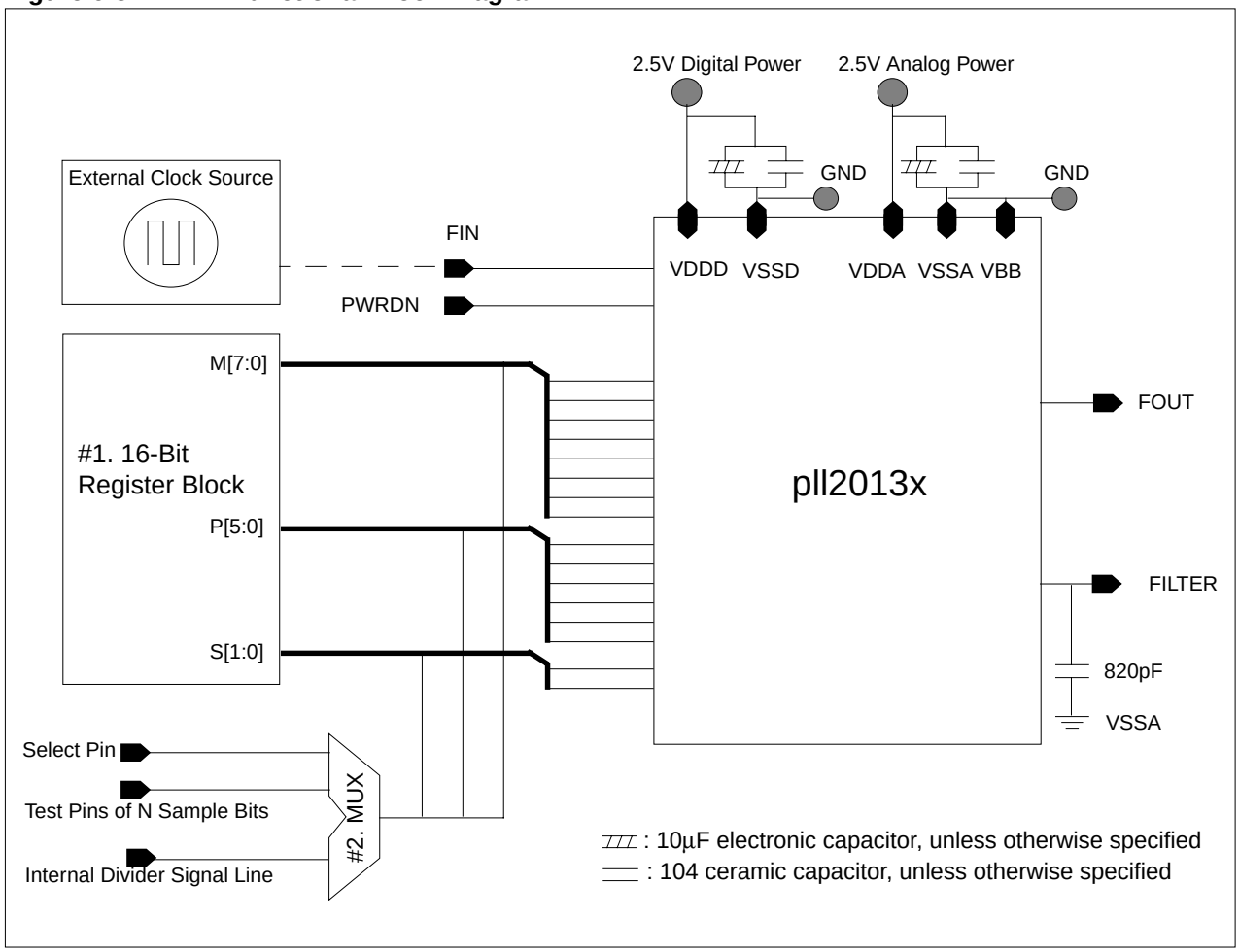
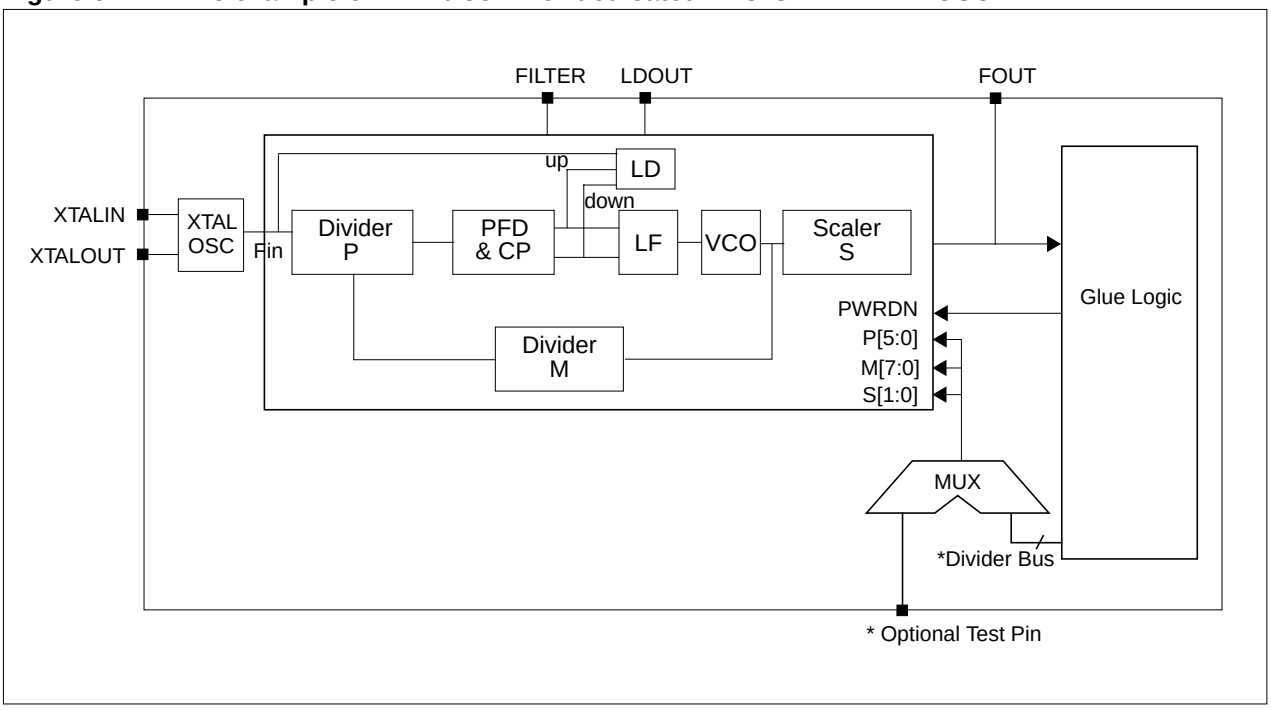
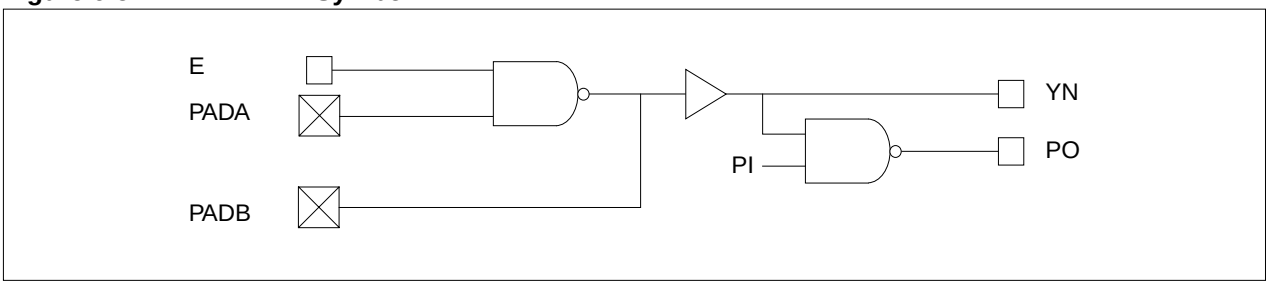


Figure 6-4 The example of PLL block with dedicated 14.318 MHz XTAL-OSC



XTAL Buffer Cell

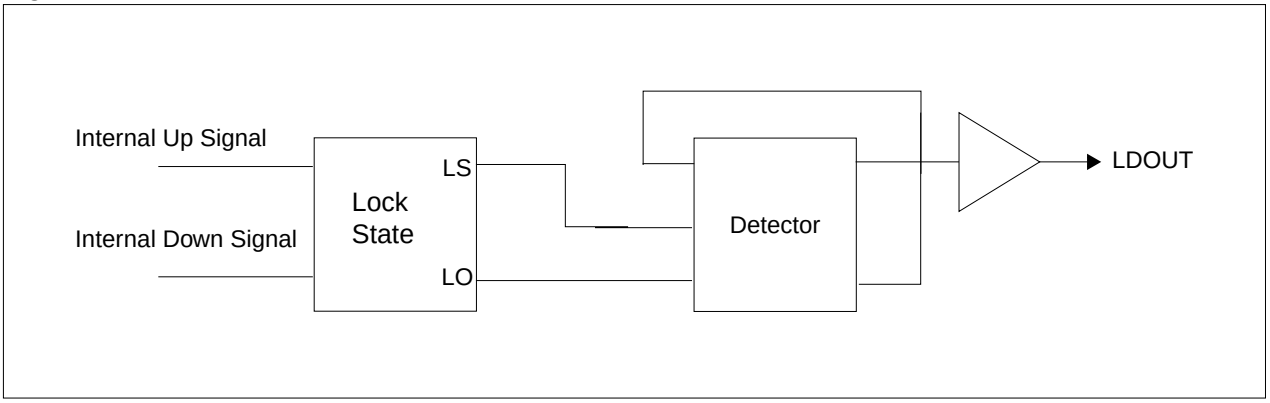
Figure 6-5 XTAL PAD Symbol



- A XTAL Buffer cell for PLL is supported MDL111 databook of SEC
- The XTAL must be located between PADA and PADB.
  Enable pin (E) must be HIGH in normal operation.
- PI pin must be connected to VDDD and the PO pin floated.

Lock Detector

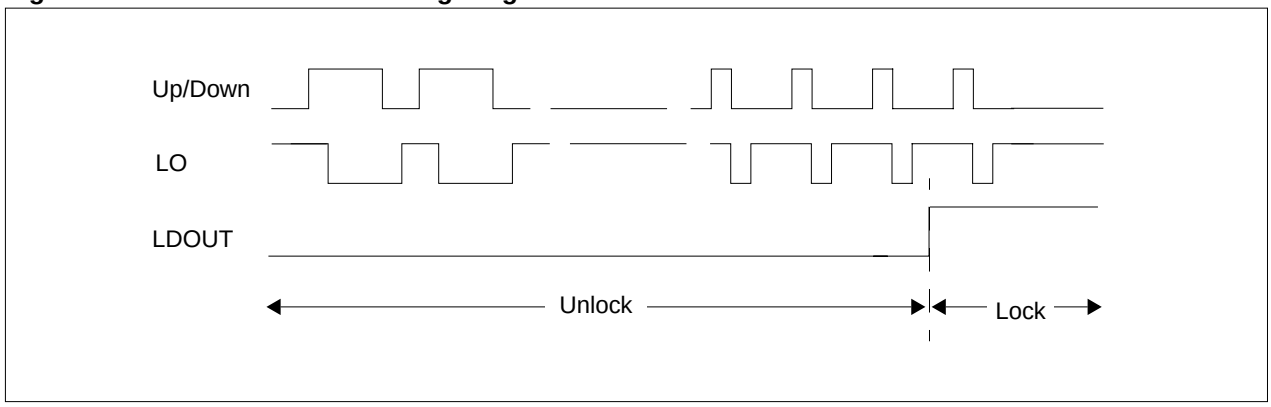
Figure 6-6 Lock Detector Block



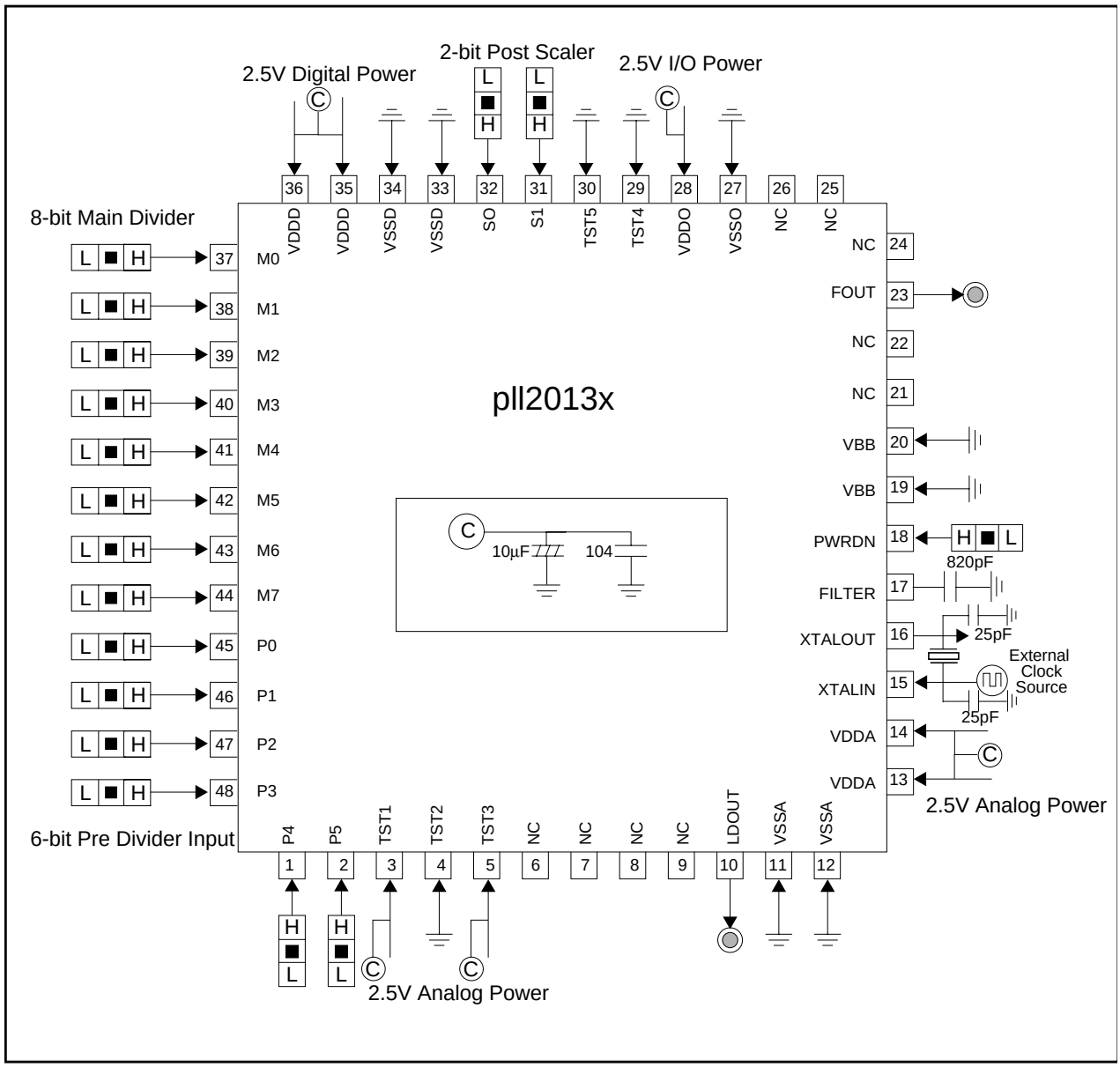
The built-in lock detector circuit will only work, when it is used in conjunction with PFD block output up/down

signal. (refer to Figure 6-6)
We represent the output of lock detector in the timing diagram. (refer to Figure 6-7)

Figure 6-7 Lock Detector Timing Diagram



PACKAGE CONFIGURATION



PACKAGE PIN DESCRIPTION

NAME	PIN No.	I/O TYPE	PIN DESCRIPTION
VDDD	35,36	DP	Digital power supply
VSSD	33,34	DG	Digital ground
VBB	19,20	AB/DB	Analog / digital sub bias
PWRDN	18	DI	FSPLL clock power down. - When PWRDN is High, PLL do not operate. - If PWRDN is not used, it should be tied to VSS.
P[0]~P[5]	45~48,1,2	DI	Pre-divider input
VDDA	13,14	AP	Analog power supply
VSSA	11,12	AG	Analog ground
XTALIN	15	AI	Crystal external clock input
XTALOUT	16	AO	Xtal buffer output clock
FOUT	23	DO	20MHZ~170MHz clock output
LDOUT	10	DO	Lock detector output
FILTER	17	AO	Pump out is connected to the Filter. A 900pF Capacitor is connected between the pin and analog pin
S[0]~S[1]	32,31	DI	Post scaler input
M[0]~M[7]	37~44	DI	8-bit main divider input
VDDO	28	PP	I/O pad power
VSSO	27	PG	I/O pad power

NOTES:

1. I/O TYPE PP and PG denote PAD power and PAD ground respectively.

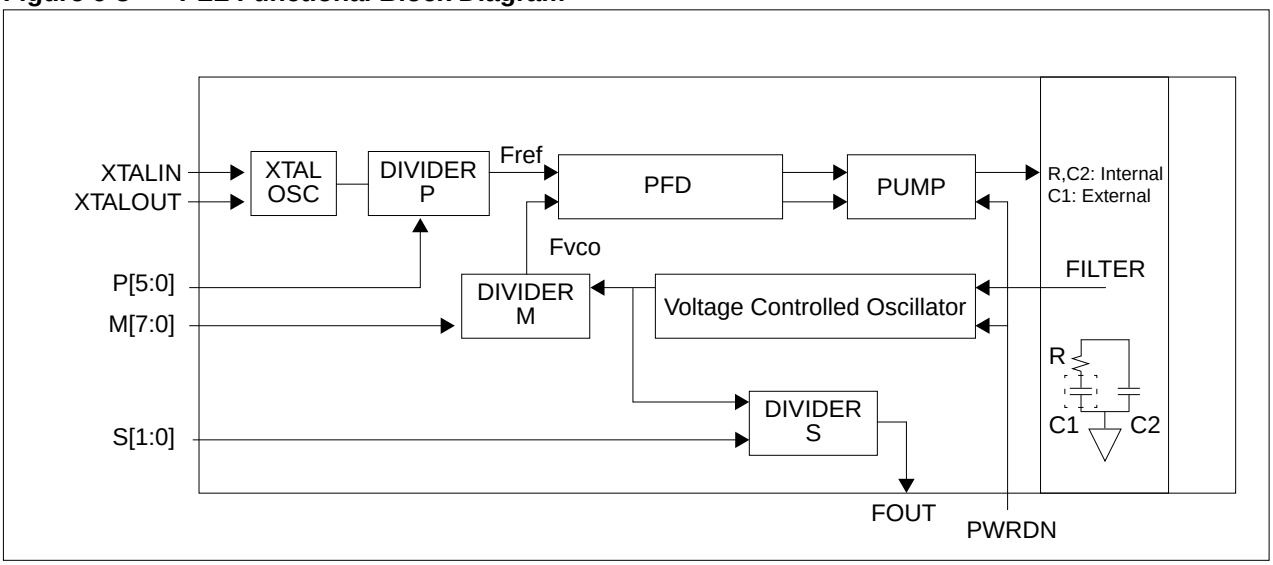
2. XTALIN, XTALOUT, LDOUT is test pin for PLL in Samsung.

PLL Components

Figure 6-8 is the block diagram of the components of a PLL: the phase detector, charge pump, voltage controlled oscillator, and loop filter.

In Samsung technology, the loop filter is implemented as external components close to the chip.

Figure 6-8 PLL Functional Block Diagram



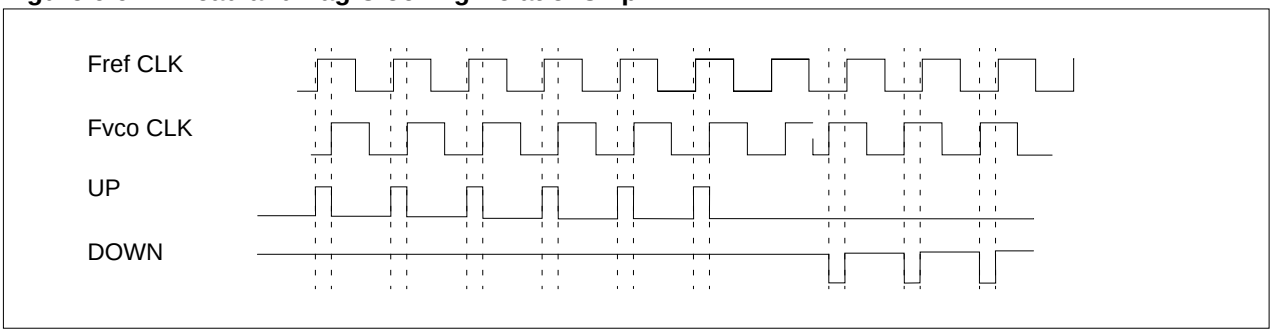
■Phase detector:

The phase detector monitors the phase difference between the Fref and Fvco, and generates a control signal when it detects difference between the two.

If the Fref frequency is higher then the Fvco frequency, its falling edge occurs before (lead) the falling edge of the Fvco output. When this occurs the phase detector signals the VCO to increase the frequency of the on-chip clock. If the falling edge of the Fref occurs after (lag) the falling edge of the Fvco output, the detector signals the VCO to decrease on-chip clock frequency. Figure 6-9 illustrates the lead and lag conditions.

If the frequencies of the Fref and Fvco are the same, the detect or does not generate a control signal, so the frequencies remain the same.

Figure 6-9 Lead and Lag Clocking Relationship



■Charge Pump:

The charge pump converts the phase detector control signal to a charge in voltage across the external filter that drives the VCO. As the Voltage Controlled Oscillator decreases, or increases, If the voltage remains constant, the frequency of the oscillator remains constant.

■Loop Filter:

The control signal that the phase detector generates for the charge pump may generate large excursions (ripples) each time the VCO output is compared to the system clock. To avoid overloading the VCO, a low pass filter samples and filters the high-frequency components out of the control signal. The filter is typically a single-pole RC filter consisting of a resistor and capacitor.

■ Voltage Controlled Oscillator (VCO):

The output voltage from the loop filter drives the VCO, causing its oscillation frequency to increase or decrease as a function of variations in voltage. When the VCO output matches the system clock in frequency and phase, the phase detector stops sending a control signal to the charge pump, which in turn stabilizes the input voltage to the loop filter. The VCO frequency then remains constant, and the PLL remains locked onto the system clock.

Frequency Synthesis

Frequency synthesis uses the system clock as a base frequency to generate higher/lower frequency clocks for internal logic.

For high speed applications in high-end designs, transmission line effects cause problems because of parasitic and impedance mismatch among various on-board components. These problems can be eliminated by moving the high frequency to the chip level. On-chip clocks that are faster than the external system clock can be synthesized by inserting a divider in the feedback path. The divider is placed after voltage controlled oscillator, as illustrated in Figure 6-11. The signal is running at M times the system clock frequency, so the PLL matches the divider signal output to the system clock. This configuration reduces the problem of interfacing to the system clock on the board, and it reduces the noise generated by the system clock oscillator and driver for all the components in the system.

Design Considerations

The following design considerations apply:

- Phase tolerance and jitter are independent of the PLL frequency.
- Jitter is affected by the noise frequency in the power (VDDD/VSSD, VDDA/VSSA). It increases when the noise level increases.
- A CMOS-level input reference clock is recommend for signal compatibility with the PLL circuit. Other levels such as TTL may degrade the tolerances.
- The used of two, or more PLLs requires special design considerations. Please consult your application engineer for more information.
- The following apply to the noise level, which can be minimized by using good analog power and ground isolation techniques in the system:
  - Use wide PCB traces for POWER (VDDD/VSSD, VDDA/VSSA, VBB) connections to the PLL core.
  - Separate the traces from the chip's VDDD/VSSD, VDDA/VSSA supplies.
  - Use proper VDDD/VSSD, VDDA/VSSA de-coupling.
  - Use good power and ground sources on the board.
  - Use power VBB for minimize substrate noise.
- The PLL core should be placed as close as possible to the dedicated loop filter and analog power and ground pins.
- It is inadvisable to locate noise-generating signals, such as data buses and high-current outputs, near the PLL I/O cells.
- Other related I/O signals should be placed near the PLL I/O but do not have any pre-defined placement restriction.

PLL Specification

We appreciate your interest in our products. If you have further questions, please specify in the attached form. Thank you very much.

Parameter	Min	Typ	Max	Unit	Remarks
Supply voltage					
Output frequency range					
Input frequency range					
Cycle-to-cycle jitter					
Lock up time					
Dynamic current					
Standby current					
Output clock duty ratio					
Long term jitter					
Output slew rate					

- Do you need XTAL driver buffer in PLL core?
  If you need it, what is the crystal frequency range?
  If not, What is the input frequency range?
- Do you need the lock detector?
- Do you need the I/O cell of Samsung?
- Do you need the external pin for PLL test?
- What is the main frequency and frequency range?
- How many FSPLLs do you use in your system?
- What is output loading?
- Could you internal/external pin configurations as required?
- Specially requested function list: