STE34NK80Z

N-CHANNEL 800V - 0.20Ω - 32A ISOTOP Zener-Protected SuperMESH™ MOSFET

PRODUCT PREVIEW

Table 1: General Features

TYPE	V_{DSS}	$R_{DS(on)}$	I_D	Pw
STE34NK80Z	800 V	< 0.24Ω	32 A	600 W

- TYPICAL R_{DS}(on) = 0.20 Ω
- EXTREMELY HIGH dv/dt CAPABILITY
- 100% AVALANCHE TESTED
- GATE CHARGE MINIMIZED
- VERY LOW INTRINSIC CAPACITANCES
- VERY GOOD MANUFACTURING REPEABILITY

DESCRIPTION

The SuperMESH™ series is obtained through an extreme optimization of ST's well established strip-based PowerMESH™ layout. In addition to pushing on-resistance significantly down, special care is taken to ensure a very good dv/dt capability for the most demanding applications. Such series complements ST full range of high voltage MOS-FETs including revolutionary MDmesh™ products.

APPLICATIONS

- HIGH CURRENT, HIGH SPEED SWITCHING
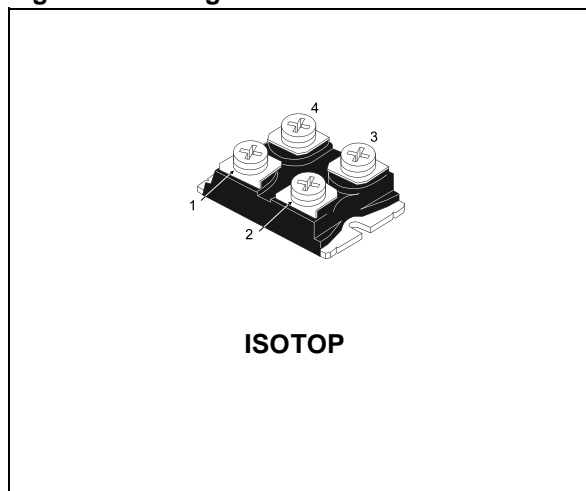- IDEAL FOR WELDING EQUIPMENT

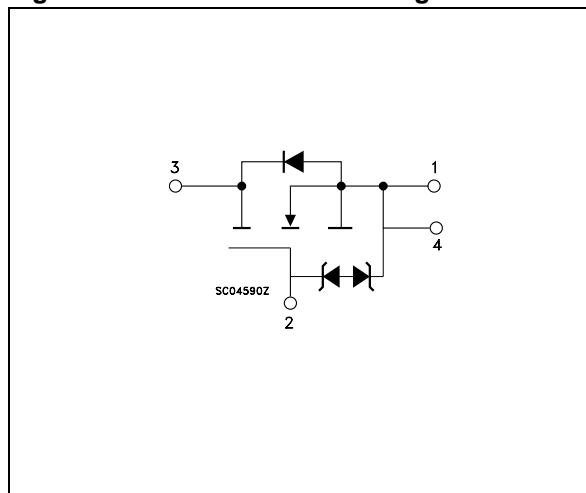### Figure 1: Package

ISOTOP

Figure 2: Internal Schematic Diagram

Table 2: Order Codes

SALES TYPE	MARKING	PACKAGE	PACKAGING
STE34NK80Z	E34NK80Z	ISOTOP	TUBE

Rev. 2

Table 3: Absolute Maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source Voltage (V_{GS} = 0)	800	V
V_{DGR}	Drain-gate Voltage (R_{GS} = 20 kΩ)	800	V
V_{GS}	Gate- source Voltage	± 30	V
I_D	Drain Current (continuous) at T_C = 25°C	32	A
I_D	Drain Current (continuous) at T_C = 100°C	20	A
I_{DM} (•)	Drain Current (pulsed)	128	A
P_{TOT}	Total Dissipation at T_C = 25°C	600	W
	Derating Factor	5	W/°C
$V_{ESD(G-S)}$	Gate source ESD (HBM-C= 100pF, R=1.5 kΩ)	6	KV
dv/dt (1)	Peak Diode Recovery voltage slope	4.5	V/ns
V_{ISO}	Insulation Withstand Voltage (AC-RMS) from All Four Terminals to External Heatsink	2500	V
T_j T_{stg}	Operating Junction Temperature Storage Temperature	-65 to 150	°C

(•) Pulse width limited by safe operating area
(1) I_{SD} ≤32A, di/dt ≤ 400 A/μs, V_{DD} ≤ $V_{(BR)DSS}$, T_j ≤ T_{JMAX}.

Table 4: Thermal Data

Rthj-case	Thermal Resistance Junction-case Max	0.2	°C/W
Rthj-amb	Thermal Resistance Junction-ambient Max	30	°C/W
T_l	Maximum Lead Temperature For Soldering Purpose	300	°C

Table 5: Avalanche Characteristics

Symbol	Parameter	Max Value	Unit
I_{AR}	Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by T_j max)	32	A
E_{AS}	Single Pulse Avalanche Energy (starting T_j = 25 °C, I_D = I_{AR}, V_{DD} = 35 V)	TBD	mJ

Table 6: Gate-Source Zener Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
BV_{GSO}	Gate source Breakdown Voltage	I_{gs}= ± 1 mA (Open Drain)	30			V

PROTECTION FEATURES OF GATE-TO-SOURCE ZENER DIODES

The built-in back-to-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.

ELECTRICAL CHARACTERISTICS (T$_{CASE}$ =25°C UNLESS OTHERWISE SPECIFIED)
Table 7: On/Off

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V$_{(BR)DSS}$	Drain-source Breakdown Voltage	I$_D$ = 1mA, V$_{GS}$ = 0	800			V
I$_{DSS}$	Zero Gate Voltage Drain Current (V$_{GS}$ = 0)	V$_{DS}$ = Max Rating V$_{DS}$ = Max Rating, T$_C$ = 125 °C			10 100	µA µA
I$_{GSS}$	Gate-body Leakage Current (V$_{DS}$ = 0)	V$_{GS}$ = ± 20V			±100	µA
V$_{GS(th)}$	Gate Threshold Voltage	V$_{DS}$ = V$_{GS}$, I$_D$ =100 µA	3	3.75	4.5	V
R$_{DS(on)}$	Static Drain-source On Resistance	V$_{GS}$ = 10V, I$_D$ = 11 A		0.2	0.24	Ω

Table 8: Dynamic

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g$_{fs}$ (1)	Forward Transconductance	V$_{DS}$ = 15 V, I$_D$= 11 A		TBD		S
C$_{iss}$ C$_{oss}$ C$_{rss}$	Input Capacitance Output Capacitance Reverse Transfer Capacitance	V$_{DS}$ = 25V, f = 1 MHz, V$_{GS}$ = 0		8000 750 190		pF pF pF
C$_{oss\ eq.}$ (3)	Equivalent Output Capacitance	V$_{GS}$ = 0V, V$_{DS}$ = 0V to 720 V		TBD		pF
t$_{d(on)}$ t$_r$ t$_{d(off)}$ t$_r$	Turn-on Delay Time Rise Time Turn-off Delay Time Fall Time	V$_{DD}$ = 450 V, I$_D$ = 11 A, R$_G$= 4.7 Ω, V$_{GS}$ = 10 V (see Figure 4)		TBD TBD TBD TBD		ns ns ns ns
Q$_g$ Q$_{gs}$ Q$_{gd}$	Total Gate Charge Gate-Source Charge Gate-Drain Charge	V$_{DD}$ = 720 V, I$_D$ = 32 A, V$_{GS}$ = 10V		390 TBD TBD	546	nC nC nC

Table 9: Source Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I$_{SD}$ I$_{SDM}$ (2)	Source-drain Current Source-drain Current (pulsed)				32 128	A A
V$_{SD}$ (1)	Forward On Voltage	I$_{SD}$ = 32 A, V$_{GS}$ = 0			TBD	V
t$_{rr}$ Q$_{rr}$ I$_{RRM}$	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	I$_{SD}$ = 32 A, di/dt = 100 A/µs V$_{DD}$ = 100 V, T$_j$ = 25°C (see test circuit, Figure 5)		TBD TBD TBD		ns µC A
t$_{rr}$ Q$_{rr}$ I$_{RRM}$	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	I$_{SD}$ = 32 A, di/dt = 100 A/µs V$_{DD}$ = 100V, T$_j$ = 150°C (see test circuit, Figure 5)		TBD TBD TBD		ns µC A

(1) Pulsed: Pulse duration = 300 µs, duty cycle 1.5 %.
(2) Pulse width limited by safe operating area.
(3) C$_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as Coss when VDS increases from 0 to 80% VDSS

Figure 3: Unclamped Inductive Load Test Circuit

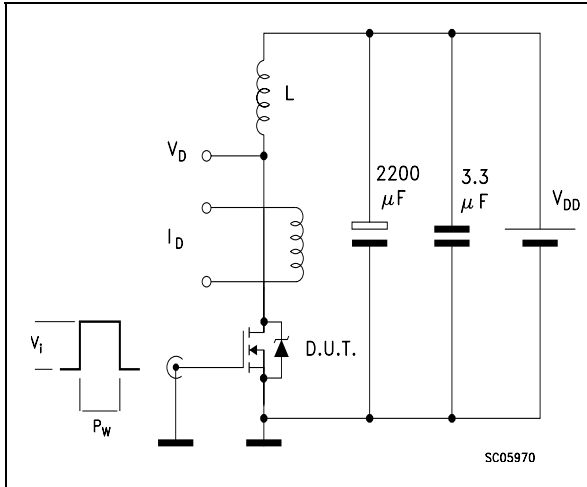**Figure 6: Unclamped Inductive Wafeform**

Figure 4: Switching Times Test Circuit For Resistive Load
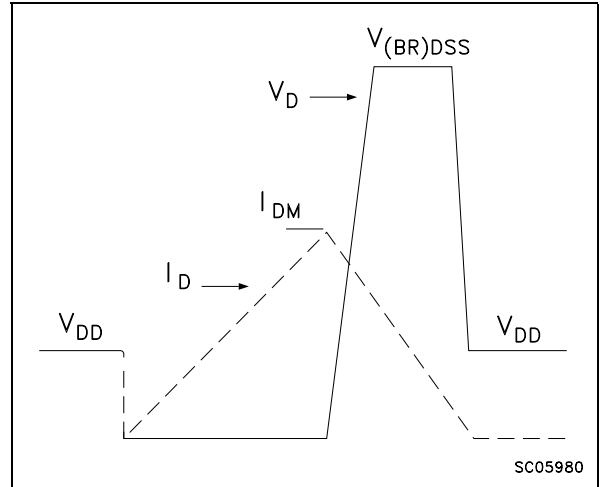
Figure 7: Gate Charge Test Circuit

Figure 5: Test Circuit For Inductive Load Switching and Diode Recovery Times
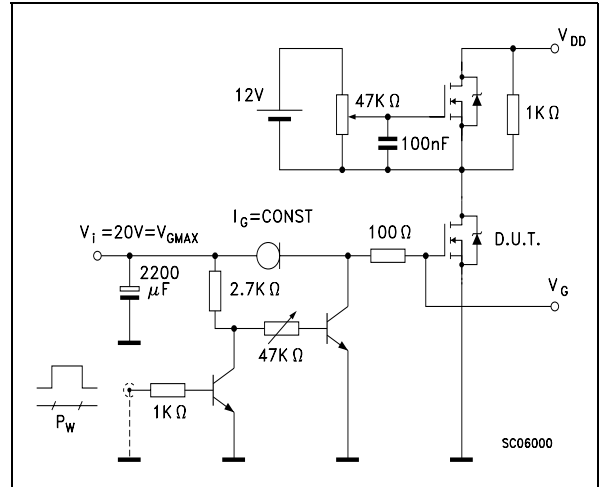
ISOTOP MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	11.8		12.2	0.466		0.480
B	8.9		9.1	0.350		0.358
C	1.95		2.05	0.076		0.080
D	0.75		0.85	0.029		0.033
E	12.6		12.8	0.496		0.503
F	25.15		25.5	0.990		1.003
G	31.5		31.7	1.240		1.248
H	4			0.157		
J	4.1		4.3	0.161		0.169
K	14.9		15.1	0.586		0.594
L	30.1		30.3	1.185		1.193
M	37.8		38.2	1.488		1.503
N	4			0.157		
O	7.8		8.2	0.307		0.322
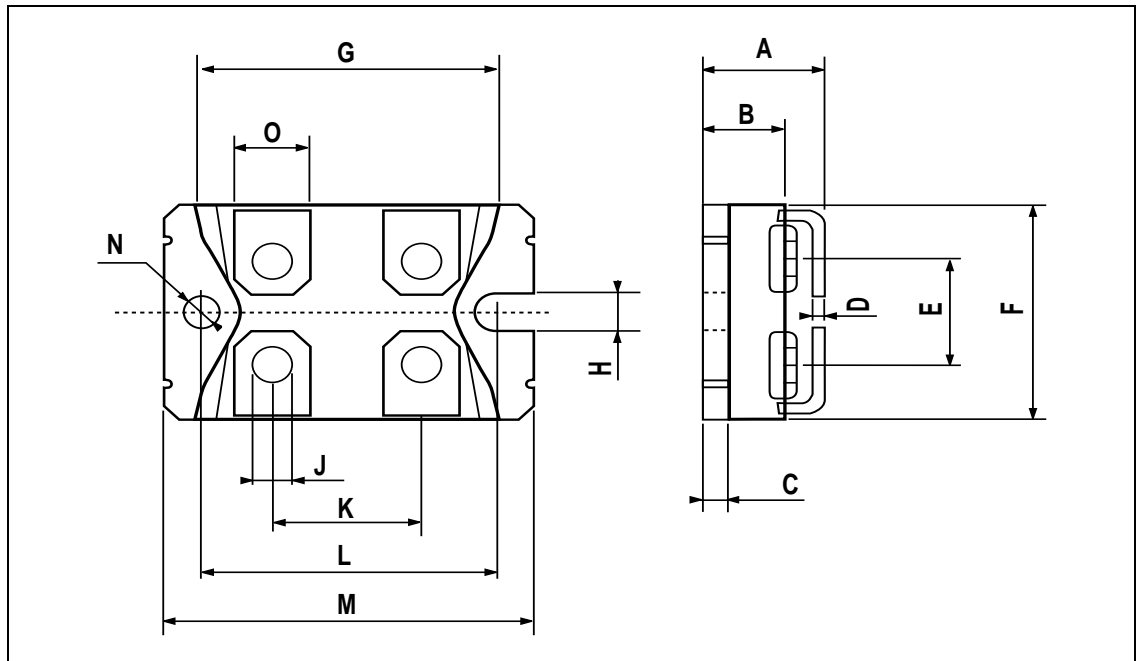
Table 10: Revision History

Date	Revision	Description of Changes
16-Jul-2004	1	First Release
15-Oct-2004	2	New value inserted in table 3. (V_{ISO})