

STY34NK80Z

N-CHANNEL 800V - 0.20Ω - 28A Max247 Zener-Protected SuperMESH[™] Power MOSFET

TARGET DATA

TYPE	V_{DSS}	R _{DS(on)}	ID	Pw
STY34NK80Z	800 V	< 0.24 Ω	28 A	450 W

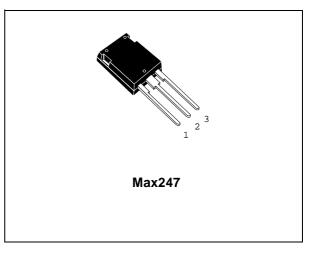
- TYPICAL $R_{DS}(on) = 0.20 \Omega$
- EXTREMELY HIGH dv/dt CAPABILITY
- 100% AVALANCHE TESTED
- GATE CHARGE MINIMIZED
- VERY LOW INTRINSIC CAPACITANCES
- VERY GOOD MANUFACTURING REPEATIBILITY

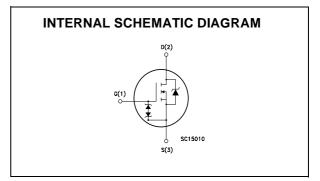
DESCRIPTION

The SuperMESH[™] series is obtained through an extreme optimization of ST's well established stripbased PowerMESH[™] layout. In addition to pushing on-resistance significantly down, special care is taken to ensure a very good dv/dt capability for the most demanding applications. Such series complements ST full range of high voltage MOSFETs including revolutionary MDmesh[™] products.

APPLICATIONS

- HIGH CURRENT, HIGH SPEED SWITCHING
- IDEAL FOR WELDING EQUIPMENT





ORDER CODES

PART	NUMBER	MARKING	PACKAGE	PACKAGING
STY3	4NK80Z	Y34NK80Z	Max247	TUBE

STY34NK80Z

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _{DS}	Drain-source Voltage (V _{GS} = 0)	800	V
V _{DGR}	Drain-gate Voltage ($R_{GS} = 20 \text{ k}\Omega$)	800	V
V _{GS}	Gate- source Voltage	± 30	V
I _D	Drain Current (continuous) at $T_C = 25^{\circ}C$	28	А
ID	Drain Current (continuous) at T _C = 100°C	17.5	А
I _{DM} (•)	Drain Current (pulsed)	112	А
P _{TOT}	Total Dissipation at $T_C = 25^{\circ}C$	450	W
	Derating Factor	3.6	W/°C
V _{ESD(G-S)}	Gate source ESD(HBM-C=100pF, R=1.5KΩ)	6	KV
dv/dt (1)	Peak Diode Recovery voltage slope	4.5	V/ns
T _j T _{stg}	Operating Junction Temperature Storage Temperature	- 65 to 150	°C

(•) Pulse width limited by safe operating area

(1) $I_{SD} \leq 28A$, di/dt $\leq 400A/\mu s$, $V_{DD} \leq V_{(BR)DSS}$, $T_j \leq T_{JMAX}$.

(*) Limited only by maximum temperature allowed

THERMAL DATA

Rthj-case	Thermal Resistance Junction-case Max	0.277	°C/W
Rthj-amb	Thermal Resistance Junction-ambient Max	30	°C/W
TI	Maximum Lead Temperature For Soldering Purpose	300	°C

AVALANCHE CHARACTERISTICS

Symbol	Parameter	Max Value	Unit
I _{AR}	Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by T _j max)	28	A
E _{AS}	Single Pulse Avalanche Energy (starting $T_j = 25 \text{ °C}$, $I_D = I_{AR}$, $V_{DD} = 35 \text{ V}$)	TBD	mJ

GATE-SOURCE ZENER DIODE

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
BV _{GSO}	Gate-Source Breakdown Voltage	lgs=± 1mA (Open Drain)	30			V

PROTECTION FEATURES OF GATE-TO-SOURCE ZENER DIODES

The built-in back-to-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.

ELECTRICAL CHARACTERISTICS (T_{CASE} =25°C UNLESS OTHERWISE SPECIFIED) ON/OFF

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
V _{(BR)DSS}	Drain-source Breakdown Voltage	$I_D = 1 \text{ mA}, V_{GS} = 0$	800			V
I _{DSS}	Zero Gate Voltage Drain Current (V _{GS} = 0)	V_{DS} = Max Rating V_{DS} = Max Rating, T _C = 125 °C			10 100	μA μA
IGSS	Gate-body Leakage Current (V _{DS} = 0)	$V_{GS} = \pm 20V$			±100	nA
V _{GS(th)}	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 100 \mu A$	3	3.75	4.5	V
R _{DS(on)}	Static Drain-source On Resistance	V _{GS} = 10V, I _D = 11 A		0.2	0.24	Ω

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
g _{fs} (1)	Forward Transconductance	V _{DS} = 15 V, I _D = 11 A		TBD		S
C _{iss} C _{oss} C _{rss}	Input Capacitance Output Capacitance Reverse Transfer Capacitance	V _{DS} = 25V, f = 1 MHz, V _{GS} = 0		8000 750 190		pF pF pF
C _{oss eq.} (3)	Equivalent Output Capacitance	$V_{GS} = 0V, V_{DS} = 0V$ to 720 V		TBD		pF
t _{d(on)} t _r t _{d(off)} t _f	Turn-on Delay Time Rise Time Turn-off Delay Time Fall Time	$\label{eq:VD} \begin{array}{l} V_{DD} = 450 \text{ V}, \text{ I}_{D} = 11 \text{ A} \\ \text{R}_{G} = 4.7\Omega \text{ V}_{\text{GS}} = 10 \text{ V} \\ \text{(Resistive Load see, Figure 3)} \end{array}$		TBD TBD TBD TBD		ns ns ns ns
Q _g Q _{gs} Q _{gd}	Total Gate Charge Gate-Source Charge Gate-Drain Charge	V _{DD} = 720 V, I _D = 28 A, V _{GS} = 10V		390 TBD TBD	546	nC nC nC

SOURCE DRAIN DIODE

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
I _{SD} I _{SDM} (2)	Source-drain Current Source-drain Current (pulsed)				28 112	A A
V _{SD} (1)	Forward On Voltage	I _{SD} = 28 A, V _{GS} = 0			TBD	V
t _{rr} Q _{rr} I _{RRM}	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	$I_{SD} = 28 \text{ A}, \text{ di/dt} = 100 \text{A/}\mu\text{s}$ $V_{DD} = 100 \text{ V}, \text{ T}_{\text{j}} = 25^{\circ}\text{C}$ (see test circuit, Figure 5)		TBD TBD TBD		ns μC Α
t _{rr} Q _{rr} I _{RRM}	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	$I_{SD} = 28 \text{ A}, \text{ di/dt} = 100 \text{A/}\mu\text{s}$ $V_{DD} = 100 \text{ V}, \text{ T}_{\text{j}} = 150^{\circ}\text{C}$ (see test circuit, Figure 5)		TBD TBD TBD		ns μC Α

Note: 1. Pulsed: Pulse duration = $300 \ \mu s$, duty cycle 1.5 %.

a local if use duration = 500 µs, auty cycle 1.5 %.
Pulse width limited by safe operating area.
C_{oss eq.} is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}.

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Fig. 1: Unclamped Inductive Load Test Circuit

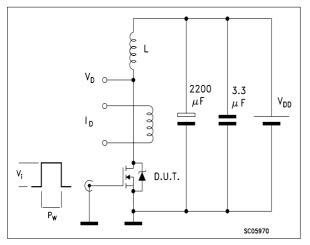


Fig. 3: Switching Times Test Circuit For Resistive Load

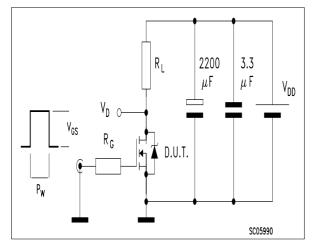


Fig. 5: Test Circuit For Inductive Load Switching And Diode Recovery Times

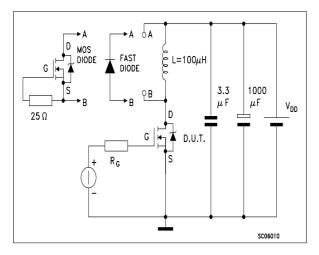


Fig. 2: Unclamped Inductive Waveform

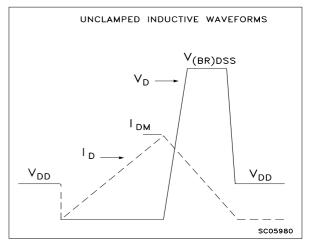
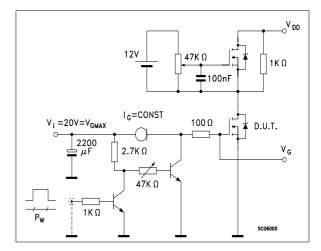
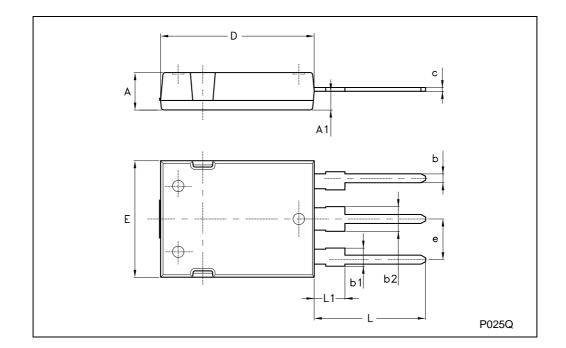


Fig. 4: Gate Charge test Circuit



DIM.		mm		inch			
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX	
А	4.70		5.30				
A1	2.20		2.60				
b	1.00		1.40				
b1	2.00		2.40				
b2	3.00		3.40				
с	0.40		0.80				
D	19.70		20.30				
е	5.35		5.55				
E	15.30		15.90				
L	14.20		15.20				

Max247 MECHANICAL DATA



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