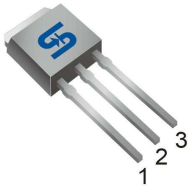
TAIWAN SEMICONDUCTOR

RoHS COMPLIANCE

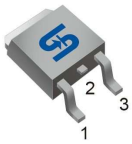
TSM5ND50

500V N-Channel Power MOSFET

TO-251 (IPAK)



TO-252 (DPAK)



Pin Definition:
1. Gate
2. Drain
3. Source

PRODUCT SUMMARY

V_{DS} (V)	$R_{DS(on)}$(Ω)	I_D (A)
500	1.5 @ V_{GS}=10V	2.2

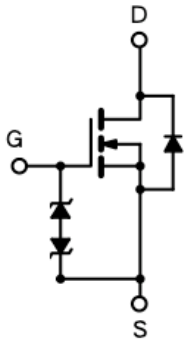
General Description

The TSM5ND50 N-Channel enhancement mode Power MOSFET is produced by planar stripe DMOS technology. This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency switch mode power supply, power factor correction, electronic lamp ballast based on half bridge.

Features

- Low gate charge typical @ 20nC
- Low Crss typical @ 17pF
- Fast Switching
- Improved dv/dt capability
- ESD Protection

Block Diagram



N-Channel MOSFET

Ordering Information

Part No.	Package	Packing
TSM5ND50CP ROG	TO-252	2,500pcs / 13" Reel
TSM5ND50CH C5G	TO-251	75pcs / Tube

Note: "G" denotes for Halogen Free

Absolute Maximum Rating (Ta = 25°C unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	500	V
Gate-Source Voltage	V_{GS}	±30	V
Continuous Drain Current	I_D	4.4	A
Pulsed Drain Current	I_{DM}	17.6	A
Continuous Source Current (Diode Conduction)	I_S	4.4	A
Peak Diode Recovery (Note 2)	dv/dt	4.5	V/ns
Single Pulse Drain to Source Avalanche Energy (Note 3)	E_{AS}	130	mJ
Total Power Dissipation @Ta = 25°C	P_{DTOT}	70	W
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 to +150	°C

Thermal Performance

Parameter	Symbol	Limit	Unit
Thermal Resistance - Junction to Case	$R\Theta_{JC}$	1.78	°C/W
Thermal Resistance - Junction to Ambient	$R\Theta_{JA}$	62.5	°C/W

Notes: Surface mounted on FR4 board t ≤ 10sec

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Electrical Specifications (Ta = 25°C unless otherwise noted)

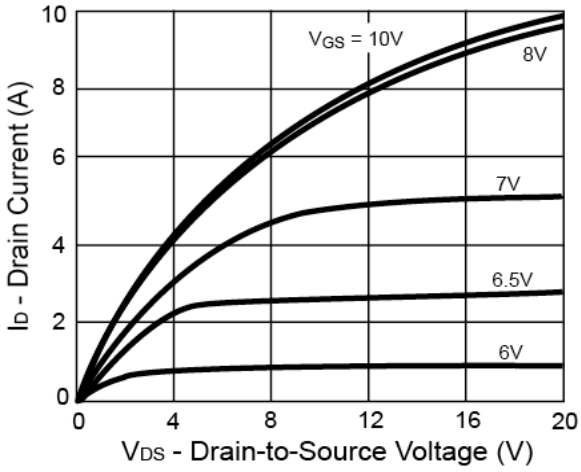
Parameter	Conditions	Symbol	Min	Typ	Max	Unit
Static						
Drain-Source Breakdown Voltage	V_{GS} = 0V, I_D = 250uA	BV_{DSS}	500	--	--	V
Drain-Source On-State Resistance	V_{GS} = 10V, I_D = 2.2A	$R_{DS(ON)}$	--	1.2	1.5	Ω
Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 50uA	$V_{GS(TH)}$	3.0	--	4.8	V
Zero Gate Voltage Drain Current	V_{DS} = 500V, V_{GS} = 0V	I_{DSS}	--	--	1	uA
Gate Body Leakage	V_{GS} = ±20V, V_{DS} = 0V	I_{GSS}	--	--	±10	uA
Forward Transconductance	V_{DS} = 15V, I_D = 2.2A	g_{fs}	--	3.1	--	S
Dynamic [b]						
Total Gate Charge	V_{DS} = 250V, I_D = 4.4A, V_{GS} = 10V	Q_g	--	20	--	nC
Gate-Source Charge		Q_{gs}	--	4	--	
Gate-Drain Charge		Q_{gd}	--	10	--	
Input Capacitance	V_{DS} = 25V, V_{GS} = 0V, f = 1.0MHz	C_{iss}	--	535	--	pF
Output Capacitance		C_{oss}	--	75	--	
Reverse Transfer Capacitance		C_{rss}	--	17	--	
Switching [c]						
Turn-On Delay Time	V_{GS} = 10V, I_D = 4.4A, V_{DD} = 250V, R_G = 25Ω	$t_{d(on)}$	--	21.6	--	nS
Turn-On Rise Time		t_r	--	11.7	--	
Turn-Off Delay Time		$t_{d(off)}$	--	14.5	--	
Turn-Off Fall Time		t_f	--	4.5	--	
Source Drain Diode						
Source-drain Current		I_{SD}	--	--	4.4	A
Diode Forward Voltage	I_S = 4.4A, V_{GS} = 0V	V_{SD}	--	0.82	1.2	V
Reverse Recovery Time	V_{DD} = 30V, I_{SD} = 4.4A, dI_F/dt = 100A/us. T_J=150ºC	t_{rr}	--	310	--	nS
Reverse Recovery Charge		Q_{rr}	--	1425	--	nC
Reverse Recovery Current		I_{RRM}	--	9.2	--	A

Notes:

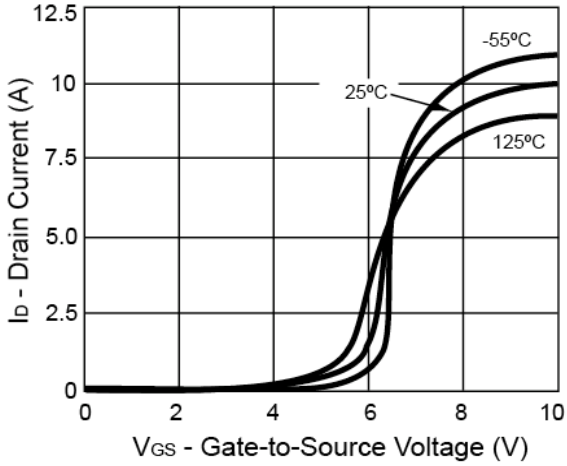
1. Pulse test: pulse width ≤300uS, duty cycle ≤2%
2. I_{SD}<4.4A, di/dt<200A/us, VDD<BV_{DSS}
3. Starting V_{DD} = 50V, I_{AS}=4.4A, T_J=25ºC
4. For design reference only, not subject to production testing.
5. Switching time is essentially independent of operating temperature.

Electrical Characteristics Curve (Ta = 25°C, unless otherwise noted)

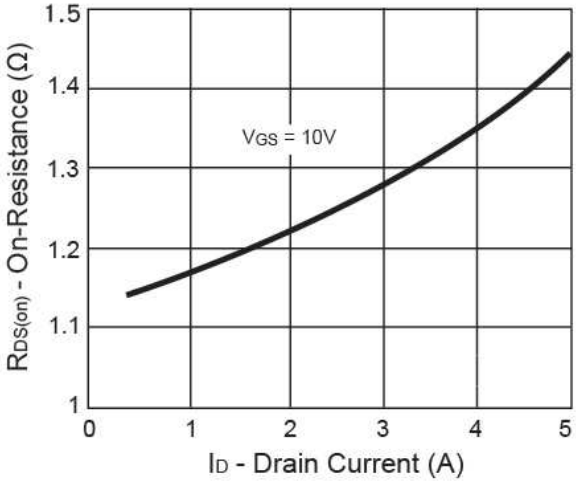
Output Characteristics



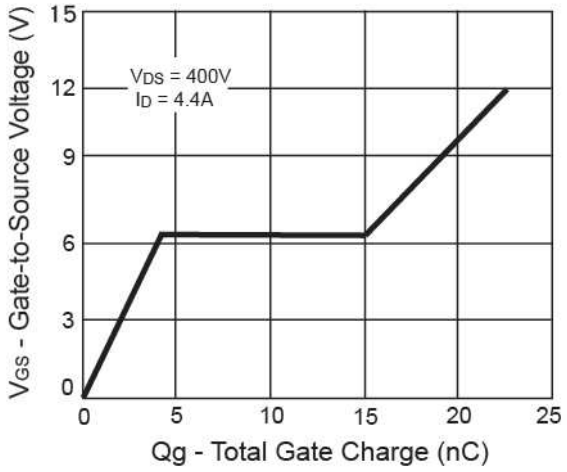
Transfer Characteristics



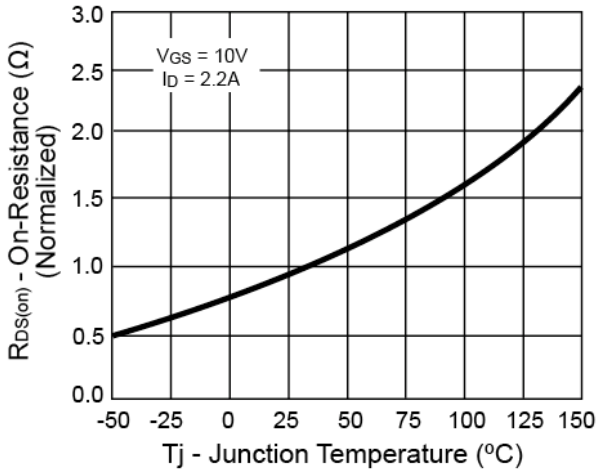
On-Resistance vs. Drain Current



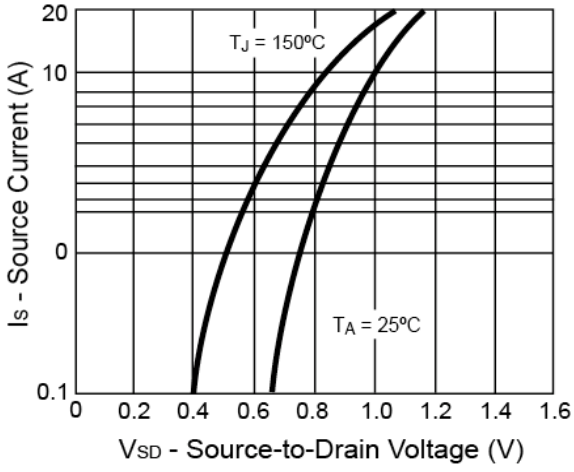
Gate Charge



On-Resistance vs. Junction Temperature



Source-Drain Diode Forward Voltage



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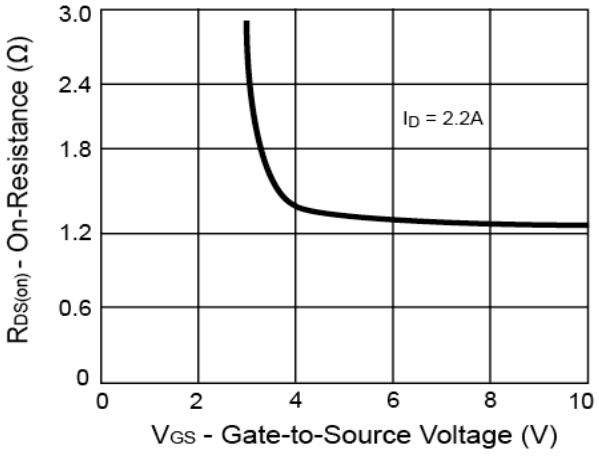
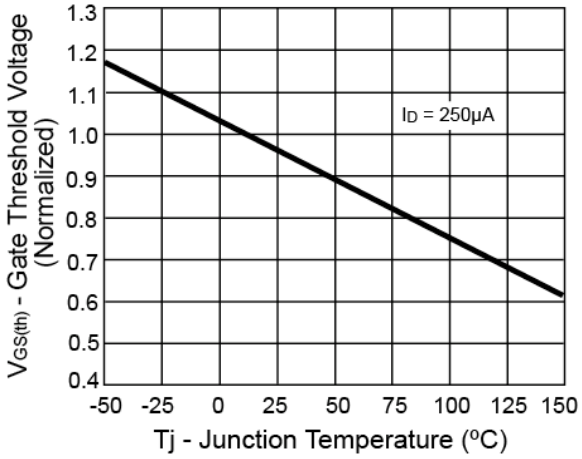
Electrical Characteristics Curve (Ta = 25°C, unless otherwise noted)

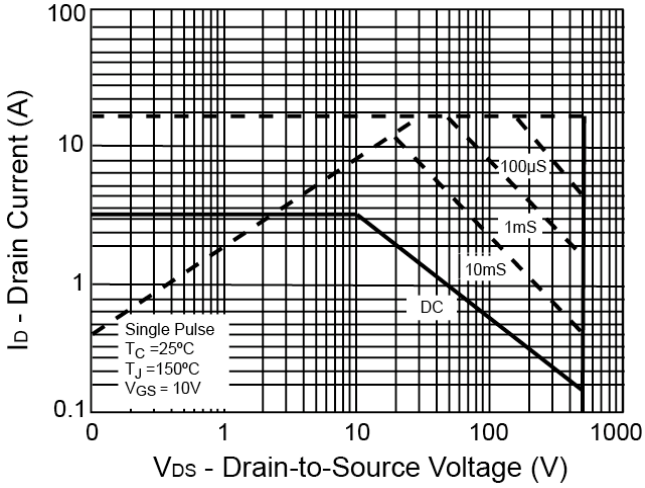
On-Resistance vs. Gate-Source Voltage



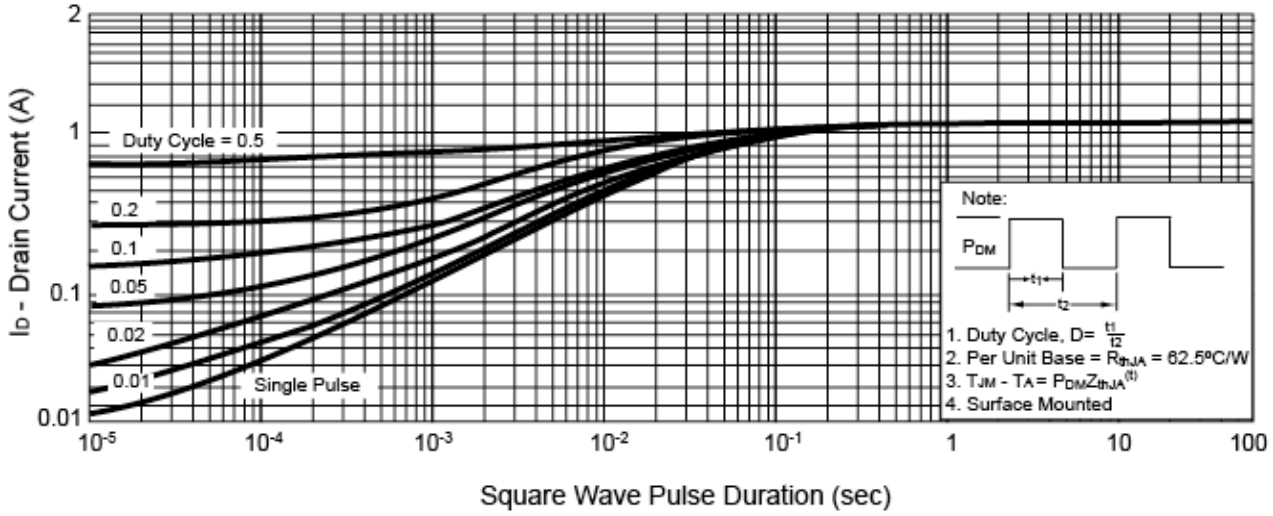
Threshold Voltage



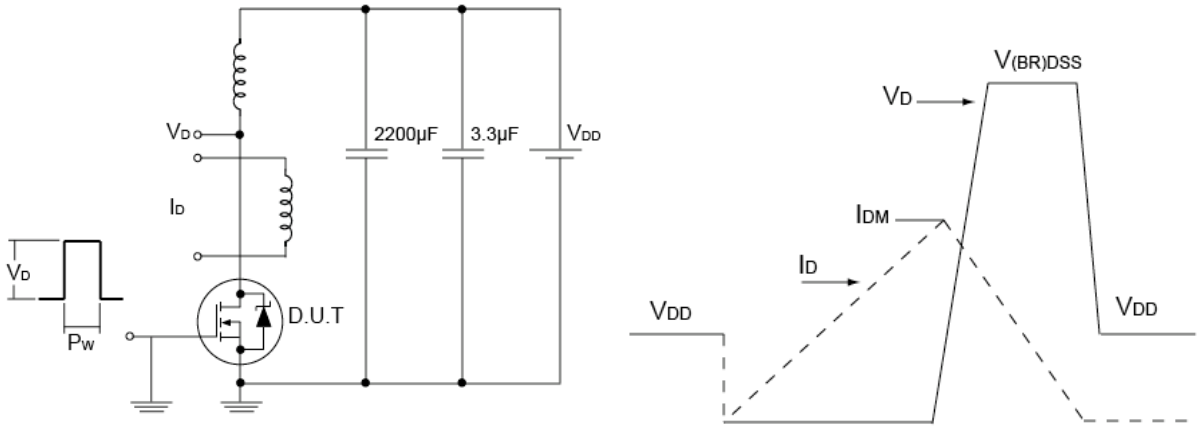
Maximum Safe Operating Area



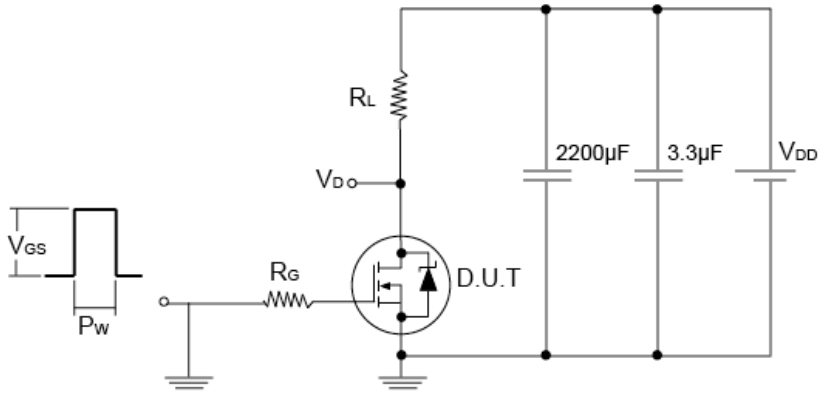
Normalized Thermal Transient Impedance, Junction-to-Ambient



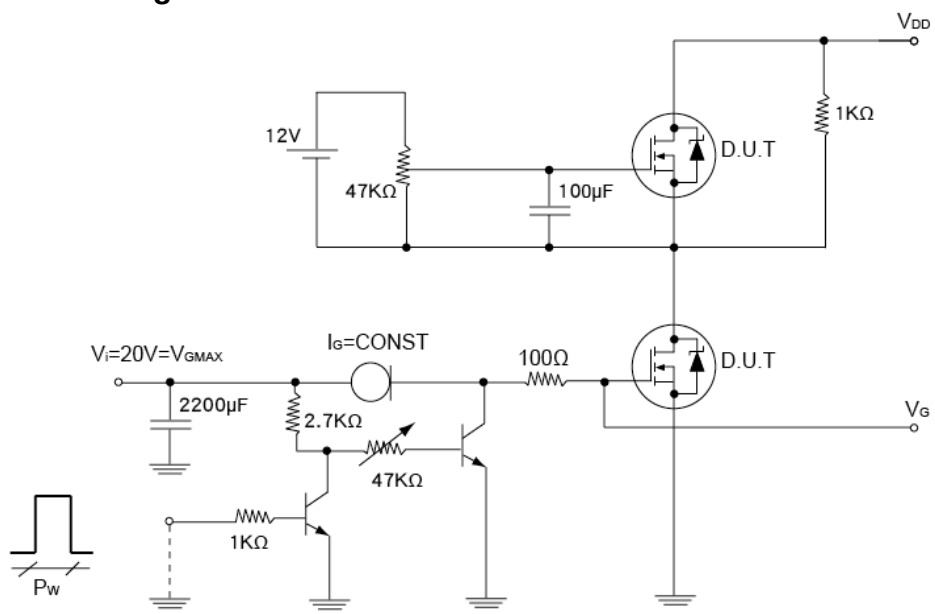
Unclamped Inductive Load Test Circuit and Waveform



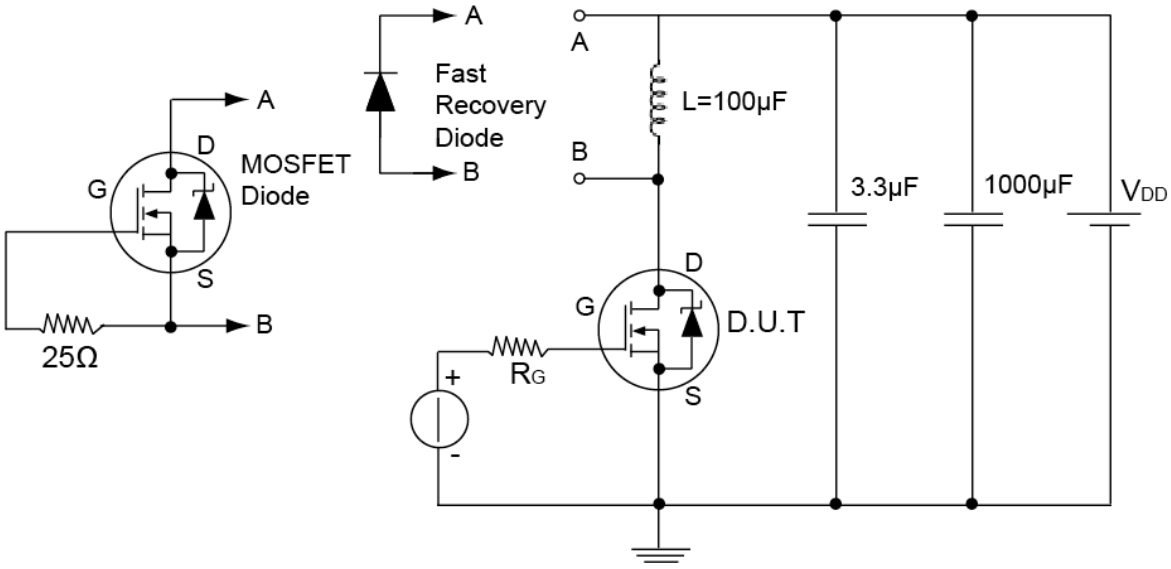
Switching Time Test Circuits for Resistive Load



Gate Charge Test Circuit



Test Circuit for Inductive Load Switching and Diode Recovery Times



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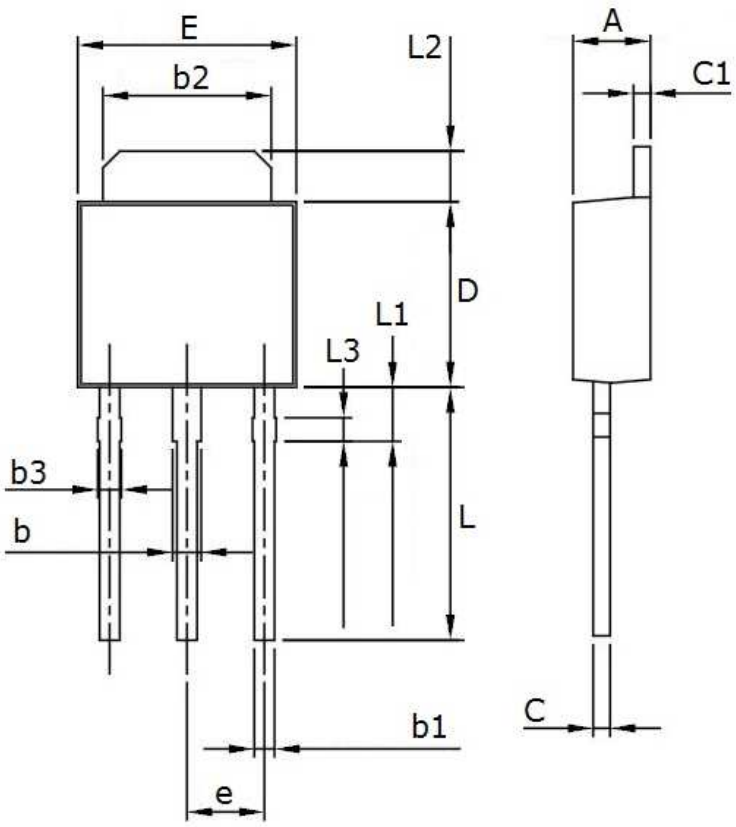
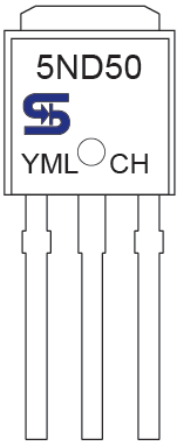
TO-251 Mechanical Drawing



TO-251 DIMENSION				
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.10	2.50	0.083	0.098
b	0.65	1.05	0.026	0.041
b1	0.58	0.62	0.023	0.024
b2	4.80	5.20	0.189	0.205
b3	0.68	0.72	0.027	0.028
C	0.35	0.65	0.014	0.026
C1	0.40	0.60	0.016	0.024
D	5.30	5.70	0.209	0.224
E	6.30	6.70	0.248	0.264
e	2.30 BSC		0.09 BSC	
L	7.00	8.00	0.276	0.315
L1	1.40	1.80	0.055	0.071
L2	1.30	1.70	0.051	0.067
L3	0.50	0.90	0.020	0.035

Marking Diagram

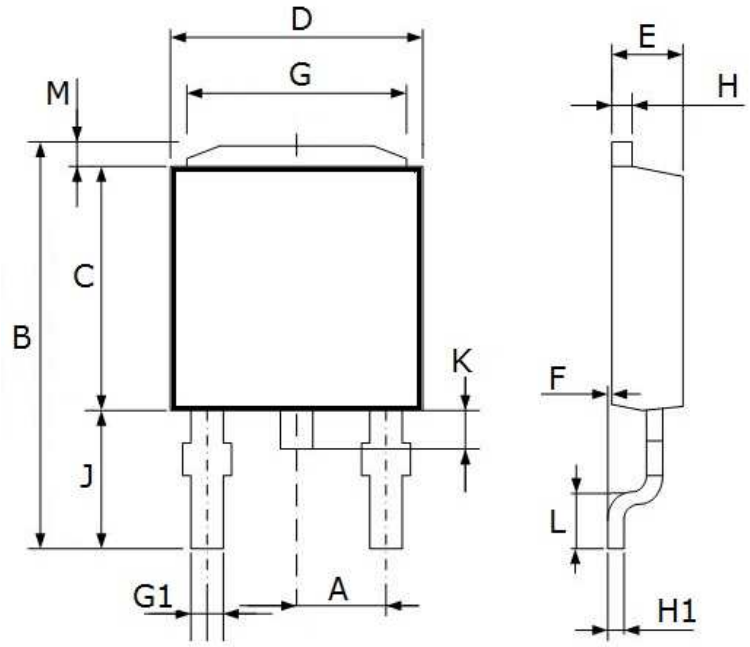


Y = Year Code

M = Month Code for Halogen Free Product
(**O**=Jan, **P**=Feb, **Q**=Mar, **R**=Apl, **S**=May, **T**=Jun, **U**=Jul, **V**=Aug, **W**=Sep, **X**=Oct, **Y**=Nov, **Z**=Dec)

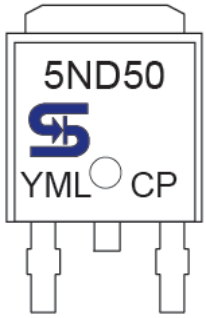
L = Lot Code

TO-252 Mechanical Drawing



TO-252 DIMENSION				
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.30 BSC		0.090 BSC	
B	10.20	10.80	0.402	0.425
C	5.30	5.70	0.209	0.224
D	6.30	6.70	0.248	0.264
E	2.10	2.50	0.083	0.098
F	0.00	0.20	0.000	0.008
G	4.80	5.20	0.189	0.205
G1	0.40	0.80	0.016	0.031
H	0.40	0.60	0.016	0.024
H1	0.35	0.65	0.014	0.026
J	3.35	3.65	0.132	0.144
K	0.50	1.10	0.020	0.043
L	0.90	1.50	0.035	0.059
M	1.30	1.70	0.051	0.067

Marking Diagram



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