DATA SHEET

74ABT16501A

18-bit universal bus transceiver (3-State)

Philips
Semiconductors

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18-bit universal bus transceiver (3-State)

74ABT16501A

FEATURES

- 18-bit bidirectional bus interface
- 3-State buffers
- Output capability: +64 mA/–32 mA
- TTL input and output switching levels
- Live insertion/extraction permitted
- Power-up reset
- Power-up 3-State
- Positive edge-triggered clock inputs
- Latch-up protection exceeds 500mA per JEDEC Std 17
- ESD protection exceeds 2000 V per MIL STD 883 Method 3015 and 200 V per Machine Model
- Flexible operation permits 18 embedded D-type latches or flip-flops to operate in clocked, transparent, and latched modes.

DESCRIPTION

The 74ABT16501A high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

This device is an 18-bit universal transceiver featuring non-inverting 3-State bus compatible outputs in both send and receive directions. Data flow in each direction is controlled by output enable (OEAB and $\overline{\text{OEBA}}$), latch enable (LEAB and LEBA), and clock (CPAB and CPBA) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is HIGH. When LEAB is LOW, the A data is latched if CPAB is held at a HIGH or LOW logic level. If LEAB is LOW, the A-bus data is stored in the latch/flip-flop on the LOW-to-HIGH transition of CPAB. When OEAB is HIGH, the outputs are active. When OEAB is LOW, the outputs are in the high-impedance state.

Data flow for B-to-A is similar to that of A-to-B but uses $\overline{\text{OEBA}}$, LEBA and CPBA. The output enables are complimentary (OEAB is Active-HIGH, and $\overline{\text{OEBA}}$ is Active-LOW).

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25 °C; GND = 0 V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay An to Bn or Bn to An	C_L = 50 pF; V_{CC} = 5 V	2.2 1.8	ns
C_{IN}	Input capacitance (Control pins)	V_I = 0 V or V_{CC}	3	pF
$C_{I/O}$	I/O pin capacitance	Outputs disabled; $V_{I/O}$ = 0 V or V_{CC}	7	pF
I_{CCZ}	Quiescent supply current	Outputs disabled; V_{CC} = 5.5 V	500	µA
I_{CCL}		Outputs LOW; V_{CC} = 5.5 V	9	mA

ORDERING INFORMATION

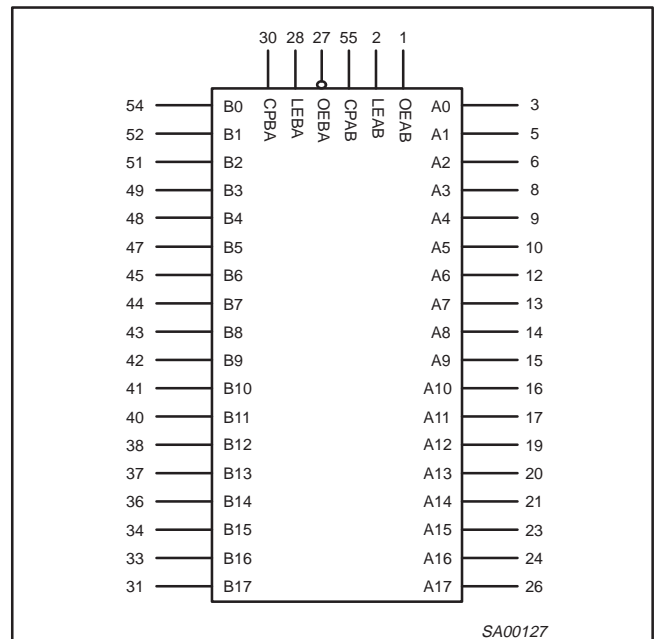| PACKAGES	TEMPERATURE RANGE	ORDER CODE	DWG NUMBER
56-Pin Plastic SSOP Type III	−40 °C to +85 °C	74ABT16501ADL	SOT371-1
56-Pin Plastic TSSOP Type II	−40 °C to +85 °C	74ABT16501ADGG	SOT364-1

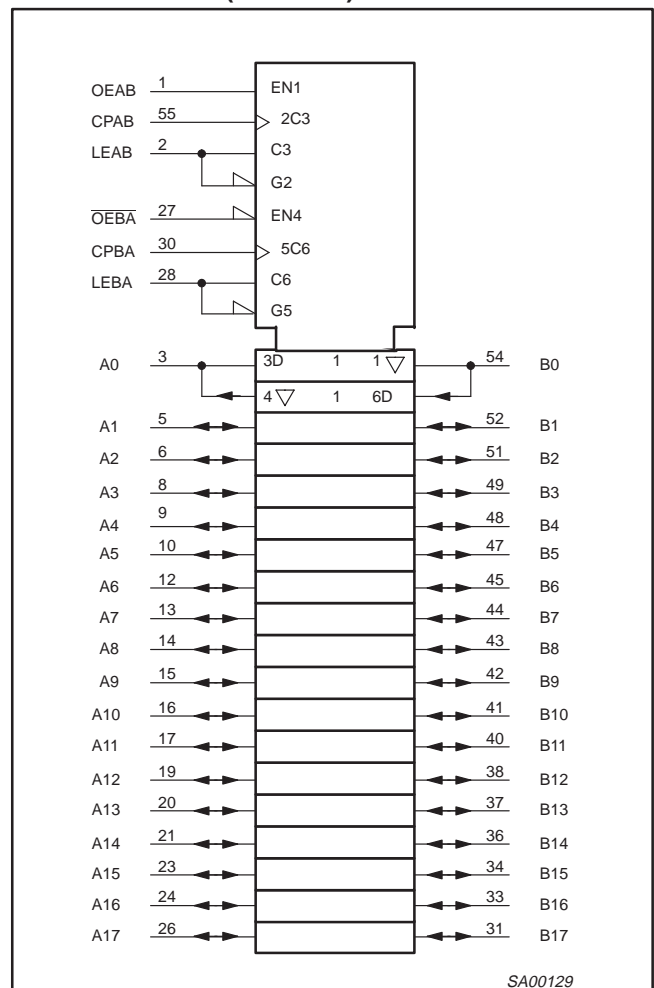## 18-bit universal bus transceiver (3-State)

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PIN CONFIGURATION

OEAB	1		56	GND
LEAB	2		55	CPAB
A0	3		54	B0
GND	4		53	GND
A1	5		52	B1
A2	6		51	B2
V_{CC}	7		50	V_{CC}
A3	8		49	B3
A4	9		48	B4
A5	10		47	B5
GND	11		46	GND
A6	12		45	B6
A7	13		44	B7
A8	14		43	B8
A9	15		42	B9
A10	16		41	B10
A11	17		40	B11
GND	18		39	GND
A12	19		38	B12
A13	20		37	B13
A14	21		36	B14
V_{CC}	22		35	V_{CC}
A15	23		34	B15
A16	24		33	B16
GND	25		32	GND
A17	26		31	B17
$\overline{OEBA}$	27		30	CPBA
LEBA	28		29	GND

SA00128

LOGIC SYMBOL

SA00127
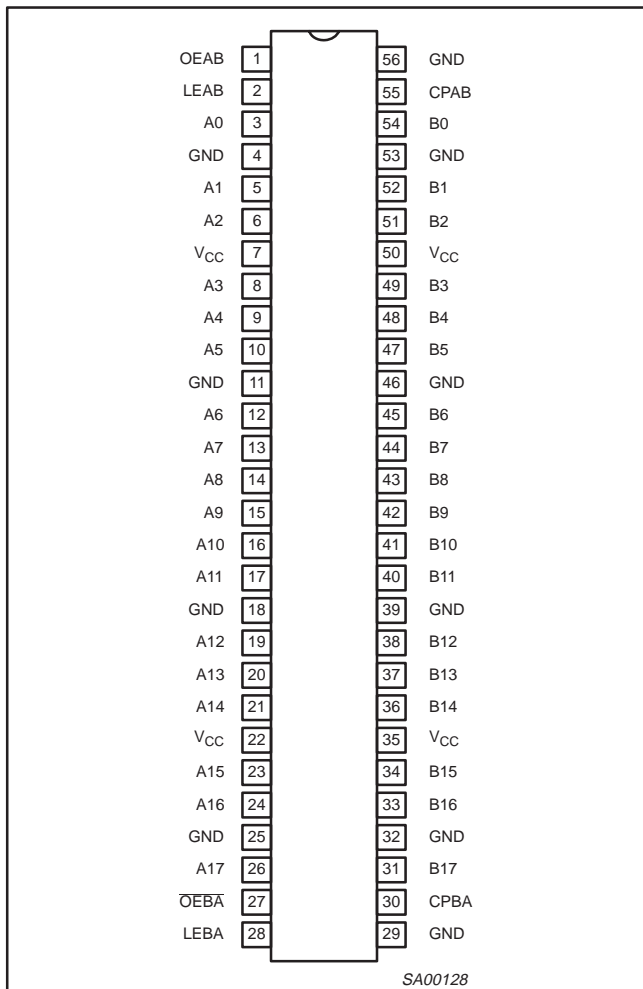
LOGIC SYMBOL (IEEE/IEC)

SA00129

PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1	OEAB	A-to-B Output enable input
27	$\overline{OEBA}$	B-to-A Output enable input (Active-LOW)
2, 28	LEAB/LEBA	A-to-B/B-to-A Latch enable input
55, 30	CPAB/CPBA	A-to-B/B-to-A Clock input (active rising edge)
3, 5, 6, 8, 9, 10, 12, 13, 14, 15, 16, 17, 19, 20, 21, 23, 24, 26	A0-A17	Data inputs/outputs (A side)
54, 52, 51, 49, 48, 47, 45, 44, 43, 42, 41, 40, 38, 37, 36, 34, 33, 31	B0-B17	Data inputs/outputs (B side)
4, 11, 18, 25, 32, 39, 46, 53	GND	Ground (0 V)
7, 22, 35, 50	V_{CC}	Positive supply voltage

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FUNCTION TABLE

INPUTS				Internal Registers	OUTPUTS	OPERATING MODE
OEAB	LEAB	CPAB	An		Bn	
L	H	X	X	X	Z	Disabled
L	↓	X	h	H	Z	Disabled, Latch data
L	↓	X	l	L	Z	
L	L	H or L	X	NC	Z	Disabled, Hold data
L	L	↑	h	H	Z	Disabled, Clock data
L	L	↑	l	L	Z	
H	H	X	H	H	H	Transparent
H	H	X	L	L	L	
H	↓	X	h	H	H	Latch data & display
H	↓	X	l	L	L	
H	L	↑	h	H	H	Clock data & display
H	L	↑	l	L	L	
H	L	H or L	X	H	H	Hold data & display
H	L	H or L	X	L	L	

NOTE: A-to-B data flow is shown; B-to-A flow is similar but uses $\overline{OEBA}$, LEBA, and CPBA.

H = High voltage level
h = High voltage level one set-up time prior to the Enable or Clock transition
L = Low voltage level
l   = Low voltage level one set-up time prior to the Enable or Clock transition
NC= No Change
X = Don't care
Z = High Impedance "off" state
↓ = HIGH-to-LOW Enable or Clock transition
↑ = LOW-to-HIGH Clock transition

LOGIC DIAGRAM

OEAB 1

CLKAB 55

LEAB 2

LEBA 28

CLKBA 30

$\overline{OEBA}$ 27

A1 3

ID
C1
CLK

ID
C1
CLK

54 B1

To 17 other channels

SW00235

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ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		−0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$ V	−18	mA
V_I	DC input voltage[3]		−1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$ V	−50	mA
V_{OUT}	DC output voltage[3]	Output in Off or HIGH state	−0.5 to +5.5	V
I_{OUT}	DC output current	Output in LOW state	128	mA
		Output in HIGH state	−64	
T_{stg}	Storage temperature range		−65 to +150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150 °C.
3. The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	HIGH-level input voltage	2.0	–	V
V_{IL}	Input voltage	–	0.8	V
I_{OH}	HIGH-level output current	–	−32	mA
I_{OL}	LOW-level output current	–	64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate; Outputs enabled	–	10	ns/V
T_{amb}	Operating free-air temperature range	−40	+85	°C

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DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS					UNIT
				T_{amb} = +25 °C			T_{amb} = −40 °C to +85 °C		
				MIN	TYP	MAX	MIN	MAX	
V_{IK}	Input clamp voltage	V_{CC} = 4.5 V; I_{IK} = −18 mA		–	−0.8	−1.2	–	−1.2	V
V_{OH}	High-level output voltage	V_{CC} = 4.5 V; I_{OH} = −3 mA; V_I = V_{IL} or V_{IH}		2.5	2.9	–	2.5	–	V
		V_{CC} = 5.0 V; I_{OH} = −3 mA; V_I = V_{IL} or V_{IH}		3.0	4.0	–	3.0	–	V
		V_{CC} = 4.5 V; I_{OH} = −32 mA; V_I = V_{IL} or V_{IH}		2.0	2.4	–	2.0	–	V
V_{OL}	Low-level output voltage	V_{CC} = 4.5 V; I_{OL} = 64 mA; V_I = V_{IL} or V_{IH}		–	0.35	0.55	–	0.55	V
V_{RST}	Power-up output voltage[3]	V_{CC} = 5.5 V; I_O = 1 mA; V_I = GND or V_{CC}		–	0.13	0.55	–	0.55	V
I_I	Input leakage current	V_{CC} = 5.5 V; V_I = GND or 5.5 V	Control pins	–	± 0.01	±1.0	–	±1.0	µA
I_{OFF}	Power-off leakage current	V_{CC} = 0.0 V; V_O or V_I ≤ 4.5 V		–	± 2	±100	–	±100	µA
$I_{PU/PD}$	Power-up/down 3-State output current[4]	V_{CC} = 2.1 V; V_O = 0.0 V or V_{CC}; V_I = GND or V_{CC}; V_{OE} = Don't care		–	± 2	±50	–	±50	µA
I_{IH} + I_{OZH}	3-State output High current	V_{CC} = 5.5 V; V_O = 5.5 V; V_I = V_{IL} or V_{IH}		–	1.0	10	–	10	µA
I_{IL} + I_{OZL}	3-State output Low current	V_{CC} = 5.5 V; V_O = 0.0 V; V_I = V_{IL} or V_{IH}		–	−1.0	−10	–	−10	µA
I_{CEX}	Output High leakage current	V_{CC} = 5.5 V; V_O = 5.5 V; V_I = GND or V_{CC}		–	2.0	50	–	50	µA
I_O	Output current[1]	V_{CC} = 5.5 V; V_O = 2.5 V		−50	−80	−180	−50	−180	mA
I_{CCH}	Quiescent supply current	V_{CC} = 5.5 V; Outputs HIGH, V_I = GND or V_{CC}		–	0.5	2	–	2	mA
I_{CCL}		V_{CC} = 5.5 V; Outputs LOW, V_I = GND or V_{CC}		–	9	19	–	19	mA
I_{CCZ}		V_{CC} = 5.5 V; Outputs 3-State; V_I = GND or V_{CC}		–	0.5	2	–	2	mA
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 5.5 V; one input at 3.4 V, other inputs at V_{CC} or GND		–	5.0	50	–	50	µA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4 V.
3. For valid test results, data must not be loaded into the flip-flops (or latches) after applying the power.
4. This parameter is valid for any V_{CC} between 0 V and 2.1 V, with a transition time of up to 10 msec. From V_{CC} = 2.1 V to V_{CC} = 5 V ± 10% a transition time of up to 100 µsec is permitted.

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AC CHARACTERISTICS
GND = 0 V, t_R = t_F = 2.5 ns, C_L = 50 pF, R_L = 500 Ω

| SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T_{amb} = +25 °C V_{CC} = +5.0 V			T_{amb} = −40 °C to +85 °C V_{CC} = +5.0 V ±0.5 V		
			MIN	TYP	MAX	MIN	MAX	
f_{max}	Maximum clock frequency	1	150	225		150		MHz
t_{PLH} t_{PHL}	Propagation delay An to Bn or Bn to An	2	1.0 1.0	2.2 1.8	3.0 2.5	1.0 1.0	3.5 3.0	ns
t_{PLH} t_{PHL}	Propagation delay LEAB to Bn or LEBA to An	3	1.5 1.4	3.2 2.9	4.3 3.8	1.5 1.4	5.0 4.2	ns
t_{PLH} t_{PHL}	Propagation delay CPAB to Bn or CPBA to An	1	1.6 1.4	3.5 2.9	4.5 3.8	1.6 1.4	5.0 4.2	ns
t_{PZH} t_{PZL}	Output enable time to HIGH and LOW level	5 6	1.1 1.0	3.0 2.4	4.0 3.4	1.1 1.0	4.7 3.9	ns
t_{PHZ} t_{PLZ}	Output disable time from HIGH and LOW level	5 6	1.3 1.0	3.3 2.4	4.3 3.4	1.3 1.0	5.3 3.9	ns

AC SETUP REQUIREMENTS
GND = 0V, t_R = t_F = 2.5ns, C_L = 50pF, R_L = 500Ω

SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			T_{amb} = +25 °C V_{CC} = +5.0 V		T_{amb} = −40 °C to +85 °C V_{CC} = +5.0 V ±0.5 V	
			MIN	TYP	MIN	
$t_s(H)$ $t_s(L)$	Setup time, HIGH or LOW An to CPAB or Bn to CPBA	4	2.0 2.0	0.5 0.5	2.0 2.0	ns
$t_h(H)$ $t_h(L)$	Hold time, HIGH or LOW An to CPAB or Bn to CPBA	4	0.7 0.7	−0.5 −0.5	0.7 0.7	ns
$t_s(H)$ $t_s(L)$	Setup time, HIGH or LOW An to LEAB or Bn to LEBA	4	2.0 2.0	0.5 0.4	2.0 2.0	ns
$t_h(H)$ $t_h(L)$	Hold time HIGH or LOW An to LEAB or Bn to LEBA	4	0.7 0.7	−0.4 −0.5	0.7 0.7	ns
t_w	Pulse width, HIGH or LOW CPAB or CPBA	1	3	1.9	3	ns
$t_w(H)$	Pulse width, HIGH LEAB or LEBA	3	3	1.2	3	ns

AC WAVEFORMS
V_M = 1.5 V, V_{IN} = GND to 3.0 V
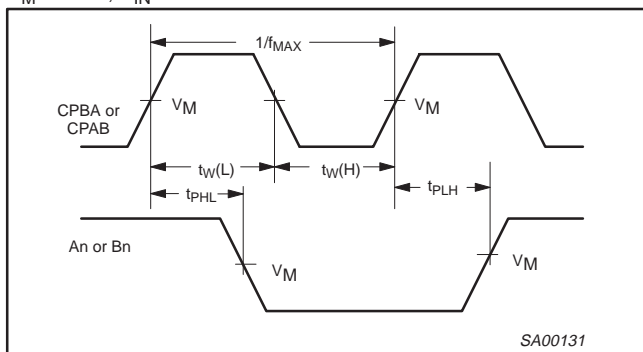
Waveform 1. Propagation Delay, Clock Input to Output, Clock Pulse Width, and Maximum Clock Frequency
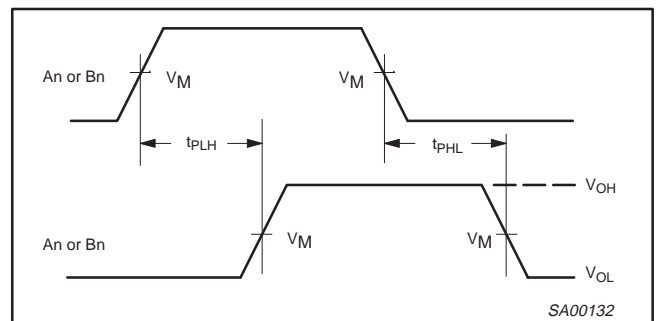
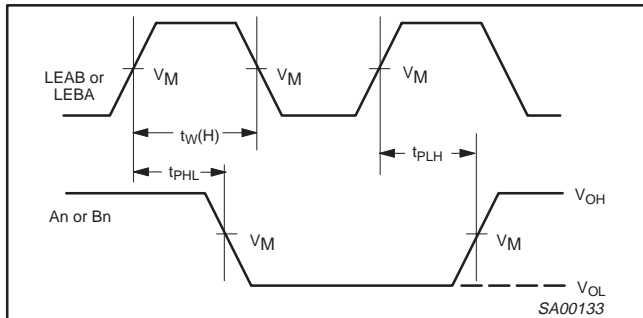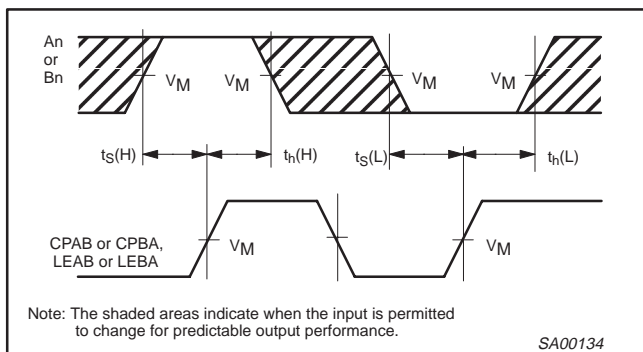**Waveform 2. Propagation Delay, Transparent Mode**

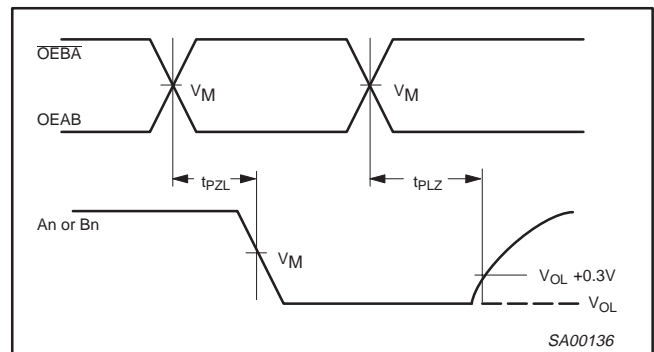## AC WAVEFORMS (Continued)

$V_M = 1.5$ V, $V_{IN} = $ GND to 3.0 V

**Waveform 3. Propagation Delay, Enable to Output,
and Enable Pulse Width**
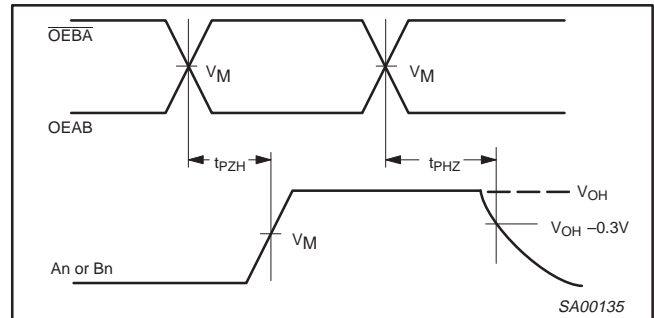
**Waveform 5. 3-State Output Enable Time to High Level
and Output Disable Time from High Level**

Note: The shaded areas indicate when the input is permitted
to change for predictable output performance.

Waveform 4. Data Set-up and Hold Times

**Waveform 6. 3-State Output Enable Time to Low Level
and Output Disable Time from Low Level**

TEST CIRCUIT AND WAVEFORMS

Test Circuit for 3-State Outputs

$V_M = 1.5V$
Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance;
see AC CHARACTERISTICS for value.

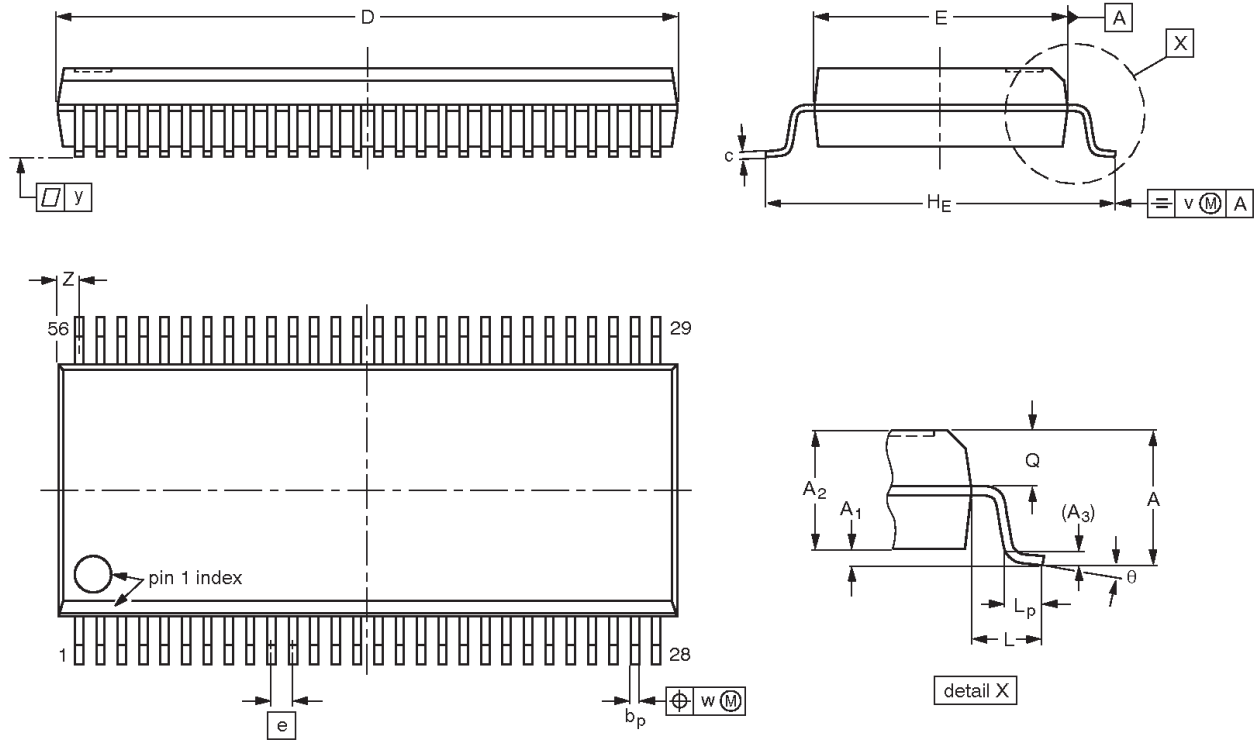R_T = Termination resistance should be equal to Z_{OUT} of
pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74ABT/H16	3.0V	1MHz	500ns	2.5ns	2.5ns

SA00018

SSOP56: plastic shrink small outline package; 56 leads; body width 7.5 mm

SOT371-1

pin 1 index

detail X

0   5   10 mm

scale

DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.8	0.4 0.2	2.35 2.20	0.25	0.3 0.2	0.22 0.13	18.55 18.30	7.6 7.4	0.635	10.4 10.1	1.4	1.0 0.6	1.2 1.0	0.25	0.18	0.1	0.85 0.40	8° 0°

Note

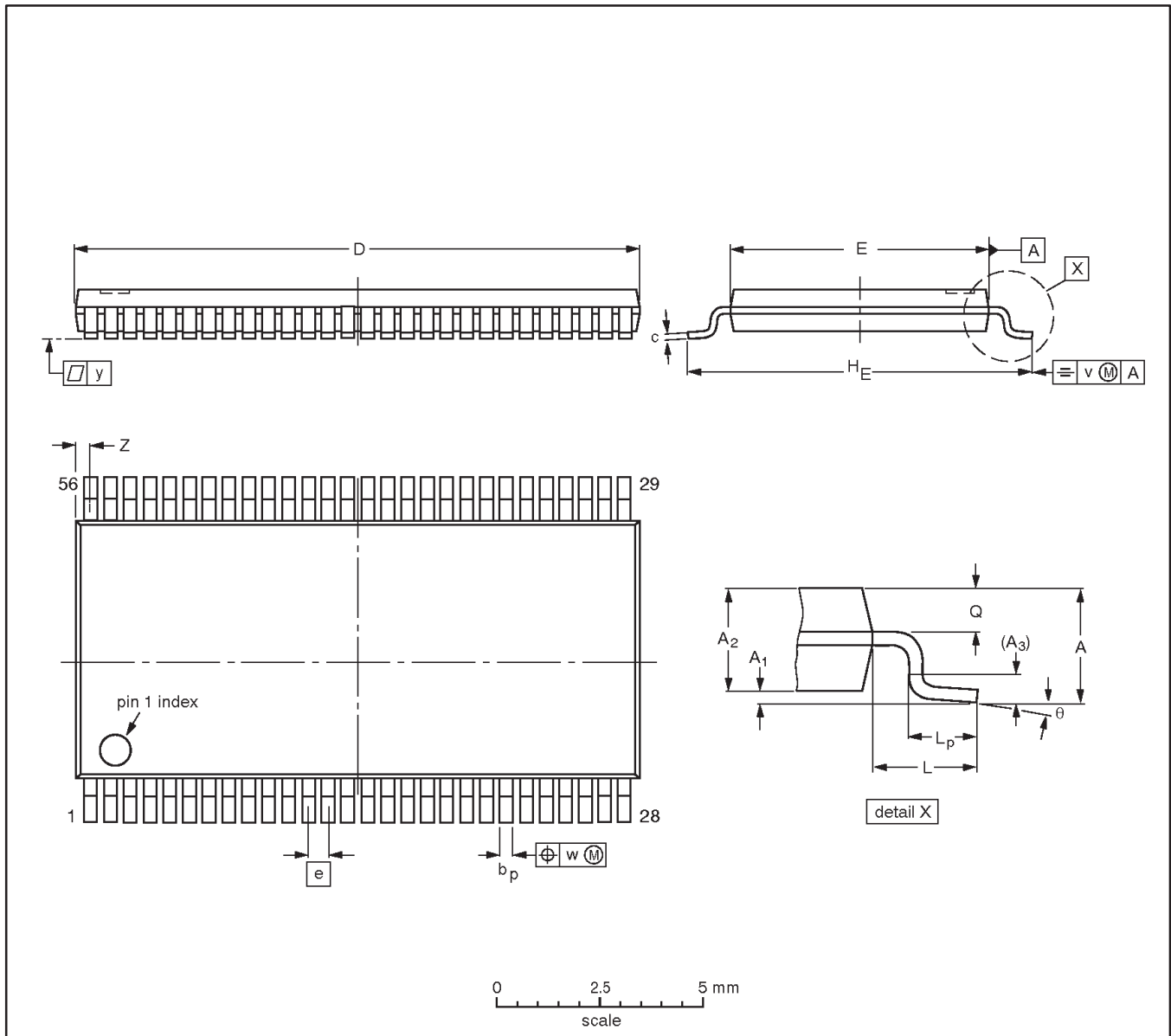1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT371-1		MO-118				~~95-02-04~~ 99-12-27

TSSOP56:   plastic thin shrink small outline package; 56 leads; body width 6.1 mm   **SOT364-1**

pin 1 index

detail X

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0        2.5      5 mm
scale
```

DIMENSIONS (mm are the original dimensions).

UNIT	A max.	A₁	A₂	A₃	bₚ	c	D(1)	E(2)	e	HE	L	Lₚ	Q	v	w	y	Z	θ
mm	1.2	0.15 0.05	1.05 0.85	0.25	0.28 0.17	0.2 0.1	14.1 13.9	6.2 6.0	0.5	8.3 7.9	1.0	0.8 0.4	0.50 0.35	0.25	0.08	0.1	0.5 0.1	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT364-1		MO-153				~~95-02-10~~ 99-12-27

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Data sheet status

Data sheet status[1]	Product status[2]	Definitions
Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Changes will be communicated according to the Customer Product/Process Change Notification (CPCN) procedure SNW-SQ-650A.

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[2]   The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

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Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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