Ordering number : ENA1668

SANYO Semiconductors
DATA SHEET

LV25450PNW

Bi-CMOS LSI
For Automotive Applications
DSP Tuner Front End

Overview

The LV25450PNW is a tuner front end IC that supports the Sanyo SDRS500 car radio DSP.
The LV25450PNW supports worldwide radio standards including the FM bands used in US, Europe, East-Europe, and Japan as well as the LW, MW, SW, and FM weather bands. It adopts an image canceling mixer for the FM mixer and incorporates a fast PLL locking function. The LV25450PNW also supports automatic alignment using CCB bus control. It requires external EEPROM.
The LV25450PNW can implement a DSP tuner at low cost with a minimal number of external components.

Functions

- AM,/FM-FE, IF, and PLL circuits

Specifications

Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{CC} 8V	OSC_V_{CC} (3), IFAGC_V_{CC} (27), IFAGCOUT-Drive_V_{CC} (35), FE_V_{CC} (61)	9.0	V
	V_{CC} 5V	XTAL_V_{CC} (16), Digital_V_{CC} (25), Analog_V_{CC} (41)	6.0	V
CCB bus maximum input voltage	V_{IN} max	Pin 21, 22, 23	-0.3 to +5.0	V
CCB bus maximum output voltage	V_O	Pin 24	-0.3 to +6.5	V
Allowable power dissipation	Pd max	Ta ≤ 85°C *	850	mW
Operating temperature	Topr		-40 to +85	°C
Storage temperature	Tstg		-50 to +150	°C

* : Using the circuit board for the SANYO tuner module (specified board : 55mm × 39mm × 1.3mm, glass epoxy)

Recommended Operating Conditions at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Recommended supply voltage	V_{CC} 8V	OSC_V_{CC} (3), IFAGC_V_{CC} (27), IFAGCOUT-Drive_V_{CC} (35), FE_V_{CC} (61)	8.0	V
	V_{CC} 5V	XTAL_V_{CC} (16), Digital_V_{CC} (25), Analog_V_{CC} (41)	5	V
Operating supply voltage range	V_{CC} 8Vop		7.5 to 8.5	V
	V_{CC} 5Vop		4.5 to 5.5	V
CCB bus high-level input voltage	V_{IH}	CE, DI, CL	2.5 to 5.0	V
CCB bus low-level input voltage	V_{IL}	CE, DI, CL	0 to 0.8	V
CCB bus high-level input current	I_{IH}	CE, DI, CL ; VI5.5V	10 or less	μA
CCB bus low-level input current	I_{IL}	CE, DI, CL ; VI0V	10 or less	μA
DO low-level output voltage	V_{OL}		0.38 or less	V
DO high-level output voltage	V_{OH}	Connected to an LC75045.	2.1 or more	V

Reception Frequencies

Parameter	Symbol	Conditions	Frequency ratings	Unit
FM reception frequencies	f_{FM}	JPN, US, EU, E-EU	65 to 108.1	MHz
FM weather band reception frequencies	f_{FM-WB}		162.4 to 162.55	MHz
AM reception frequencies	f_{AMLW}	LW	144 to 288	kHz
	fAMMW	MW	520 to 1710	kHz
	fAMSW	SW	2.94 to 22.0	MHz

Power on/Power off Timing and the Power on Reset

Recommended Operating Ratings at Ta = 25°C, GND = 0V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Operating supply voltage	Vcop H	Pin 3, 27, 35, 54, 55, 61	7.5		8.5	V
	Vcop L	Pin 16, 25, 41	4.5		5.5	V
Internal logic voltage	VREG3	Pin 26	2.7		3.3	V
	VREG4	Pin 15	3.7		4.3	V
Power application time (8.0 V → 5.0 V)	T7		10		100	ms
Internal register retention voltage	Vhmin3	Pin 26 : Design reference value	VREG3		2.2	V
	Vhmin4	Pin 15 : Design reference value	VREG4		2.2	V
Internal register reset voltage	Voff	Pin 16, 25, 41 : Design reference value	0		0.2	V
Internal register reset power supply rise time	tPOR	Pin 16, 25, 41 : Design reference value	0.05		3	ms
Power application time (5.0 V → 8.0 V)	T14		10		100	ms

Power-on Sequence and Power-on Reset

(1) Power on image and power on reset

Recommended Operating Ratings at Ta = 25°C, GND = 0V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Operating supply voltage	Vcop H	Pins 3, 27, 35, and 61	7.5		8.5	V
	Vcop L	Pins16, 25, and 41	4.5		5.5	V
Internal logic voltage	VREG3	Pin 26	2.7		3.3	V
	VREG4	Pin 15	3.7		4.3	V
Internal register retention voltage	Vhmin3	Pin 26 : Design reference value	2.2		VREG3	V
	Vhmin4	Pin 15 : Design reference value	2.2		VREG4	V
Internal register reset voltage	Voff	Pins 16, 25, and 41 : Design reference value	0		0.2	V
Internal register reset power supply rise time	tPOR	Pins 16, 25, and 41 : Design reference value	0.05		3	ms

Note 1 : When reading out data from pin D0 connection (e.g., E2PROM) with the voltage at the pin 23 below 2.2V, be sure to read the data after transmitting the control data and pin D0 being set “open” because the state of internal register cannot be specified.

Note 2 : It is necessary to set data when power is first applied or there is a momentary power interruption.

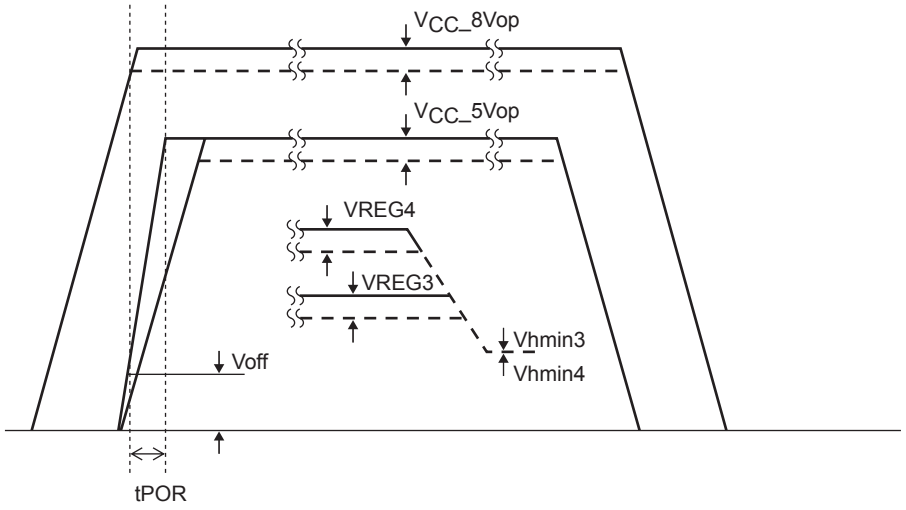
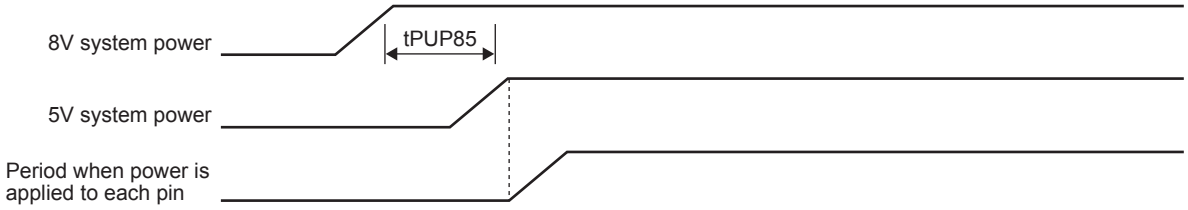


Image of Supply Voltage

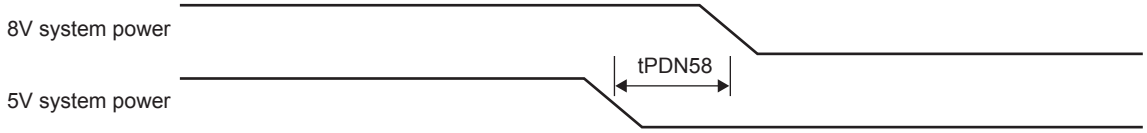
(2) Power on/off sequence

The power on and power off sequences for the IC must follow the order shown below.

- Power on sequence



- Power off sequence



Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Power on period (8V → 5V)	tPUP85		0		100	ms
Power off period (5V → 8V)	tPDN58		0		100	ms

Never apply power to the IC until all the supply voltages reach the predetermined values.

For pin D0, refer to the above section (1), Note 1, and Note 2.

Regarding voltage applied to each power pin, 8V system must always be higher than 5V system (8V system > 5V).

As long as this relationship is maintained and the power supply rise/fall time is within 100ms, there is no problem if the low voltage side power is started up first.

AC Characteristics

Operating Characteristics at Ta = 25°C, V_{CC} = 8.0V, V_{DD} = 5.0V, unless otherwise specified. Ratings for publications

* : These measurements are made using the Yamaichi Electronics IC51-0644-807 IC socket. An IHF bandpass filter is used as the audio filter.

FM Characteristics - FM Front End Mixer Input (No dummy)

Parameter	Symbol	Conditions	Applied voltage				CCB Command				min	typ	max	unit
			Pin 28	Pin 34	Pin 50	Pin 2	IN1	IN2	IN3-1	IN3-2				
DC Characteristics														
Current drain-8V FM	I_{CCO}-8V FM	No input, FM mode I3+I27+I355+I54+I55+I61	3				15	13	25	25	43.2	54	64.8	mA
Current drain-5V FM	I_{CCO}-5V FM	No input, FM mode I16+I25+I41	3				15	13	25	25	20.8	26	31.2	mA
Regulator bias 3V	VREG3V	The pin 26 voltage	3				15	13	25	25	2.7	3	3.3	V
Regulator bias 4V	VREG4V	The pin 15 voltage	3				15	13	25	25	3.6	4	4.4	V
FM antenna dump output current	IANTD-F	The pin 64 output current (Pin 64 load = 100Ω +Pin_Diode × 2 when 6.0V is applied to pin 2	0	0		6	15	13	25	25	4.5	7.5	11	mA
AC Characteristics														
Crystal oscillator frequency	FXTAL	D2-7, 6, 5 = [100]	3				15	13	25	25		4.5		MHz
Crystal oscillator level	VXTAL	D2-7, 6, 5 = [100] (reference value) D32-08 = 0, D2-10, 9, 8 = [100]	3				15	13	25	25	15			mVrms
Crystal oscillator buffer level	VXTAL OSC OUT2	D2-7, 6, 5 = [100] (reference value) D32-08 = 0, D2-10, 9, 8 = [100]	3				15	13	25	25	115	165		mVrms
S-meter DC output * : Adjust the shifter-bits with a 50dBμV input so that Vsm is set to 2.15V.	VSMFM-1	10dBμV, the pin 34 DC output, no modulation	3				15	13	25	25B	0.65	0.95	1.25	V
	VSMFM-2	30dBμV, the pin 34 DC output, no modulation	3				15	13	25	25B	0.95	1.25	1.55	V
	VSMFM-3	50dBμV, the pin 34 DC output, no modulation	3				15	13	25	25B	2.10	2.15	2.20	V
	VSMFM-4	70dBμV, the pin 34 DC output, no modulation	3				15	13	25	25B	3.1	3.4	3.7	V
	VSMFM-5	90dBμV, the pin 34 DC output, no modulation	3				15	13	25	25B	3.7	4	4.3	V
Total gain from mixer to DIV IF amplifier	GMXDIV	FM_MIX_IN, DIV_OUT_IF (pin 32) Ratio of the input to output signal levels 98.1MHz mod = off, 70dBμV-Input	1.5				15	13	25	25	16	19	22	dB
DIV IF amplifier gain	GDIVIF	IF_N_IN1 (pin 46), DIV_OUT_IF (pin 32) Ratio of the input to output signal levels 10.7MHz mod = off, 88dBμV-Input	3				15	13	25	25	4.5	7.5	10.5	dB
1dB compression point driver IF	1DB POINT DIF	IF_N_IN1 (pin 46), DIV_OUT_IF (pin 32) Ratio of the input to output signal levels 10.7MHz mod = off	3				15	13	25	25		111		dB
Narrow IF AGC grain (FM)	GIFAGCNF1	FM_ANALOG_IN (pin 46), 10.7OUTN (pin 30) Ratio of the input to output signal levels 10.7MHz mod = off 100dBμV-Input D32-27 to 25 = 011	0				15	13	25	25	-4.5	-2.5	-0.5	dB
Narrow IF AGC grain (FM)	GIFAGCNF2	FM_ANALOG_IN (pin 46), 10.7OUTN (pin 30) Ratio of the input to output signal levels 10.7MHz mod = off 80dBμV-Input D32-27 to 25 = 011	3				15	13	25	25	23.5	25.5	27.5	dB
1dB complession point FM-Narrow	1DB POINT NF	FM_ANALOG_IN (pin 46), 10.7OUTN (pin 30) 10.7MHz mod = off D32-27 to 2] = 011	0				15	13	25	25	107			dBμV

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Parameter	Symbol	Conditions	Applied voltage				CCB Command				min	typ	max	unit
			Pin 28	Pin 34	Pin 50	Pin 2	IN1	IN2	IN3-1	IN3-2				
Image cancellation ratio (US)	IR US	98.1MHz reference, the amount rejected at +21.4MHz Trm-Bit D2-18=[0]:ON APF-ADJ D32-19 to 16=[1010]:10	1.5				15	21	25	58	30			dB
Image cancellation ratio (JPN)	IR JPN	83MHz reference, the amount rejected at -21.4MHz D1-28 to 26 = [010] Trm-Bit D2-18=[1]:OFF APF-ADJ D32-19 to 16=[1000]:8	1.5				22	13	27	25	25			dB
FM wide AGC on sensitivity F1	WAGC ON-F1	fr = 102.1MHz FM-Wide AGC-Bit D32-3 to 0 = [0000] : minimum	0	3			15	13	25	13	78	85	92	dBμV
FM wide AGC on sensitivity F2	WAGC ON-F2	fr = 102.1MHz FM-Wide AGC-Bit D32-3 to 0 = [1111] : maximum	0	3			15	13	25	15	92	99	106	dBμV
FM narrow AGC on sensitivity F1	NAGC ON-F1	fr = 98.1MHz FM-Narrow AGC-Bit D32-7 to 4 = [0000] : minimum	0	3			15	13	25	16	70	77	84	dBμV
FM narrow AGC on sensitivity F2	NAGC ON-F2	fr = 98.1MHz FM-Narrow AGC-Bit D32-7 to 4 = [1111] : maximum	0	3			15	13	25	18	86	93	100	dBμV
Practical sensitivity	S/N-31	Connected to an LA1787 (MPX, left channel output) *HCC OFF 98.1MHz, 31dBμV, fm = 1kHz, 22.5kHz-mod 62/63pin input	3				15	13	25	25	30			dB
Signal-to-noise ratio	S/N-90	Connected to an LA1787 (MPX, left channel output) 98.1MHz, 90dBμV, fm = 1kHz, 22.5kHz-mod 62/63pin input	0				15	13	25	25	54	57		dB

AM Characteristics : AM, AM-ANT inputs

Parameter	Symbol	Conditions	Applied voltage				CCB Command				min	typ	max	unit
			Pin 28	Pin 34	Pin 50	Pin 2	IN1	IN2	IN3-1	IN3-2				
DC Characteristics														
Current drain-8V AM	I_{CCO}-8V AM	No input, AM mode I3+I27+I35+I54+I55+I61	3				33	15	26	26	36	46	56	mA
Current drain-5V AM	I_{CCO}-5V AM	No input, AM mode I16+I25+I41	3				33	15	26	26	15	19	23	mA
AM antenna dump output current	IANTD-A	When pin 50 is connected to ground The ANT-D (pin 52) output current	3		0		33	15	26	26	3.5	6	9	mA
AC Characteristics														
First AM amplifier gain	GAMP1	FM_N_IN1 (pin 46) IF_OUT (pin 44), after CF matching, 10.7MHz mod = off 74dBμV = Input	0				33	15	26	26	5.2	6.2	7.2	dB
Narrow IF AGC grain (AM)	GIFAGCNA1	AM_ANALOG_IN (pin 39), 10.7OUTN (pin 30) Ratio of the input to output signal levels 10.7MHz mod = off 100dBμV-Input D32-27 to 25 = [011]	0				33	15	26	26	-4.5	-2.5	-0.5	dB
Narrow IF AGC grain (AM)	GIFAGCNA2	AM_ANALOG_IN (pin 39), 10.7OUTN (pin 30) Ratio of the input to output signal levels 10.7MHz mod = off 80dBμV-Input D32-27 to 25 = [011]	3				33	15	26	26	23.5	25.5	27.5	dB
1dB compression point AM - narrow	1DB POINT NA	AM_ANALOG_IN (pin 39), 10.7OUTN (pin 30) 10.7MHz mod = off D32-27 to 25 = [011]	0				33	15	26	26	107			dBμV

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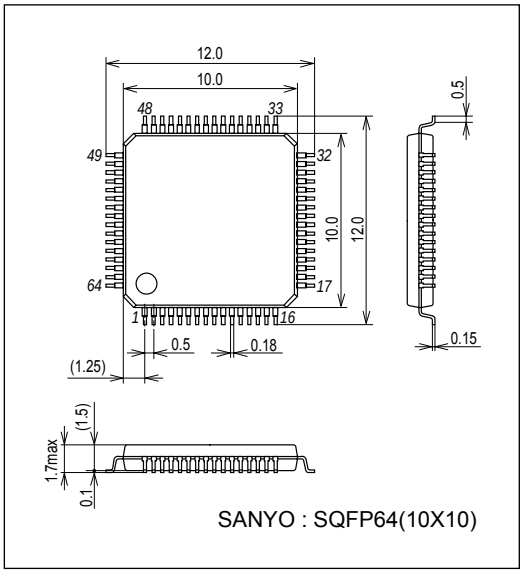
Parameter	Symbol	Conditions	Applied voltage				CCB Command				min	typ	max	unit
			Pin 28	Pin 34	Pin 50	Pin 2	IN1	IN2	IN3-1	IN3-2				
AM wide-AGC on sensitivity A1	WAGC ON-A1	AM-ANT-IN = 1.4MHz, mod = off The input level such that the ANT_D (pin 52) level becomes 0.5V. AM wide AGC-Bit D32-3 to 0 = [0000]	0				33	15	26	27	78.5	83.5	88.5	dBμV
AM wide AGC on sensitivity A2	WAGC ON-A2	AM-ANT-IN = 1.4MHz, mod = off The input level such that the ANT_D (pin 52) level becomes 0.5V. AM wide AGC-Bit D32-3 to 0 = [1101]	0				33	15	26	29	92	97	102	dBμV
AM narrow AGC on sensitivity A1	NAGC ON-A1	AM-ANT-IN = 1MHz, mod = off The input level such that the ANT_D (pin 52) level becomes 0.5V. AM narrow AGC-Bit D32-7 to 4 = [0000]	0				33	15	26	30	60	65	70	dBμV
AM narrow AGC on sensitivity A2	NAGC ON-A2	AM-ANT-IN = 1MHz, mod = off The input level such that the ANT_D (pin 52) level becomes 0.5V. AM narrow AGC-Bit D32-7 to 4 = [1111]	0				33	15	26	32	75	80	85	dBμV
Total AM gain	AMGAIN	1MHz, 60dBμV, mod = off, the ration of the AM_ANT input and the 10.7OUTN (pin 30) output levels	3				33	15	26	26	36	41	46	dB
Practical sensitivity	S/N-33	With an LA1787 connected With a 1MHz, 33dBμV, fm = 1kHz, 30% modulation ANT input and the IF AGC voltage = 3V add.	3				33	15	26	26	20			dB
AM-THD	THD-74	With an LA1787 connected With a 1MHz, 74dBμV, fm = 1kHz, 80% modulation ANT input and the IF AGC voltage adjusted so that the IFAGCOUT level is 100dBμV.	Adjusted				33	15	26	26		0.7	1.0	%
Signal-to-noise ratio	S/N-74	With an LA1787 connected With a 1MHz, 74dBμV, fm = 1kHz, 30% modulation ANT input and the IF AGC voltage adjusted so that the IFAGCOUT level is 100dBμV.	Adjusted				33	15	26	26	52.5	56		dB

Package Dimensions

unit : mm (typ)

3190A



SANYO : SQFP64(10X10)

Test data pattern

PLL IN1 data		CCB address								Control data 1								Control data 2								Control data 3								Control data 4									
IN1	Data contents	A0	A1	A2	A3	A4	A5	A6	A7	P0	P1	P2	P3	P4	P5	P6	P7	P8	P9	P10	P11	P12	P13	P14	P15	OSC_D1	OSC_D2	AM/FM	DVS	R0	R1	R2	R3	OSC_DIV	WB	DELAY_ADJ0	DELAY_ADJ1	DELAY_ADJ2	- - - -	FMFIL	AMFIL	PLL Counter value	Delay-Adj
15	FM_US98.1M fref = 100kHz	0	0	0	1	0	1	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	1	0	2176	0
22	FM_JP83M fref = 100kHz, Delay = 1	0	0	0	1	0	1	0	0	1	0	0	1	1	1	1	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	1	0	1	0	0	0	1	0	2169	1
33	MW1000k fref = 10k (USA)	0	0	0	1	0	1	0	0	0	0	0	1	0	1	1	0	1	1	0	1	1	0	1	0	0	0	1	1	0	0	0	1	0	0	0	0	0	0	0	1	23400	0

PLL IN2 data		CCB address								Control data 1								Control data 2								Control data 3								Control data 4									
IN2	Data contents	A0	A1	A2	A3	A4	A5	A6	A7	- - - -	- - - -	- - - -	- - - -	- - - -	X_SW_0	X_SW_1	X_SW_2	XLVL0	XLVL1	XLVL2	ALC_OFF	- - - -	- - - -	- - - -	- - - -	- - - -	- - - -	OFFSET_SW	- - - -	ULD	UL0	UL1	TWO_DOFF	- - - -	- - - -	DZ0	DZ1	DLC	TEST0	TEST1	TEST2	X'tal-Adj	X'tal-Level
13	FM reception mode settings (Trm=OFF)	1	0	0	1	0	1	0	0	1	0	0	1	0	0	0	1	0	0	1	0	0	0	0	0	0	0	1	0	0	1	1	0	1	0	0	1	0	0	0	0	4	4
15	MW reception mode settings	1	0	0	1	0	1	0	0	1	0	0	1	0	0	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	1	1	0	1	0	0	1	0	0	0	0	4	4
21	FM reception mode settings (Trm=ON)	1	0	0	1	0	1	0	0	1	0	0	1	0	0	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	1	1	0	1	0	0	1	0	0	0	0	4	4

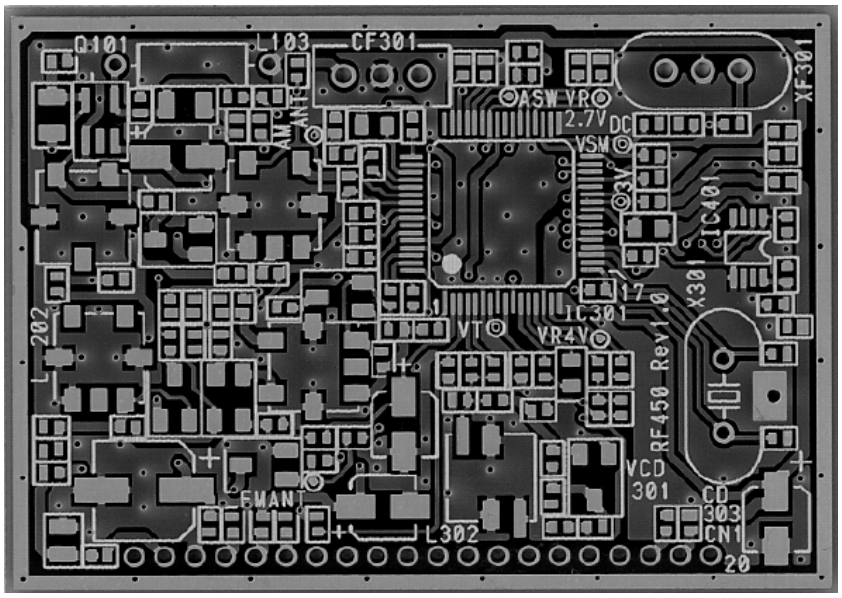
PLL IN3-1 data		CCB address								Control data 1								Control data 2								Control data 3								Control data 4									
IN3-1	Data contents	A0	A1	A2	A3	A4	A5	A6	A7	RFDAC0	RFDAC1	RFDAC2	RFDAC3	RFDAC4	RFDAC5	RFDAC6	RFDAC7	RFDAC8	TUNEROFF	ANTDAC0	ANTDAC1	ANTDAC2	ANTDAC3	ANTDAC4	ANTDAC5	ANTDAC6	ANTDAC7	ANTDAC8	REG_ADJ0	REG_ADJ1	XS0	XS1	DAC9_SW2	DAC9_SW	IQMIX_GAIN	IQ_SW	FMAGC_ON	AMAGC_ON	IFAGC_OFF	DTESTSW	Sub-Address	RF-DAC	ANT-DAC
1	Bit-Check-0	1	0	0	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
2	Bit-Check-1	1	0	0	1	0	1	1	0	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	1	1
3	Bit-Check-2	1	0	0	1	0	1	1	0	0	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	2	2
5	Bit-Check-4	1	0	0	1	0	1	1	0	0	0	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	4	4
6	Bit-Check-7	1	0	0	1	0	1	1	0	1	1	1	0	0	0	0	0	0	0	1	1	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	7	7
7	Bit-Check-8	1	0	0	1	0	1	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	8	8
8	Bit-Check-15	1	0	0	1	0	1	1	0	1	1	1	1	0	0	0	0	0	0	1	1	1	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	15	15
9	Bit-Check-16	1	0	0	1	0	1	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	16	16
10	Bit-Check-31	1	0	0	1	0	1	1	0	1	1	1	1	1	0	0	0	0	0	1	1	1	1	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	31	31
11	Bit-Check-32	1	0	0	1	0	1	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	32	32
12	Bit-Check-63	1	0	0	1	0	1	1	0	1	1	1	1	1	1	0	0	0	0	1	1	1	1	1	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	63	63
13	Bit-Check-64	1	0	0	1	0	1	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	64	64
14	Bit-Check-127	1	0	0	1	0	1	1	0	1	1	1	1	1	1	1	0	0	0	1	1	1	1	1	1	1	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	127	127
15	Bit-Check-128	1	0	0	1	0	1	1	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	128	128
16	Bit-Check-255	1	0	0	1	0	1	1	0	1	1	1	1	1	1	1	1	0	0	1	1	1	1	1	1	1	1	1	0	0	1	0	0	0	0	0	0	0	0	0	0	255	255
17	Bit-Check-256	1	0	0	1	0	1	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0	256	256
18	Bit-Check-511	1	0	0	1	0	1	1	0	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	511	511
25	Standard FM (Upper)	1	0	0	1	0	1	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	1	0	0	0	0	0	256	256
26	Standard FM	1	0	0	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
27	Standard FM (Lower)	1	0	0	1	0	1	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	1	1	0	1	0	0	0	0	0	0	0	0	0	0	256	256
30	Tuner-OFF(FM)	1	0	0	1	0	1	1	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	1	1	0	1	0	0	0	0	0	0	1	0	0	0	256	256

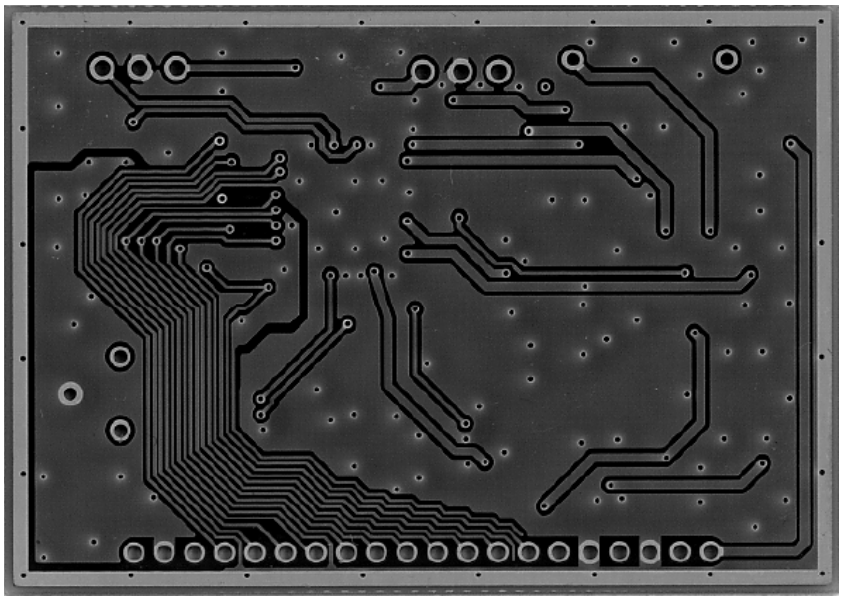
PLL IN3-2 data		CCB address								Control data 1								Control data 2								Control data 3								Control data 4												
IN3-2	Data contents	A0	A1	A2	A3	A4	A5	A6	A7	W_AGC0	W_AGC1	W_AGC2	W_AGC3	N_AGC0	N_AGC1	N_AGC2	N_AGC3	EVA2 (Xtal)	- - - -	- - - -	VREG4V_OFF	KEY_AGC0/RFAGC_H0	KEY_AGC1/RFAGC_H1	KEY_AGC2/RFAGC_H2	KEY_AGC3/RFAGC_H3	APF_ADJ0/RFAGC_S0	APF_ADJ1/RFAGC_S1	APF_ADJ2/RFAGC_S2	APF_ADJ3/RFAGC_S3	S_METER0	S_METER1	S_METER2	S_METER3	S_METER4	ADJ_N0	ADJ_N1	ADJ_N2	- - - -	FMFETOFF	W_KEYED	Sub-Address	Wide-AGC	Narrow-AGC	Keyed-AGC	AM-RFAGC Hard	AM-RFAGC Soft	FM-S-meter Shifter	IFAGC-Amp Gain
13	FM (W-AGC-Bit = 0)	1	0	0	1	0	1	1	0	0	0	0	0	1	1	1	0	0	0	0	0	1	1	1	0	1	1	1	0	1	1	1	1	0	1	1	0	0	0	0	1	0	7	0	7	7	15	3
15	FM (W-AGC-Bit = 15)	1	0	0	1	0	1	1	0	1	1	1	1	1	1	1	0	0	0	0	0	1	1	1	0	1	1	1	0	1	1	1	1	0	1	1	0	0	0	0	1	15	7	0	7	7	15	3
16	FM (N-AGC-Bit = 0)	1	0	0	1	0	1	1	0	1	1	1	0	0	0	0	0	0	0	0	0	1	1	1	0	1	1	1	0	1	1	1	1	0	1	1	0	0	0	0	1	7	0	0	7	7	15	3
18	FM (N-AGC-Bit = 15)	1	0	0	1	0	1	1	0	1	1	1	0	1	1	1	1	0	0	0	0	1	1	1	0	1	1	1	0	1	1	1	1	0	1	1	0	0	0	0	1	7	15	0	7	7	15	3
25	Standard FM-2	1	0	0	1	0	1	1	0	1	1	1	0	1	1	1	0	0	0	0	0	1	1	1	0	1	1	1	0	1	1	1	1	0	1	1	0	0	0	0	1	7	7	0	7	7	15	3
25B	Standard FM-2 Vsm-Shifter After the adjusting	1	0	0	1	0	1	1	0	1	1	1	0	1	1	1	0	0	0	0	0	1	1	1	0	1	1	1	0	*	*	*	*	*	1	1	0	0	0	0	1	7	7	0	7	7	Adjust-ment	3
26	Standard AM-2	1	0	0	1	0	1	1	0	1	1	1	0	1	1	1	0	0	0	0	0	0	1	1	0	0	0	1	1	1	1	1	1	0	1	1	0	0	0	0	1	7	7	0	6	12	15	3
27	AM (W-AGC-Bit = 0)	1	0	0	1	0	1	1	0	0	0	0	0	1	1	1	0	0	0	0	0	1	1	1	0	0	0	1	1	1	1	1	1	0	1	1	0	0	0	0	1	0	7	0	6	12	15	3
29	AM (W-AGC-Bit = 13)	1	0	0	1	0	1	1	0	1	0	1	1	1	1	1	0	0	0	0	0	1	1	1	0	0	0	1	1	1	1	1	1	0	1	1	0	0	0	0	1	13	7	0	6	12	15	3
30	AM (N-AGC-Bit = 0)	1	0	0	1	0	1	1	0	1	1	1	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0	1	1	1	1	1	1	0	1	1	0	0	0	0	1	7	0	0	6	12	15	3
32	AM (A-AGC-Bit = 15)	1	0	0	1	0	1	1	0	1	1	1	0	1	1	1	1	0	0	0	0	1	1	1	0	0	0	1	1	1	1	1	1	0	1	1	0	0	0	0	1	7	15	0	6	12	15	3
58	Standard FM-2 Trm=ON APF-Adj=10	1	0	0	1	0	1	1	0	1	1	1	0	1	1	1	0	1	0	0	0	1	1	1	0	1	0	1	0	1	1	1	1	0	1	1	0	0	0	0	1	7	7	1	7	5	15	3

Items marked with an asterisk are Vsm adjustment items. The bit values after adjustment must be retained.

Power dissipation test board

Material : Glass epoxy resin
Conditions : Double-sided circuit board, without chassis
Board size : 55mm × 39mm × 1.3mm





* Ratings for LV25450PNW power dissipation is measured using the above circuit board.

Pin Functions

Pin No.	Pin Name	Pin No.	Pin Name
1	FE_GND	33	IFAGCOUT-Drive GND
2	FM-RF-AGC	34	VSM_DC
3	Local-OSC-V_{CC} 8V	35	IFAGCOUT-Drive V_{CC}
4	Local-OSC (B)	36	VREG2.7V
5	Local-OSC (C)	37	Analog_GND
6	Local-OSC_GND	38	AM ANALOG IN Bypass
7	VT (LPF)	39	AM ANALOG IN
8	FET_GND	40	(non-connection)
9	PLL-LPF_AM	41	Analog_V_{CC} 5V
10	FM_FET_OUT	42	AM_N-AGC pick-up
11	AM_FET_OUT	43	Address-SW
12	AM_CP OUT	44	AM 1stIF_AMP_OUT
13	FM_CP OUT	45	VREG4.9V
14	Digital_GND	46	IF-IN-N1 (CF = 180k)
15	VREG 4V	47	IF-IN-N_Bypass
16	Xtal-V_{CC} 5V	48	(non-connection)
17	XTAL-IN	49	AM-W-AGC
18	XTAL-OUT	50	AM-RF-AGC
19	Xtal-GND	51	AM RF-AGC (Bypass)
20	XTAL_OSC_OUT2	52	AM-ANT-D
21	CE	53	FM N-AGC-IN
22	DI	54	MIX-OUT
23	CL	55	MIX-OUT
24	DO	56	ANT-DAC
25	Digital_V_{CC} 5V	57	RF-DAC
26	VREG 3V	58	(non-connection)
27	IFAGCAMP_V_{CC} 8V	59	AM-MIX-IN2 (Bypass)
28	AGC_DAC_S (fromDSP)	60	AM-MIX-IN1
29	IFAGCAMP_GND	61	FE V_{CC}_8V
30	IFAGC-OUT (10.7MHz) N	62	FM-MIX-IN1
31	IFAGC-OUT (10.7MHz) P	63	FM-MIX-IN2
32	DIV_IF-OUT	64	FM-ANT-D

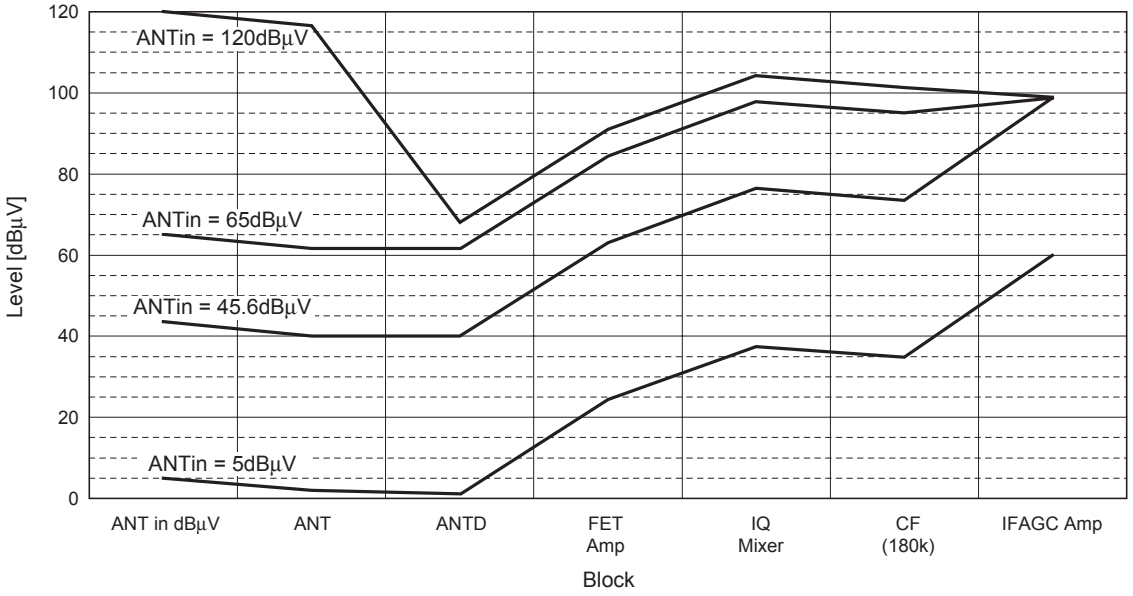
Functions

AM/FM front-end AGC block		
FM Image rejection Mixer (IQ-MIX)	Gain switching : 1 bit	
FM IQ-MIX phase adjust (For the Japanese FM band)		
Injection switching	1 bit	for East Band Receive
AM Double balance Mixer		
Pin diode drive AGC output (AM/FM)		
Wide AGC sensitivity setting (AM/FM)	4 bit DAC	
Narrow AGC sensitivity setting (AM/FM)	4 bit DAC	
Keyed AGC adjust (FM)	4 bit DAC	
AM RF AGC	4 bit DAC	
Local oscillator	133MHz to 262MHz	
Local osc divider (FM/AM)	Division by 1, 2, or 3	
Local osc divider (AM)	Division by 20, 16, 12, or 8	
ANT/RF DAC (FM)	9 bit DAC × 2	
AM 1st IF AMP block		
1st-IF amplifier 10.7M		
IF-Lim-Amp/S-meter block		
S-meter shifter	5 bit DAC	
IF Limiter Amplifier 6 stage		for FM-S-meter
S-meter (DC for keyed AGC) (FM)		
IF-AGC-Amp/IF-Amp for Diversity block		
IF AGC Amplifier (control Voltage from DSP)		
IF output Driver for DSP	10.7MHz IF	
IFAGC-Amp Gain Adjust.		
IF-Amplifier for Diversity (Fixed Gain)	10.7MHz IF	
IF-Output Driver for DIV-IF	10.7MHz IF	
PLL		
Fast lock PLL		
Filter SW		
Charge-Pomp switching		
other		
Tuner off	1 bit SW	
2.7V Regurator adjust	2 bit DAC	

LV25450PNW Level Diagrams

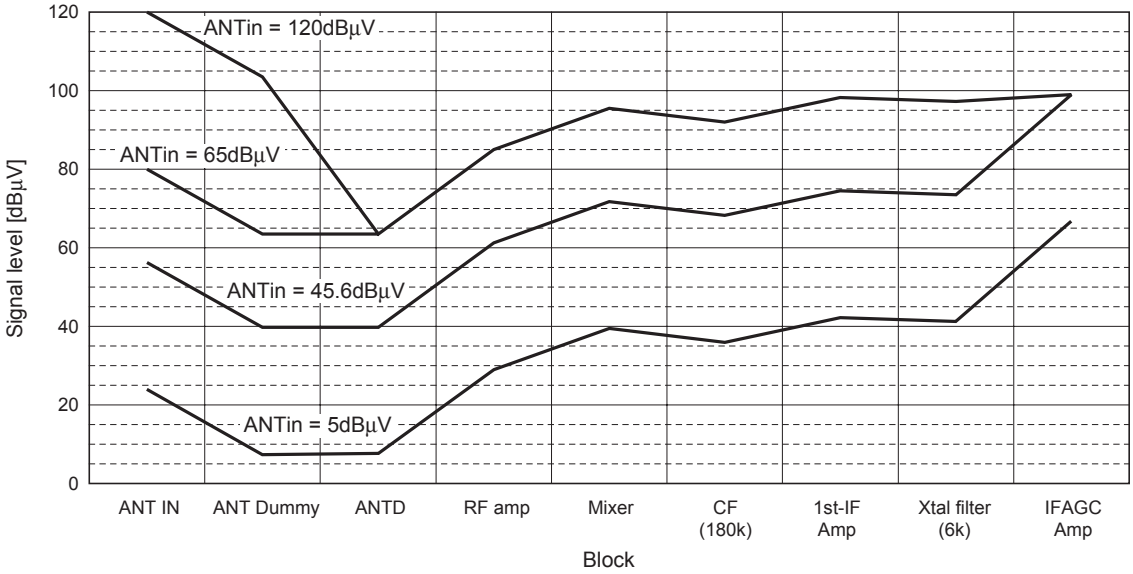
FET : FET Application		-3.5	0	22.9	13.5	-3	25.5	55.4
FM (FET) Gain Down	ANT in dBμV	ANT	ANTD	FET Amp	IQ Mixer	CF (180k)	IFAGC Amp	Total Gain
Near practical sensitivity	5.0	1.5	1.5	24.4	37.9	34.9	60.4	
IFAGC-ON	43.6	40.1	40.1	63.0	76.5	73.5	99.0	
RFAGC-ON	65.0	61.5	61.5	84.4	97.9	94.9	99.0	
Strong input signal	120.0	116.5	68.1	91.0	104.5	101.5	99.0	

FM Level Diagram

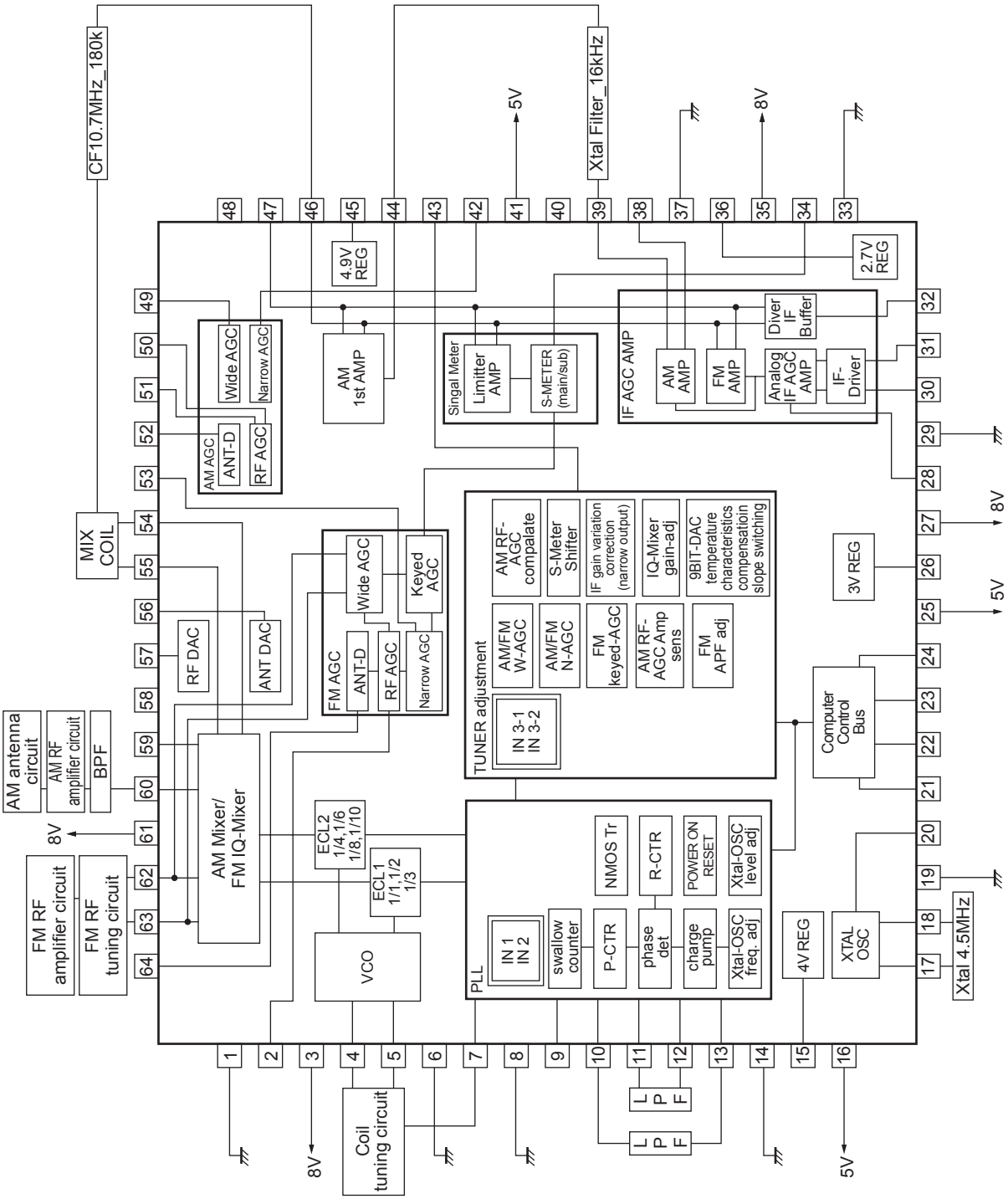


AM	Full Gain	-16.5	0	21.5	10.5	-3.5	6.2	-1	25.5
	ANT IN	ANT Dummy	ANTD	RF amp	Mixer	CF (180k)	1st-IF Amp	Xtal filter (6k)	IFAGC Amp
Near practical sensitivity	24	7.5	7.5	29	39.5	36	42.2	41.2	66.7
IFAGC-ON	56.3	39.8	39.8	61.3	71.8	68.3	74.5	73.5	99
RFAGC-ON	80	63.5	63.5	85	95.5	92	98.2	97.2	99
Strong input signal	120	103.5	63.5	85	95.5	92	98.2	97.2	99

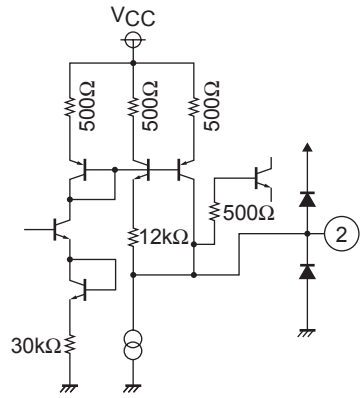
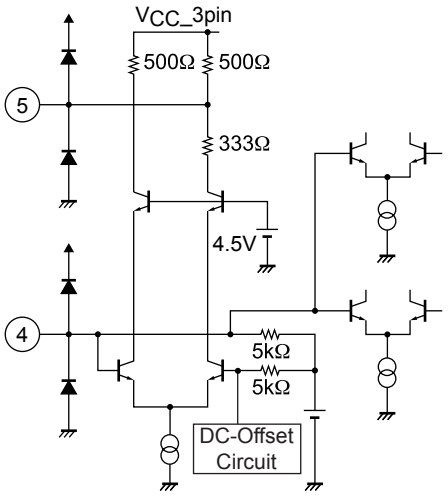
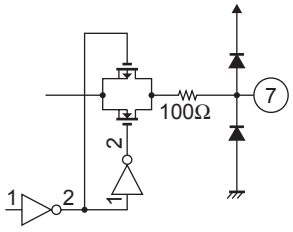
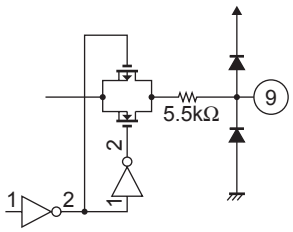
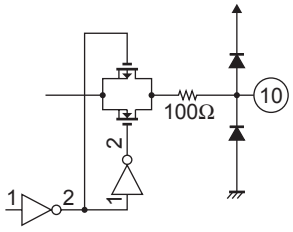
AM Level Diagram



Block Diagram



Pin Description

Pin No.	Pin Function	Description	Equivalent Circuit
1	FE.GND	Front-end block GND	
2	FM-RF-AGC	FM RF AGC voltage output	
3	Local-OSC-V_{CC} 8V	Local oscillator system power supply	
4 5	Local-OSC (B) Local-OSC (C)	Oscillator pins	
6	Local-OSC-GND	Local oscillator system GND	
7	VT (LPF)		
8	FET_GND	Active filter FET GND in the PLL circuit block	
9	PLL-LPF_AM		
10	FM_FET_OUT		

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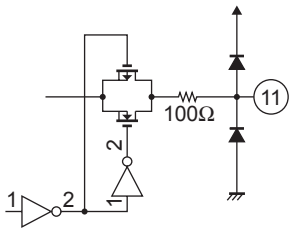
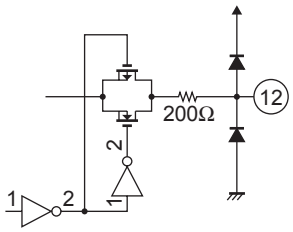
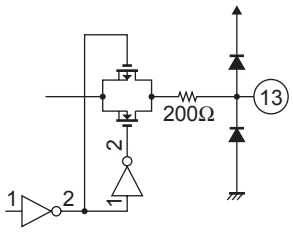
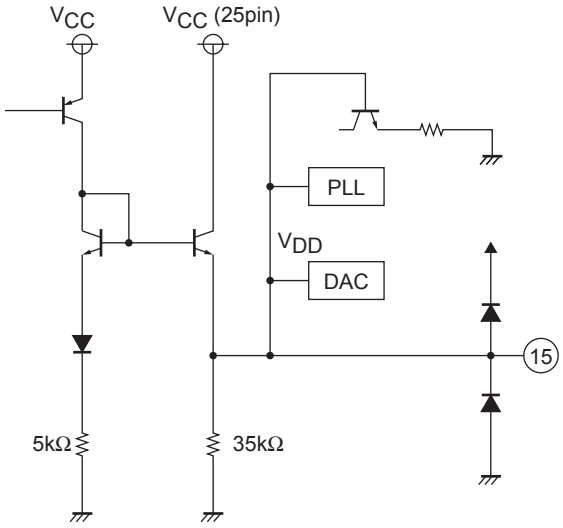
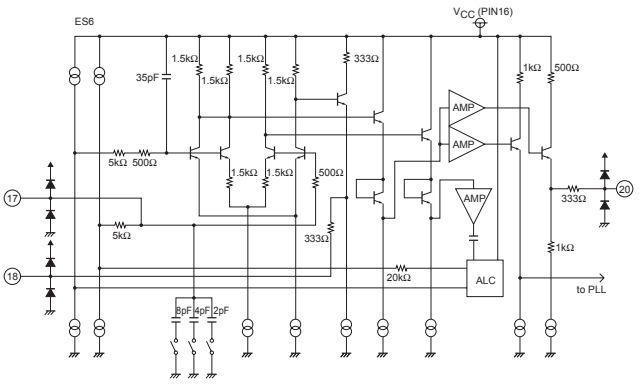
Pin No.	Pin Function	Description	Equivalent Circuit
11	AM_FET_OUT		
12	AM_CP OUT		
13	FM_CP OUT		
14	Digital_GND	Digital system GND	
15	VREG 4V	Dedicated swallow counter 4V regulator voltage smoothing	
16	Xtal-V_{CC} 5V	Dedicated crystal oscillator power supply	
17 18	XTAL-IN XTAL-OUT	Connect a 4.5MHz crystal resonator between pins 17 and 18. Connect a 10pF capacitor between pin 17 and GND, and a 150pF capacitor between pin 18 and GND.	
19	Xtal-GND	Dedicated crystal oscillator GND	

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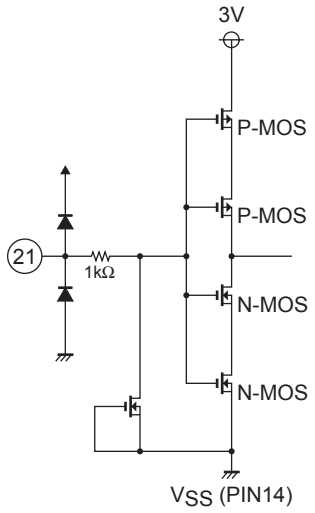
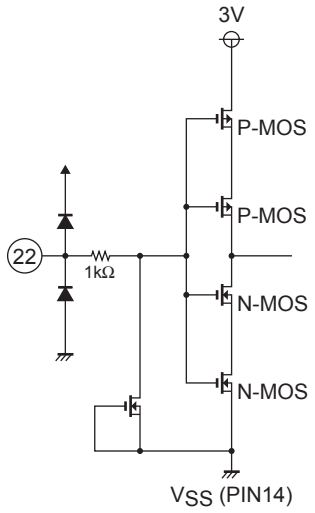
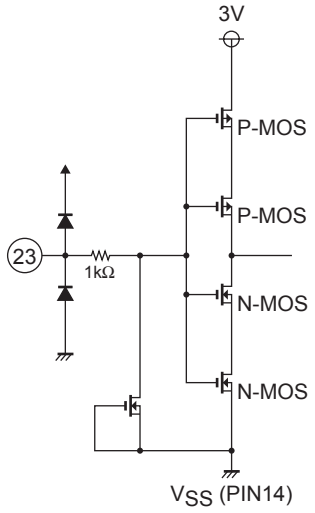
Pin No.	Pin Function	Description	Equivalent Circuit
20	XTAL_OSC_OUT2	Pin 20: clock signal output for 2-tuner	
21	CE	Serial data input (DE) to the LV25450PNW. Force the output to the high level during serial data output (DO).	
22	DI	Input for the serial data transferred to the LV25450PNW from the controller.	
23	CL	Clock used for synchronization when serial data is input to the LV25450PNW (DI) or when serial data is output (DO).	

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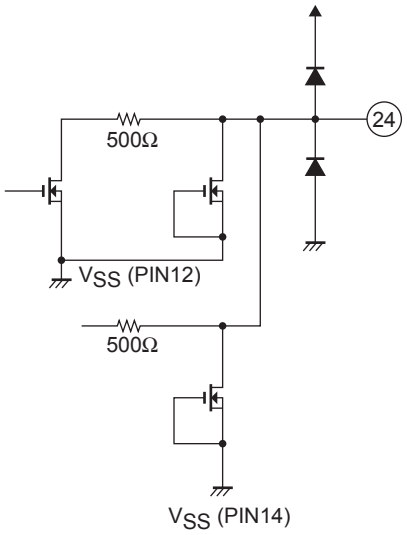
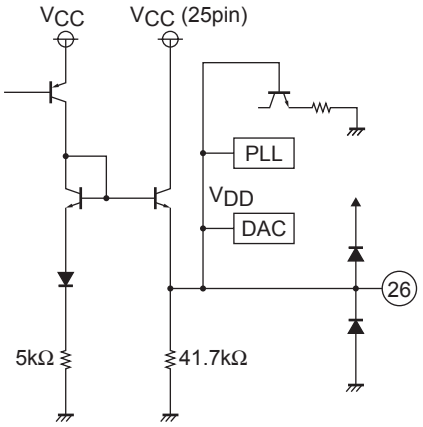
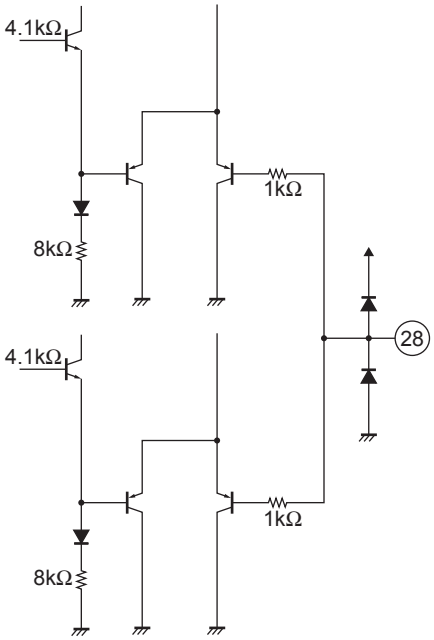
Pin No.	Pin Function	Description	Equivalent Circuit
24	DO	Output for data transferred to the controller by the LV25450PNW	
25	Digital_V_{CC} 5V	Digital system power supply	
26	VREG3V	3V regulator output for PLL power supply	
27	IFAGCAMP_V_{CC} 8V	IF (10.7MHz) signal system power supply	
28	AGC_DAC_S	IF AGC control bias is supplied from the LC7504x (for the analog system).	
29	IFAGCAMP_GND	IF (10.7MHz) signal system GND	

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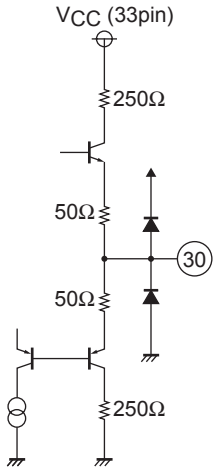
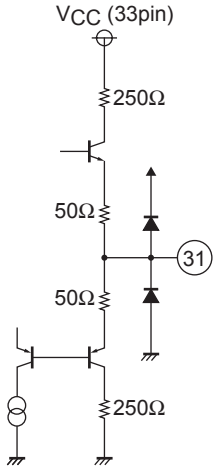
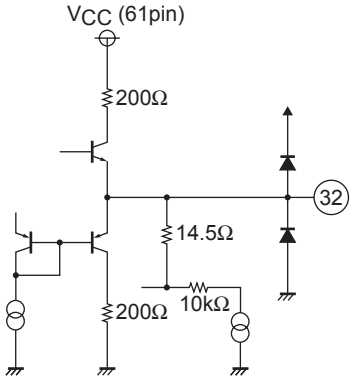
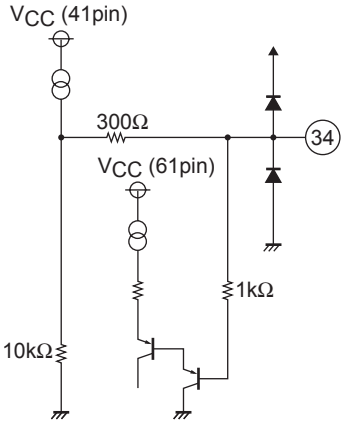
Pin No.	Pin Function	Description	Equivalent Circuit
30	IFAGC-OUT (10.7MHz) N	Narrowband IF (10.7MHz) signal differetial output to the LC7504x for analog use.	
31	IFAGC-OUT (10.7MHz) P	Narrowband IF (10.7MHz) signal differential output to the LC7504x for analog use.	
32	DIV_IF-OUT	Driver 10.7MHz signal buffer output	
33	IFAGCOUT-Drive GND	Dedicated IFAGC output driver GND	
34	VSM_DC	Current driver S-meter output AC components are removed with an external capacitor.	

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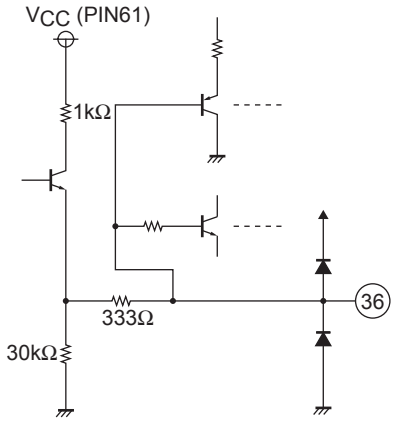
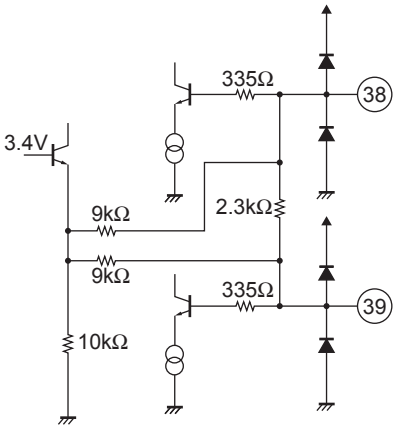
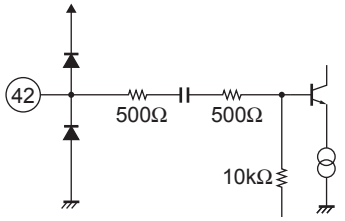
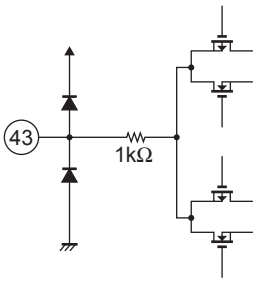
Pin No.	Pin Function	Description	Equivalent Circuit
35	IFAGCOUT-Drive V_{CC}	Dedicated IFAGC output driver V_{CC}	
36	VREG2.7V	2.7V internal regulator output (smoothing)	
37	Analog_GND	Analog system GND	
38 39	AM ANALOG IN Bypass AM ANALOG IN	Pin 39 : AM analog signal input to the AM IFAGC amplifier. (AM 10.7MHz IF signal) Pin 38 : Connected to ground with an external bypass capacitor.	
40	N.C.		
41	Analog_V_{CC} 5V	Analog system power supply	
42	AM Narrow-AGC Pick-Up	AM narrow AGC detection input	
43	Address_SW	When two tuners are used, one (for substitute) of the two ICs'pin 43 is connected to ground, need changes the sddress.	

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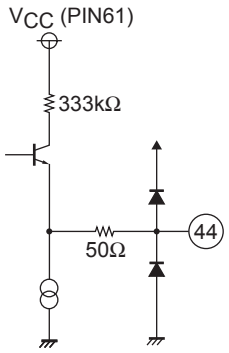
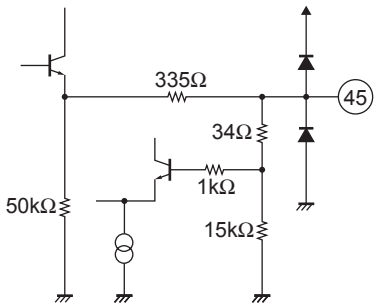
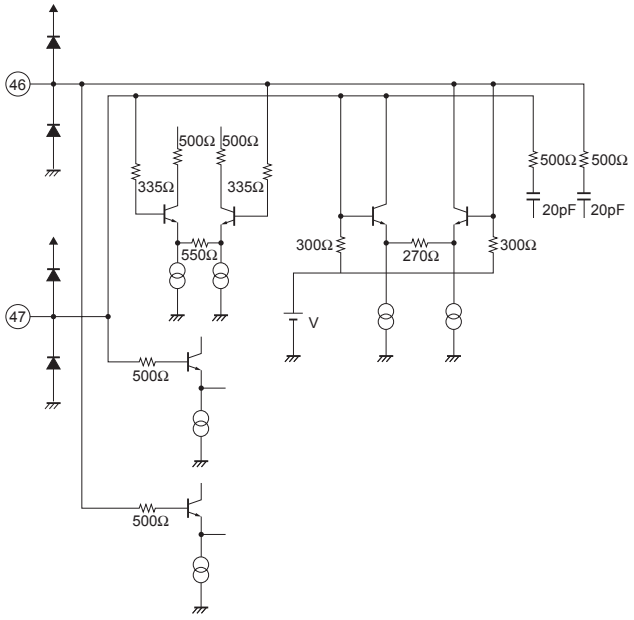
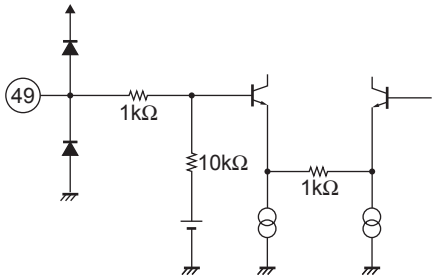
Pin No.	Pin Function	Description	Equivalent Circuit
44	AM 1stIF_AMP_OUT	First AM IF amplifier output	
45	VREG4.9V	4.9V internal regulator output (smoothing)	
46 47	IF-IN-N1 IF-IN-N_Bypass	First AM IF amplifier input Driver 10.7MHz signal buffer input FM limiter amplifier input	
48	N.C.		
49	AM-W-AGC	AM wide AGC pickup	

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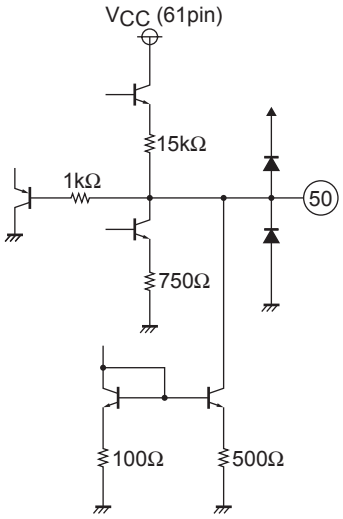
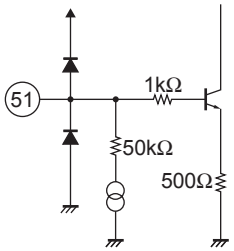
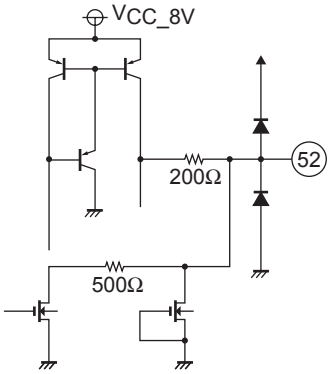
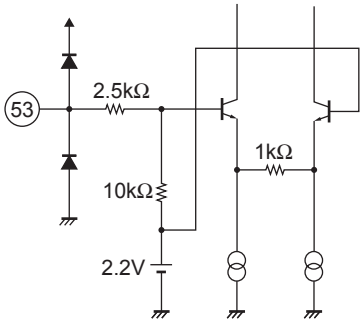
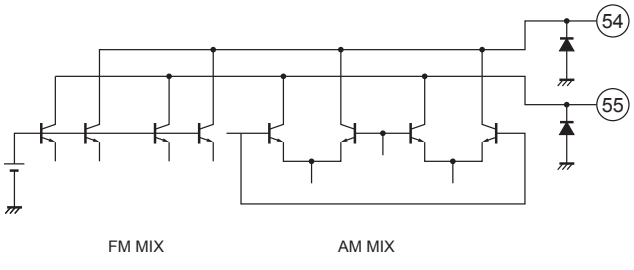
Pin No.	Pin Function	Description	Equivalent Circuit
50	AM-RF-AGC	RF AGC rectifying capacitor Determines the distortion for low-frequency modulation. Increasing the size of C50 : Distortion → Improves Response → Becomes slower Reducing the size of C50 and C 51 : Distortion → Degrades Response → Becomes faster	
51	AM-RF-AGC (Bypass)	Reducing the size of C51 : Distortion → Degrades Response → Becomes faster	
52	AM-ANT-D	Provides the PIN diode drive current. This is the antenna dumping current output.	
53	FM N-AGC-IN	FM narrow AGC input	
54 55	MIX-OUT MIX-OUT	Mixer output (common to FM and AM)	

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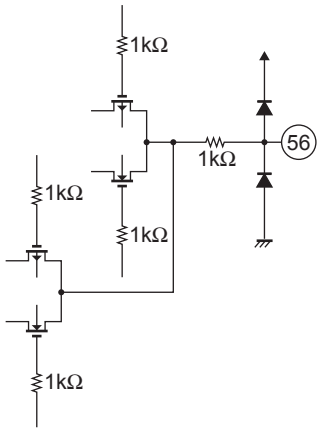
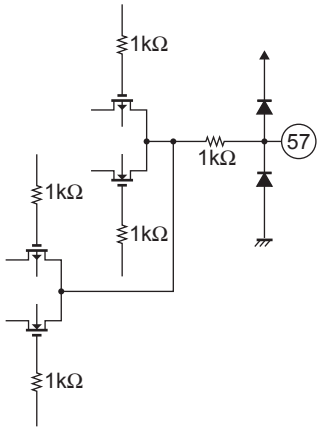
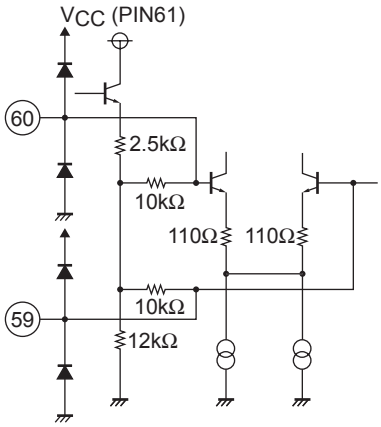
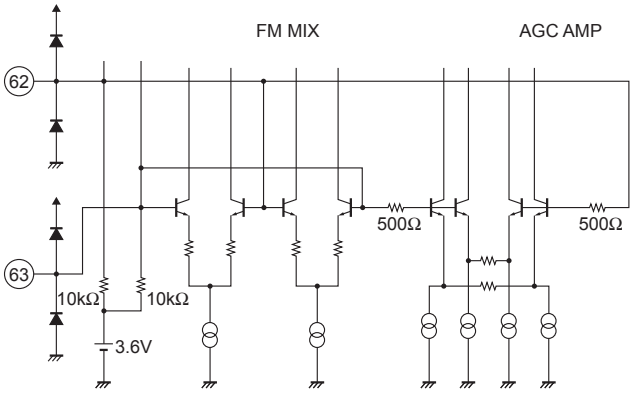
Pin No.	Pin Function	Description	Equivalent Circuit
56	ANT-DAC	Antenna tuning circuit adjustment D/A converter output (9-bit D/A converter)	
57	RF-DAC	RF tuning circuit adjustment D/A converter output (9-bit D/A converter)	
58	N.C.		
59 (Bypass) 60	AM MIX-IN2 AM MIX-IN1	AM mixer input Input impedance : 10kΩ	
61	FE V_{CC} 8V	Front-end block power supply	
62 63	FM MIX-IN1 FM MIX-IN2	FM mixer input FM wide AGC pickup Input impedance : 10kΩ	

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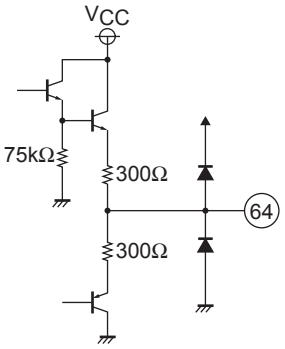
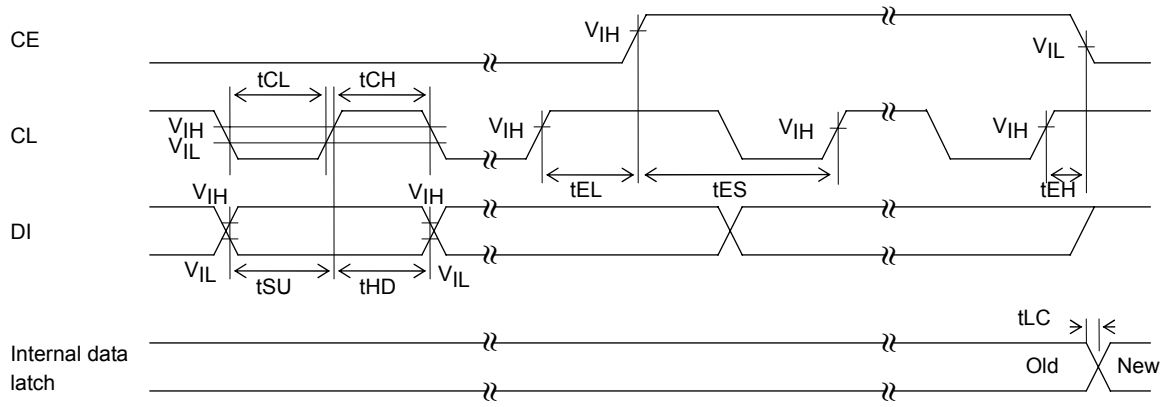
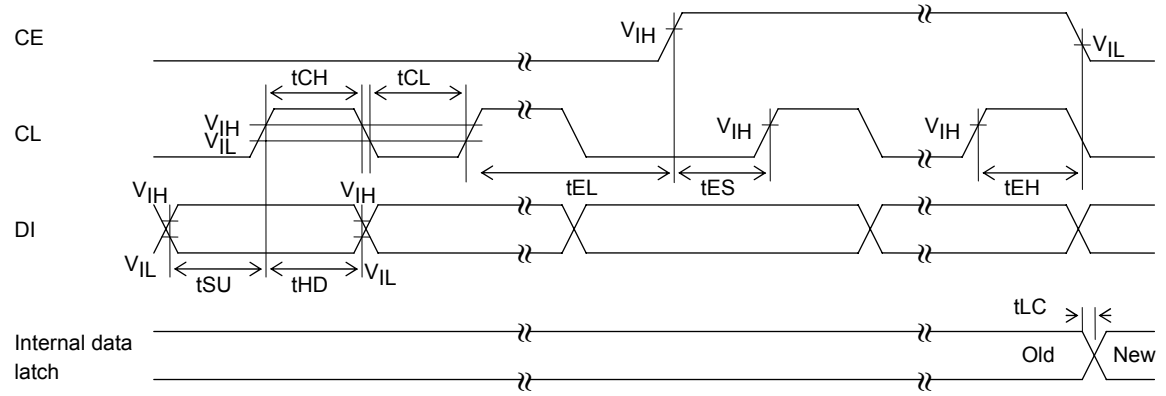
Pin No.	Pin Function	Description	Equivalent Circuit
64	FM ANT D	Pin 64 : The antenna driving current flows when the RF AGC voltage reaches (V_{CC} - Vbe).	

Serial Bus Data Timing

CE : Chip enable
CL : Clock
DI : Data input
DO : Data output (pin information only)



〈〈 When CL is stopped at the L level 〉〉



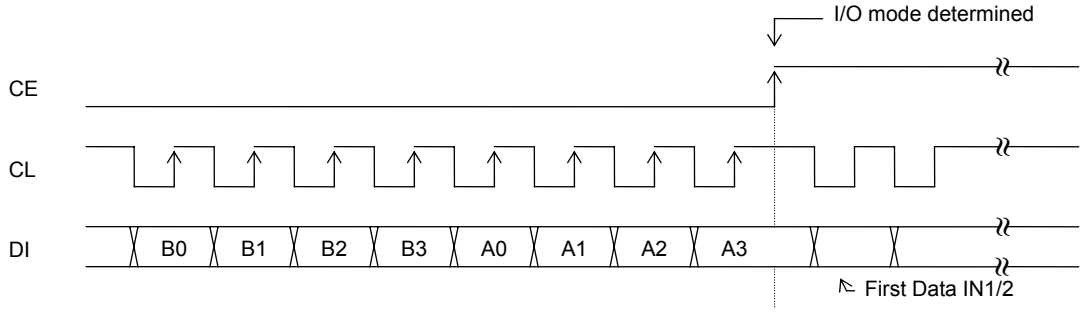
〈〈 When CL is stopped at the H level 〉〉

Parameter	Symbol	Pin	Conditions	min	typ	max	unit
Data setup time	tSU	DI, CL		0.45			μs
Data hold time	tHD	DI, CL		0.45			μs
Clock L-level time	tCL	CL		0.45			μs
Clock H-level time	tCH	CL		0.45			μs
CE wait time	tEL	CE, CL		0.45			μs
CE setup time	tES	CE, CL		0.45			μs
CE hold time	tEH	CE, CL		0.45			μs
Data latch change time	tLC					0.45	μs
Data input high-level voltage	V_{IH}	CL, DI, CE		2.5		5.0	V
Data input low-level voltage	V_{IL}	CL, DI, CE		0		0.8	V

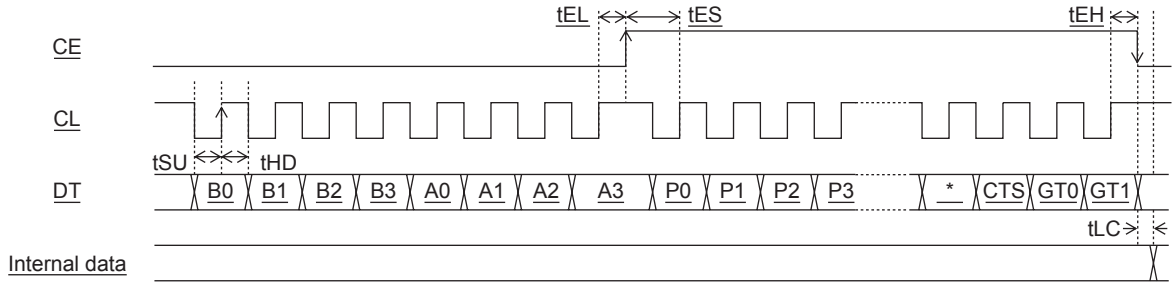
Serial Data I/O Procedures

The LV25450PNW uses the SANYO audio IC serial bus format. Data is input and output using a CCB (Computer Control Bus). The LV25450PNW adopts an 8-bit address version of the CCB format.

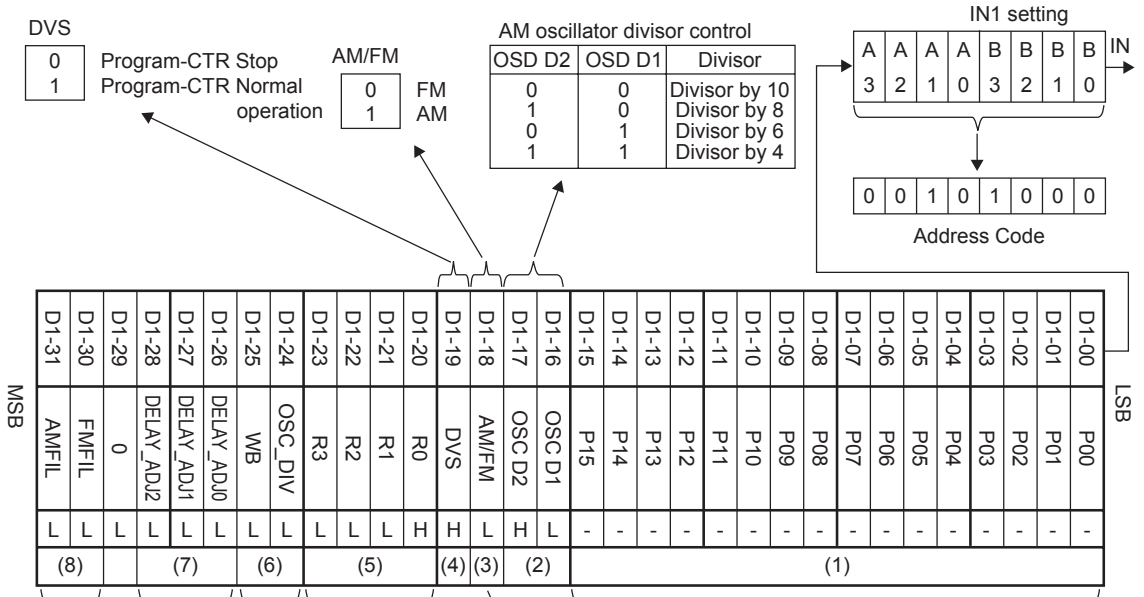
	I/O mode	Address								Contents
		B0	B1	B2	B3	A0	A1	A2	A3	
[1]	IN1	0	0	0	1	0	1	0	0	• Control data input mode. PLL setup • 32 bits of data are input • IN1B is the 2-tuner mode address (when pin 43 is tied to ground)
	IN1B	0	1	0	1	0	1	0	0	
[2]	IN2	1	0	0	1	0	1	0	0	• Control data input mode. PLL setup • 32 bits of data are input • IN2B is the 2-tuner mode address (when pin 43 is tied to ground)
	IN2B	1	1	0	1	0	1	0	0	
[3]	IN3	1	0	0	1	0	1	1	0	• The tuner block is set up in control data input (serial data input) mode. • 32 bits of data are input - There is a sub-address • IN3B is the 2-tuner mode address (when pin 43 is tied to ground)
	IN3B	0	0	0	1	0	1	1	0	

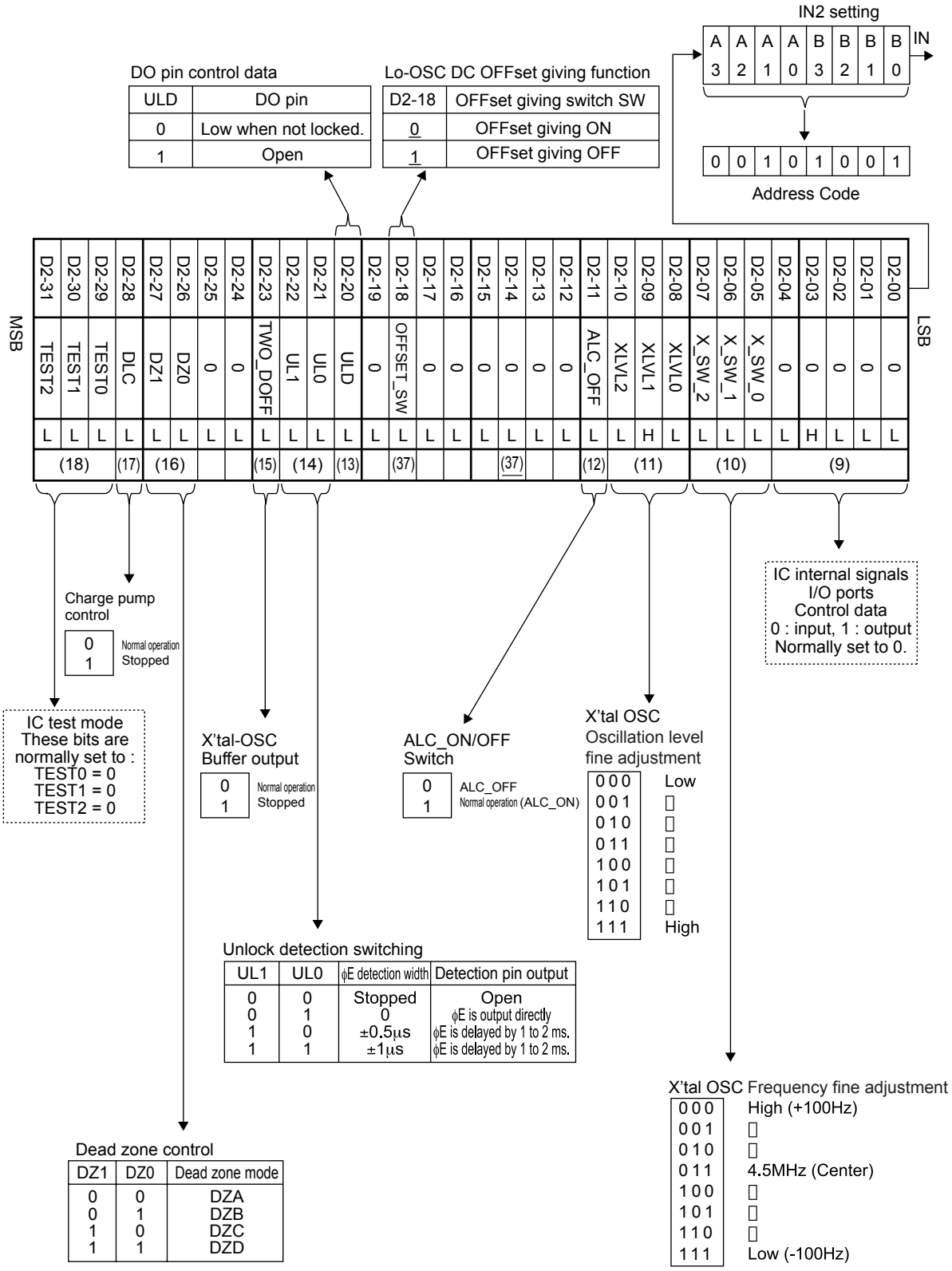


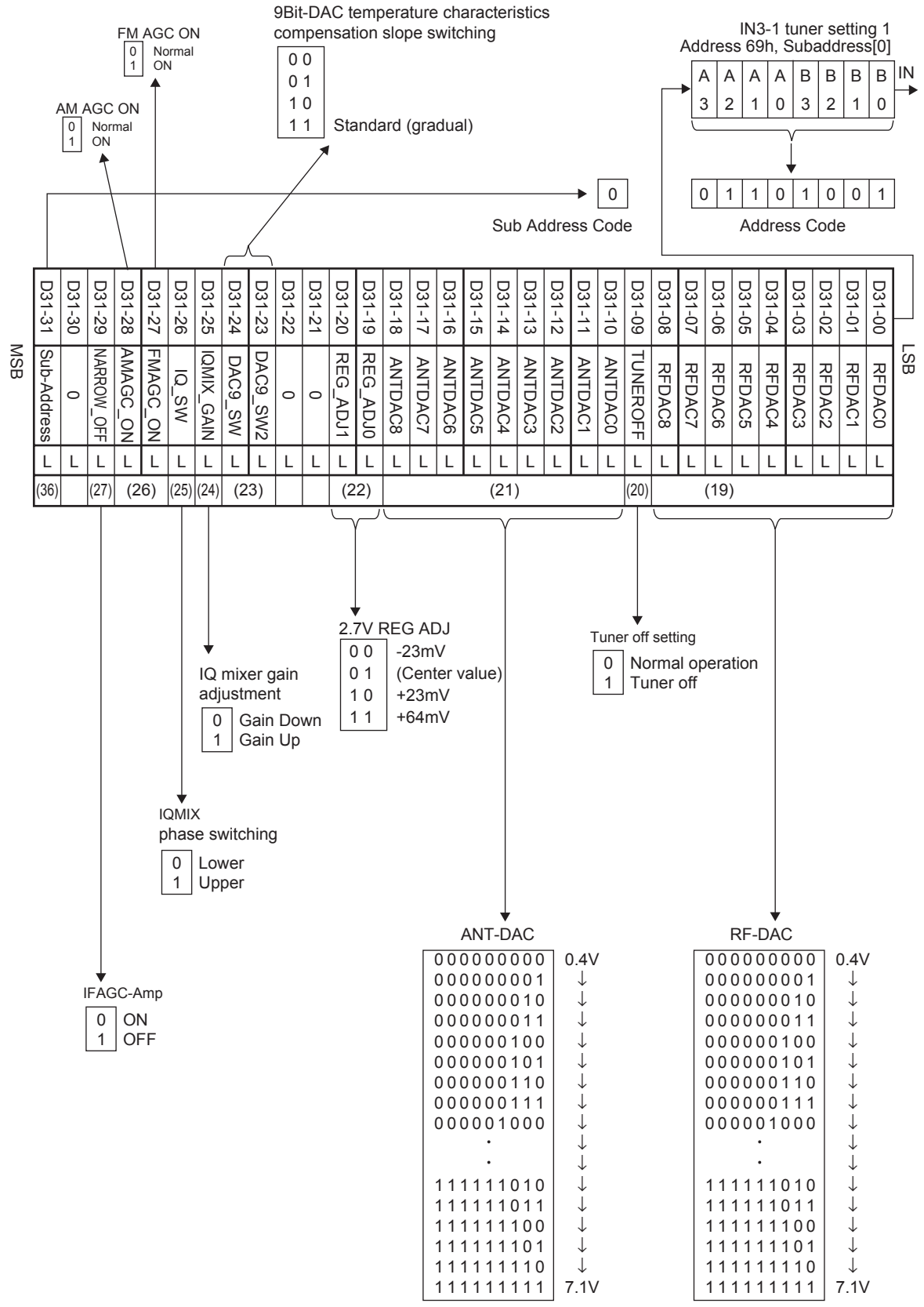
i) Serial data inputs (IN1/IN2/IN3) tSU, tHD, tES, tEL, tEH > 0.45μs tLC < 0.45μs

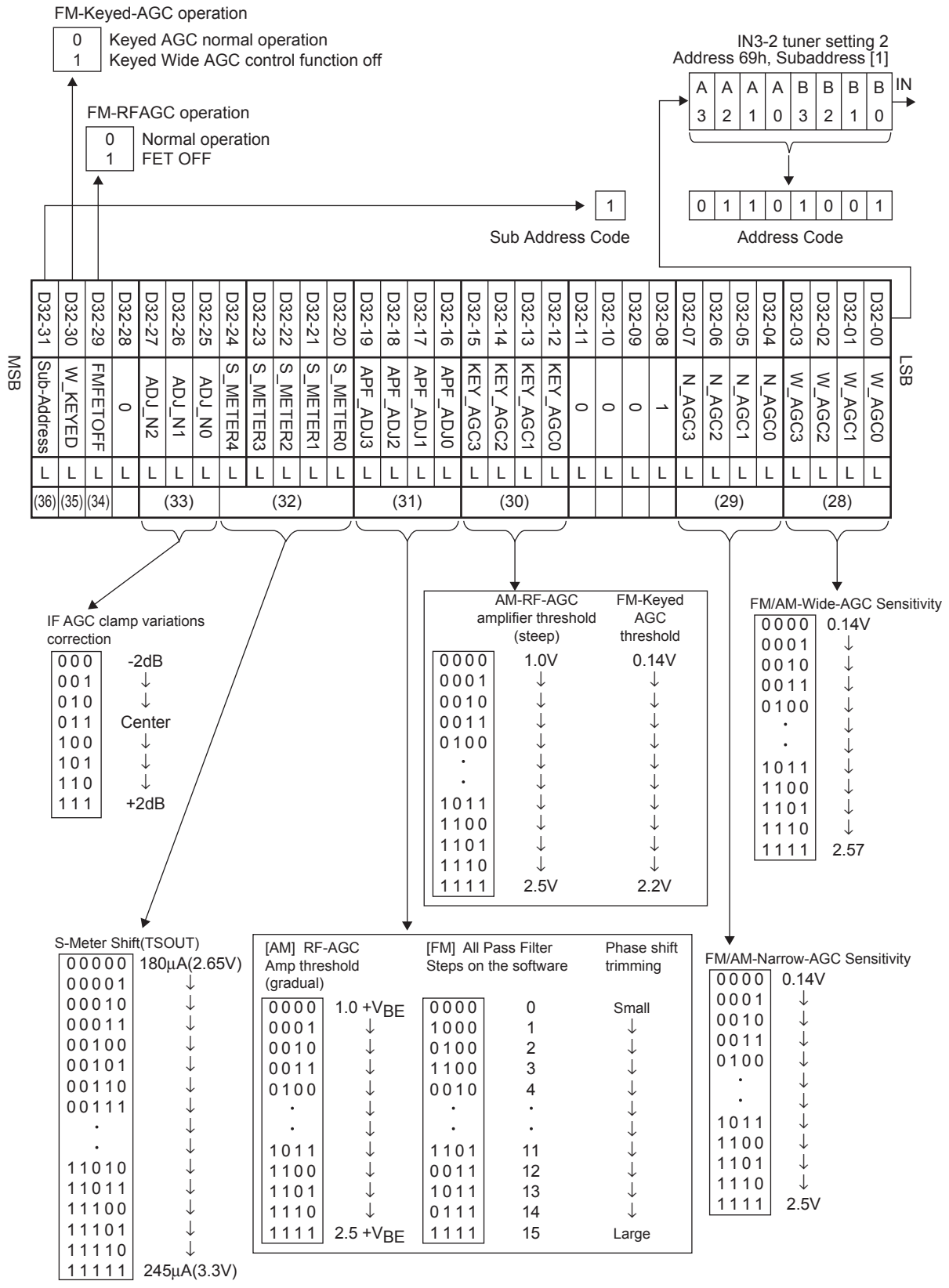


(*1) Since the DO pin is an N-channel open drain circuit, the times for the data to change will differ depending on the value of the pull-up resistor and printed circuit board capacitance.
(*2) The DO pin is normally left open.


DVS
0
1
Program-CTR Stop
Program-CTR Normal operation
AM/FM
0
1
FM
AM
AM oscillator divisor control
OSD D2 | OSD D1 | Divisor
0 | 0 | Divisor by 10
1 | 0 | Divisor by 8
0 | 1 | Divisor by 6
1 | 1 | Divisor by 4
IN1 setting
A3 A2 A1 A0 B3 B2 B1 B0 IN
0 0 1 0 1 0 0 0
Address Code
D1-31 D1-30 D1-29 D1-28 D1-27 D1-26 D1-25 D1-24 D1-23 D1-22 D1-21 D1-20 D1-19 D1-18 D1-17 D1-16 D1-15 D1-14 D1-13 D1-12 D1-11 D1-10 D1-09 D1-08 D1-07 D1-06 D1-05 D1-04 D1-03 D1-02 D1-01 D1-00
MSB
AMFIL FMFIL 0 DELAY_ADJ2 DELAY_ADJ1 DELAY_ADJ0 WB OSC_DIV R3 R2 R1 R0 DVS AM/FM OSC D2 OSC D1 P15 P14 P13 P12 P11 P10 P09 P08 P07 P06 P05 P04 P03 P02 P01 P00
LSB
L L L L L L L L L L L H H L H L - - - - - - - - - - - - - - - -
(8) (7) (6) (5) (4) (3) (2) (1)
AM/FM/WB oscillator divide control
WB | OSD DIV | Divisor
0 | 0 | Divide by 2
0 | 1 | Divide by 3
1 | 0 | Divide by 1
1 | 1 | Divide by 1
*WB : Select 1 for weather band reception
Reference frequency setting
0 0 0 0 100kHz
0 0 0 1 50kHz
0 0 1 0 25kHz
0 0 1 1 25kHz
0 1 0 0 12.5kHz
0 1 0 1 6.25kHz
0 1 1 0 3.125kHz
0 1 1 1 3.125kHz
1 0 0 0 10kHz
1 0 0 1 9kHz
1 0 1 0 5kHz
1 0 1 1 1kHz
1 1 0 0 3kHz
1 1 0 1 30kHz
1 1 1 0 Illegal value
1 1 1 1 Illegal value
PLL filter switching
Filter state | AM/FM | AMFIL | FMFIL
Normal | 0 | OFF | ON
Normal | 1 | ON | OFF
Programmable counter divisor setting (from 272 to 65535)
0 0 0 0 0 0 0 1 0 0 0 1 0 0 0 Divide by 272
0 0 0 0 0 0 0 1 1 1 1 1 0 1 0 Divide by 500
0 0 0 0 0 0 1 1 1 1 1 0 1 0 0 Divide by 1000
0 0 0 0 0 1 1 1 1 1 0 1 0 0 0 Divide by 2000
0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 Divide by 21845
1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 Divide by 43690
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 Divide by 65535
FM-IQMIX phase_Adjust
DELAY_ADJ2 | DELAY_ADJ1 | DELAY_ADJ0 | Adjustment amount
0 | 0 | 0 | Small
0 | 0 | 1 |
0 | 1 | 0 |
0 | 1 | 1 |
1 | 0 | 0 |
1 | 0 | 1 |
1 | 1 | 0 |
1 | 1 | 1 | Large


IN2 setting
A3 A2 A1 A0 B3 B2 B1 B0 IN
0 0 1 0 1 0 0 1
Address Code
DO pin control data
ULD: 0 = Low when not locked., 1 = Open
Lo-OSC DC OFFset giving function
D2-18: 0 = OFFset giving ON, 1 = OFFset giving OFF
MSB
LSB
D2-31 TEST2
D2-30 TEST1
D2-29 TEST0
D2-28 DLC
D2-27 DZ1
D2-26 DZ0
D2-25 0
D2-24 0
D2-23 TWO_DOFF
D2-22 UL1
D2-21 UL0
D2-20 ULD
D2-19 0
D2-18 OFFSET_SW
D2-17 0
D2-16 0
D2-15 0
D2-14 0
D2-13 0
D2-12 0
D2-11 ALC_OFF
D2-10 XLVL2
D2-09 XLVL1
D2-08 XLVL0
D2-07 X_SW_2
D2-06 X_SW_1
D2-05 X_SW_0
D2-04 0
D2-03 0
D2-02 0
D2-01 0
D2-00 0
(18) (17) (16) (15) (14) (13) (37) (37) (12) (11) (10) (9)
Charge pump control
0 Normal operation
1 Stopped
IC test mode
These bits are normally set to :
TEST0 = 0
TEST1 = 0
TEST2 = 0
X'tal-OSC Buffer output
0 Normal operation
1 Stopped
ALC_ON/OFF Switch
0 ALC_OFF
1 Normal operation (ALC_ON)
X'tal OSC Oscillation level fine adjustment
000 Low
001
010
011
100
101
110
111 High
IC internal signals
I/O ports
Control data
0 : input, 1 : output
Normally set to 0.
Unlock detection switching
UL1 UL0 φE detection width Detection pin output
0 0 Stopped Open
0 1 0 φE is output directly
1 0 ±0.5μs φE is delayed by 1 to 2 ms.
1 1 ±1μs φE is delayed by 1 to 2 ms.
Dead zone control
DZ1 DZ0 Dead zone mode
0 0 DZA
0 1 DZB
1 0 DZC
1 1 DZD
X'tal OSC Frequency fine adjustment
000 High (+100Hz)
001
010
011 4.5MHz (Center)
100
101
110
111 Low (-100Hz)


FM AGC ON
0 Normal
1 ON
AM AGC ON
0 Normal
1 ON
9Bit-DAC temperature characteristics
compensation slope switching
0 0
0 1
1 0
1 1
Standard (gradual)
IN3-1 tuner setting 1
Address 69h, Subaddress[0]
A A A A B B B B IN
3 2 1 0 3 2 1 0
0 1 1 0 1 0 0 1
Address Code
0
Sub Address Code
MSB
LSB
D31-31 D31-30 D31-29 D31-28 D31-27 D31-26 D31-25 D31-24 D31-23 D31-22 D31-21 D31-20 D31-19 D31-18 D31-17 D31-16 D31-15 D31-14 D31-13 D31-12 D31-11 D31-10 D31-09 D31-08 D31-07 D31-06 D31-05 D31-04 D31-03 D31-02 D31-01 D31-00
Sub-Address 0 NARROW_OFF AMAGC_ON FMAGC_ON IQ_SW IQMIX_GAIN DAC9_SW DAC9_SW2 0 0 REG_ADJ1 REG_ADJ0 ANTDAC8 ANTDAC7 ANTDAC6 ANTDAC5 ANTDAC4 ANTDAC3 ANTDAC2 ANTDAC1 ANTDAC0 TUNEROFF RFDAC8 RFDAC7 RFDAC6 RFDAC5 RFDAC4 RFDAC3 RFDAC2 RFDAC1 RFDAC0
L L L L L L L L L L L L L L L L L L L L L L L L L L L L L L L L
(36) (27) (26) (25) (24) (23) (22) (21) (20) (19)
2.7V REG ADJ
0 0 -23mV
0 1 (Center value)
1 0 +23mV
1 1 +64mV
Tuner off setting
0 Normal operation
1 Tuner off
IQ mixer gain
adjustment
0 Gain Down
1 Gain Up
IQMIX
phase switching
0 Lower
1 Upper
IFAGC-Amp
0 ON
1 OFF
ANT-DAC
000000000 0.4V
000000001 ↓
000000010 ↓
000000011 ↓
000000100 ↓
000000101 ↓
000000110 ↓
000000111 ↓
000001000 ↓
· ↓
· ↓
111111010 ↓
111111011 ↓
111111100 ↓
111111101 ↓
111111110 ↓
111111111 7.1V
RF-DAC
000000000 0.4V
000000001 ↓
000000010 ↓
000000011 ↓
000000100 ↓
000000101 ↓
000000110 ↓
000000111 ↓
000001000 ↓
· ↓
· ↓
111111010 ↓
111111011 ↓
111111100 ↓
111111101 ↓
111111110 ↓
111111111 7.1V


FM-Keyed-AGC operation
0 Keyed AGC normal operation
1 Keyed Wide AGC control function off
FM-RFAGC operation
0 Normal operation
1 FET OFF
IN3-2 tuner setting 2
Address 69h, Subaddress [1]
A3 A2 A1 A0 B3 B2 B1 B0 IN
0 1 1 0 1 0 0 1
Address Code
1
Sub Address Code
MSB
LSB
D32-31 D32-30 D32-29 D32-28 D32-27 D32-26 D32-25 D32-24 D32-23 D32-22 D32-21 D32-20 D32-19 D32-18 D32-17 D32-16 D32-15 D32-14 D32-13 D32-12 D32-11 D32-10 D32-09 D32-08 D32-07 D32-06 D32-05 D32-04 D32-03 D32-02 D32-01 D32-00
Sub-Address W_KEYED FMFETOFF 0 ADJ_N2 ADJ_N1 ADJ_N0 S_METER4 S_METER3 S_METER2 S_METER1 S_METER0 APF_ADJ3 APF_ADJ2 APF_ADJ1 APF_ADJ0 KEY_AGC3 KEY_AGC2 KEY_AGC1 KEY_AGC0 0 0 0 1 N_AGC3 N_AGC2 N_AGC1 N_AGC0 W_AGC3 W_AGC2 W_AGC1 W_AGC0
(36) (35) (34) (33) (32) (31) (30) (29) (28)
IF AGC clamp variations correction
000 -2dB
001 ↓
010 ↓
011 Center
100 ↓
101 ↓
110 ↓
111 +2dB
AM-RF-AGC amplifier threshold (steep)
FM-Keyed AGC threshold
0000 1.0V 0.14V
0001 ↓ ↓
0010 ↓ ↓
0011 ↓ ↓
0100 ↓ ↓
· ↓ ↓
· ↓ ↓
1011 ↓ ↓
1100 ↓ ↓
1101 ↓ ↓
1110 ↓ ↓
1111 2.5V 2.2V
FM/AM-Wide-AGC Sensitivity
0000 0.14V
0001 ↓
0010 ↓
0011 ↓
0100 ↓
· ↓
· ↓
1011 ↓
1100 ↓
1101 ↓
1110 ↓
1111 2.57
S-Meter Shift(TSOUT)
00000 180μA(2.65V)
00001 ↓
00010 ↓
00011 ↓
00100 ↓
00101 ↓
00110 ↓
00111 ↓
· ↓
· ↓
11010 ↓
11011 ↓
11100 ↓
11101 ↓
11110 ↓
11111 245μA(3.3V)
[AM] RF-AGC Amp threshold (gradual)
[FM] All Pass Filter Steps on the software
Phase shift trimming
0000 1.0 +VBE 0000 0 Small
0001 ↓ 1000 1 ↓
0010 ↓ 0100 2 ↓
0011 ↓ 1100 3 ↓
0100 ↓ 0010 4 ↓
· ↓ · · ↓
· ↓ · · ↓
1011 ↓ 1101 11 ↓
1100 ↓ 0011 12 ↓
1101 ↓ 1011 13 ↓
1110 ↓ 0111 14 ↓
1111 2.5 +VBE 1111 15 Large
FM/AM-Narrow-AGC Sensitivity
0000 0.14V
0001 ↓
0010 ↓
0011 ↓
0100 ↓
· ↓
· ↓
1011 ↓
1100 ↓
1101 ↓
1110 ↓
1111 2.5V

Control Data Documentation

<table>
<tr><th>No.</th><th>Control block/data</th><th>Description</th><th>Related data</th></tr>
<tr><td>(1)</td><td>Programmable divider data
P0 to P15

DVS</td><td>• Sets the programmable divider's divisor.
This is a binary value in which P0 is the LSB, P15 the MSB.
DVS = 0 : The IC internal PLL IN pin is stopped (pulled down)
DVS = 1 : The IC internal PLL IN pin is selected
Set divisor (N) : 272 to 65536
Input frequency range : 120 to 270 MHz
* : See the "Programmable Divider Structure" section for more information.</td><td>AM/FM
OSC D1, D2
WB, OSC DIV</td></tr>
<tr><td>(2)</td><td>AM oscillator divisor control

OSC D1, OSC D2</td><td>• OSC D1, OSC D2–AM oscillator divisor control
<table>
<tr><th>OSC D1</th><th>OSC D2</th><th>Divisor</th></tr>
<tr><td>0</td><td>0</td><td>Divide by 10</td></tr>
<tr><td>0</td><td>1</td><td>Divide by 8</td></tr>
<tr><td>1</td><td>0</td><td>Divide by 6</td></tr>
<tr><td>1</td><td>1</td><td>Divide by 4</td></tr>
</table></td><td>AM/FM
P0 to P15</td></tr>
<tr><td>(3)</td><td>Tuner mode switching

AM/FM</td><td>• Tuner mode switching between AM and FM
1 = AM 0 = FM</td><td>P0 to P15
OSC D1, D2</td></tr>
<tr><td>(4)</td><td>Programmable divider stop

DVS</td><td>• DVS = 0 : The IC internal PLL-IN pin is stopped (pulled down)
DVS = 1 : The IC internal PLL-IN pin is selected
Set divisor (N) : 272 to 65536
Input frequency range : 120 to 270 MHz
* : See the "Programmable Divider Structure" section for more information.</td><td></td></tr>
<tr><td>(5)</td><td>Reference divider data

R0 to R3</td><td>• Selects the reference frequency.
<table>
<tr><th colspan="4"></th><th>Reference frequency setting (kHz)</th></tr>
<tr><th>R3</th><th>R2</th><th>R1</th><th>R0</th><th>Crystal : 4.5MHz</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>100</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>50</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>25</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td><td>25</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>0</td><td>12.5</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>1</td><td>6.25</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>0</td><td>3.125</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>1</td><td>3.125</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td><td>10</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1</td><td>9</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>0</td><td>5</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>0</td><td>3</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>1</td><td>30</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>0</td><td>Illegal value</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>1</td><td>Illegal value</td></tr>
</table></td><td></td></tr>
</table>

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<table>
<tr><th>No.</th><th>Control block/data</th><th>Description</th><th>Related data</th></tr>
<tr><td>(6)</td><td>Tuner mode switching

AM/FM oscillator divisor

OSC_DIV
WB</td><td>(1) AM/FM/WB oscillator divisor control
<table>
<tr><th>WB</th><th>OSC DIV</th><th>Divisor</th></tr>
<tr><td>0</td><td>0</td><td>Divide by 2</td></tr>
<tr><td>0</td><td>1</td><td>Divide by 3</td></tr>
<tr><td>1</td><td>0</td><td>Divide by 1</td></tr>
<tr><td>1</td><td>1</td><td>Divide by 1</td></tr>
</table>
* : WB: Select 1 for weather band reception

(2) AM oscillator divisor control
<table>
<tr><th>OSD D2</th><th>OSC D1</th><th>Divisor</th></tr>
<tr><td>0</td><td>0</td><td>Divide by 10</td></tr>
<tr><td>1</td><td>0</td><td>Divide by 8</td></tr>
<tr><td>0</td><td>1</td><td>Divide by 6</td></tr>
<tr><td>1</td><td>1</td><td>Divide by 4</td></tr>
</table>
In FM mode, only the WB and OSC DIV bits are valid.
In AM mode, this function is set up by combination of the OSC D2, OSC (however, this is fixed at the divide-by-2 setting) D1, WB, and the OSC DIV bits.
FM (Japan) : Fixed at the divide-by-3 setting
FM (other regions) : Fixed at the divide-by-2 setting
WB : Fixed at the divide-by-1 setting (OK if WB = 1)

In AM mode, set WB = 0, OSC DIV = 0 for the divide-by-2 setting.
The OSC D2 and OSC D1 bits can be set according to end product needs.

Example : USA : (1) <divide by 2> × (2) <divide by 10> = divide by 20
SW2 : (1) <divide by 2> × (2) <divide by 4> = divide by 8</td><td>P0 to P15
DVS</td></tr>
<tr><td>(7)</td><td>FM IQ mixer phase adjustment

DELAY_ADJ0 to DELAY_ADJ1</td><td>• FM IQ mixer phase adjustment
FM-IQMIX phase_Adjust
<table>
<tr><th>DELAY_ADJ2</th><th>DELAY_ADJ1</th><th>DELAY_ADJ0</th><th>Adjustment amount</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>Small</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>↓</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>↓</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>↓</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>↓</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>↓</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>↓</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>Large</td></tr>
</table></td><td>OSC_DIV</td></tr>
</table>

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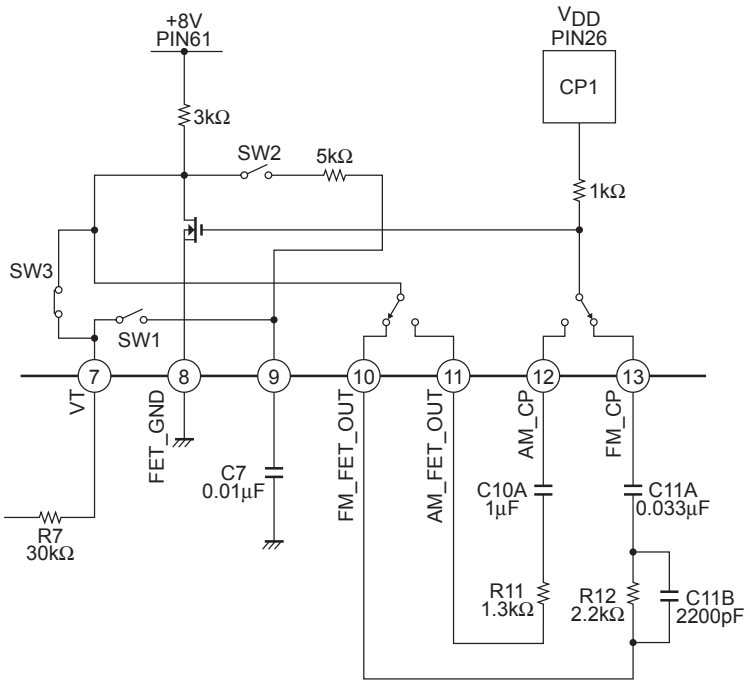
<table>
<tr><th>No.</th><th>Control block/data</th><th>Description</th><th>Related data</th></tr>
<tr><td>(8)</td><td>PLL filter switching mode

FMFIL
AMFIL</td><td>• Switches the PLL filter
PLL filter switching
<table>
<tr><th>Filter state</th><th>AM/FM</th><th>AM filter</th><th>FM filter</th></tr>
<tr><td rowspan="2">Normal</td><td>0</td><td>OFF</td><td>ON</td></tr>
<tr><td>1</td><td>ON</td><td>OFF</td></tr>
</table>
Normal mode (MODE = 0)
The filter state is switched in conjunction with the AM/FM bit.

FM mode (AM/FM = 0)
A filter is formed on pins 8 and 11.
Since this filter can be independent of the filter used in AM mode, PLL locking can be fast.

AM mode (AM/FM = 1)
A filter is formed on pins 9 and 10 and with the two internal switches SW1 and SW2.
An additional filter is added to pin 5 using an internal resistor and an external capacitor.

 
</td><td>AM/FM</td></tr>
<tr><td>(9)</td><td>IC internal signals
I/O ports
Control data</td><td>• Specifies the I/O direction for the I/O ports
Data = 0 : Input port. The value 0 should be specified in normal operation.
= 1 : Output port. A value of 1 is used for IC testing.
* : This data must be set to 0 at all times other than IC evaluation.
Normally set to 0.</td><td></td></tr>
<tr><td>(10)</td><td>Crystal oscillator oscillation frequency fine adjustment data

X_SW_0 to X_SW_2</td><td>• Adjusts the crystal 4.5 MHz reference frequency if beating occurs

X'tal OSC ADJ [When a 4.5MHz oscillator element is used]
<table>
<tr><td>0 0 0</td><td>High (+100Hz)</td></tr>
<tr><td>0 0 1</td><td>↓</td></tr>
<tr><td>0 1 0</td><td>↓</td></tr>
<tr><td>0 1 1</td><td>4.5MHz (Center value)</td></tr>
<tr><td>1 0 0</td><td>↓</td></tr>
<tr><td>1 0 1</td><td>↓</td></tr>
<tr><td>1 1 0</td><td>↓</td></tr>
<tr><td>1 1 1</td><td>Low (-100Hz)</td></tr>
</table></td><td>R0 to R3,
XLVL0 to XLVL2</td></tr>
</table>

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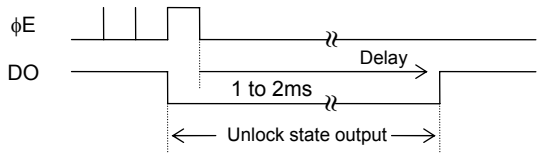
<table>
<tr><th>No.</th><th>Control block/data</th><th>Description</th><th>Related data</th></tr>
<tr><td>(11)</td><td>Crystal oscillator oscillation level
adjustment data

XLVL0 to XLVL2</td><td>• Data used to adjust the crystal 4.5MHz oscillation level when the S/N condition is worsening.

X'tal OSC oscillation level adjustment
0 0 0 Low
0 0 1 ↓
0 1 0 ↓
0 1 1 ↓
1 0 0 ↓
1 0 1 ↓
1 1 0 ↓
1 1 1 High</td><td>R0 to R3,
X_SW_0 to
X_SW_2</td></tr>
<tr><td>(12)</td><td>Crystal oscillator
ACL circuit
ON/OFF switching

ALC_OFF</td><td>• Switches on and off the ALC (Auto level control) in the crystal oscillation circuit. Normally set to high.
ALC_ON/OFF switching
0 ALC_OFF
1 Normal operation (ALC_ON)</td><td></td></tr>
<tr><td>(13)</td><td>DO pin control data

ULD</td><td>• Determines the DO pin output.
DO pin control data
ULD | DO pin
0 | Low when not locked.
1 | Open
* In such a case that the DO pin is multiplexed with EEPROM, transmit a setting data that opens the LV25450PNW DO pin control just before reading out the EEPROM data.
The following item (14) must also be set when monitoring the unlock detection signal.</td><td>UL0, UL1</td></tr>
<tr><td>(14)</td><td>Unlock state detection data

UL0, UL1</td><td>• Selects the phase error (øE) detection width used to judge the PLL locked state.
If a phase error in excess of the øE detection width from the table below occurs, the PLL is seen as being in the unlocked state.
When the PLL is seen as being unlocked, the detection pin (DO) is set low.
UL1 | UL0 | ϕE detection width | Detection pin output
0 | 0 | Stopped | Open
0 | 1 | 0 | ϕE is output directly
1 | 0 | ±0.5μs | ϕE is delayed by 1 to 2 ms.
1 | 1 | ±1μs | ϕE is delayed by 1 to 2 ms.
 
</td><td>ULD</td></tr>
<tr><td>(15)</td><td>Crystal oscillator buffer output stop switching

TWO_DOFF</td><td>• Stops the crystal oscillator buffer output.
1 bit Crystal oscillator buffer switching
0 Normal operation
1 Stopped</td><td></td></tr>
<tr><td>(16)</td><td>Phase comparator control data

DZ0, DZ1</td><td>• Controls the phase comparator's dead zone.
DZ1 | DZ0 | Dead zone mode
0 | 0 | DZA
0 | 1 | DZB
1 | 0 | DZC
1 | 1 | DZD
The DZA setting is selected after the power-on reset.</td><td></td></tr>
</table>

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No.	Control block/data	Description	Related data
(17)	Charge pump control data DLC	• Forcibly sets the charge pump output to the low level (V_{SS} level). DLC = 1 : Low level DLC = 0 : Normal operation * : If the IC deadlocks with VCO oscillator stopped with the VCO control voltage (Vtune) at 0 V, the deadlock can be resolved by setting the charge pump output to the low level and setting Vtune to V_{CC}. This item is set to the normal operation state after the power-on reset.	
(18)	IC internal signal I/O port control data TEST0, TEST1, TEST2	• Specifies the I/O direction for the I/O ports Data = 0 : Input port. The value 0 should be specified in normal operation. = 1 : Output port. A value of 1 is used for IC testing. * : This data must be set to 0 at all times other than IC evaluation.	
(19)	RF tuning D/A converter output RFDAC0 to RFDAC8	• Applies a control voltage to the RF tuning circuit (varactor). 9 bit	DAC9_SW2, DAC9_SW
(20)	Tuner off setting TUNEROFF	• Set the IC to tuner off mode. 1 bit Tuner OFF mord 0 Normal operation 1 Tuner-OFF	
(21)	Antenna tuning D/A converter output ANTDAC0 to ANTDAC8	• Applies a control voltage to the antenna tuning circuit (varactor). 9 bit	DAC9_SW2, DAC9_SW
(22)	2.7V REG ADJ REG_ADJ0 REG_ADJ1	• Adjusts the 2.7 V regulator 2.7V REG ADJ 0 0 -23mV 0 1 (Center value) 1 0 +23mV 1 1 +64mV	
(23)	RF block tuning circuit temperature characteristics compensatioin slope switching data DAC9_SW2 DAC9_SW	• RF block tuning circuit temperature characteristics compensatioin slope switching bits 9bit temperature characteristics compensatioin slope switching 0 0 0 1 1 0 1 1 Standard (Gradual)	RFDAC0 to RFDAC8, ANTDAC0 to ANTDAC8
(24)	IQ mixer gain adjustment data IQMIX_GAIN	• Data used to switch FM IQ mixer gain. 1 bit IQ mixer gain adjustment 0 Gain Down (with RF-Amp) 1 Gain Up (without RF-Amp)	
(25)	IQ mixer phase switching data IQ_SW	• Data used to switch FM IQ mixer phase. 1 bit IQ mixer phase switching 0 Lower 1 Upper	
(26)	Forced AGC (AM/FM) switching data FMAGC_ON AMAGC_ON	• Data used to operate the forced AGC circuit (antenna dumping). FMAGC_ON : FM AGC「0」= NORMAL,「1」= ON AMAGC_ON : AM AGC「0」= NORMAL,「1」= ON Each 1 bit	

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<table>
<tr><th>No.</th><th>Control block/data</th><th>Description</th><th>Related data</th></tr>
<tr><td>(27)</td><td>IF AGC amplifier circuit off switching

NARROW_OFF</td><td>• Switches off the IF AGC amplifier circuit.

1 bit IF AGC amplifier
0 ON (normal operation)
1 OFF</td><td></td></tr>
<tr><td>(28)</td><td>AM/FM wide AGC setting

W_AGC0 to W_AGC3</td><td>• Sets the AM/FM wide AGC sensitivity.

4 bit</td><td>AM/FM</td></tr>
<tr><td>(29)</td><td>AM/FM narrow AGC setting

N_AGC0 to N_AGC3</td><td>• Sets the AM/FM narrow AGC sensitivity.

4 bit</td><td>AM/FM</td></tr>
<tr><td>(30)</td><td>AM RF AGC amplifier threshold (steep) and Keyed AGC setting data

KEY_AGC0 to KEY_AGC3</td><td>• Sets the AM RF AGC amplifier circuit threshold (steep) and the FM Keyed AGC sensitivity.

4 bit | AM-RF-AGC Amp threshold (steep) | FM-Keyed AGC threshold
0 0 0 0 | 1.0V | 0.14V
0 0 0 1 | ↓ | ↓
0 0 1 0 | ↓ | ↓
0 0 1 1 | ↓ | ↓
0 1 0 0 | ↓ | ↓
• | ↓ | ↓
• | ↓ | ↓
1 0 1 1 | ↓ | ↓
1 1 0 0 | ↓ | ↓
1 1 0 1 | ↓ | ↓
1 1 1 0 | ↓ | ↓
1 1 1 1 | 2.5V | 2.2V</td><td>AM/FM</td></tr>
<tr><td>(31)</td><td>AM RF AGC amplifier threshold (gradual) and All Pass Filter setting data

APF_ADJ0 to APF_ADJ3</td><td>• Data used to set the AM RF AGC amplifier threshold (gradual) and the All Pass Filter.

4 bit | AM-RF-AGC Amp threshold (gradual) | FM-Keyed AGC threshold the software | phase shift trimming
0 0 0 0 | 1.0+VBE | 0 0 0 0 | 0 | Small
0 0 0 1 | ↓ | 1 0 0 0 | 1 | ↓
0 0 1 0 | ↓ | 0 1 0 0 | 2 | ↓
0 0 1 1 | ↓ | 1 1 0 0 | 3 | ↓
0 1 0 0 | ↓ | 0 0 1 0 | 4 | ↓
• | ↓ | • | • | ↓
• | ↓ | • | • | ↓
1 0 1 1 | ↓ | 1 1 0 1 | 11 | ↓
1 1 0 0 | ↓ | 0 0 1 1 | 12 | ↓
1 1 0 1 | ↓ | 1 0 1 1 | 13 | ↓
1 1 1 0 | ↓ | 0 1 1 1 | 14 | ↓
1 1 1 1 | 2.5V+VBE | 1 1 1 1 | 15 | Large</td><td>AM/FM</td></tr>
<tr><td>(32)</td><td>S-meter shifter control

S_METER0 to S_METER4</td><td>• Controls the FM S-meter shifter circuit output value.

5 bit</td><td></td></tr>
<tr><td>(33)</td><td>Analog (narrow) IF AGC clamp variations correction

ADJ_N0 to ADJ_N2</td><td>• Corrects the sample-to-sample variations in the IF AGC clamp circuit.

Amount of correction : ±2 dB

3 bit</td><td></td></tr>
<tr><td>(34)</td><td>FM PIN diode forced on state bit

FMFETOFF</td><td>• Forcibly sets the FM PIN diode to the on state.

1 bit</td><td></td></tr>
</table>

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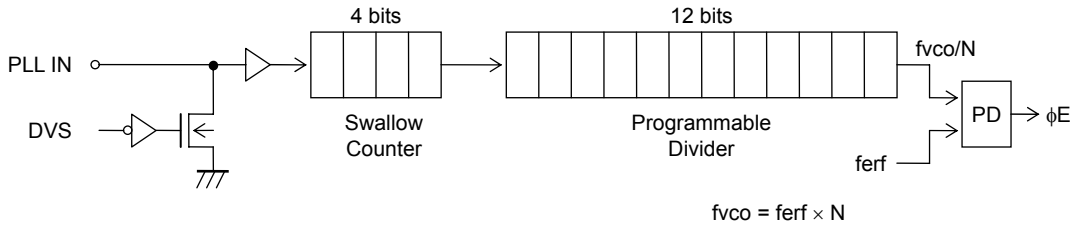
No.	Control block/data	Description	Related data
(35)	LSI test data W_KEYED	• Modifies the keyed AGC connection circuit. 1 bit Keyed AGC switch 0 Wide + narroww 1 Narrow only	
(36)	Sub-Address	• Sub-code address Each 1 bit	
(37)	OFFSET_SW	• The DC offset was given to the differential motion part of LO-OSC for the IRR improvement, and the function to correct Duty was added. It is control Bit to stop this function, and to switch in a state past (The offset giving is not done). 1BITbit	

Programmable Divider Structure



fvco = ferf × N

DVS	Set divisor (N)	Input frequency range (f (MHz))	IC internal PLL IN pin
1	272 to 65535	120 ≤ f ≤ 270	Selected
0	-	-	Stopped

* : Since the IC is closed internally, the input sensitivity is not specified.

Phase Comparator and Charge Pump Circuits

(1) Phase comparator and charge pump operation

In the PLL circuit block shown in figure 1, the phase comparator compares the phases of the reference frequency (fr) and the comparison frequency (fp), and outputs the amount of the phase difference from the charge pump.

Figure 1 PLL Circuit Block

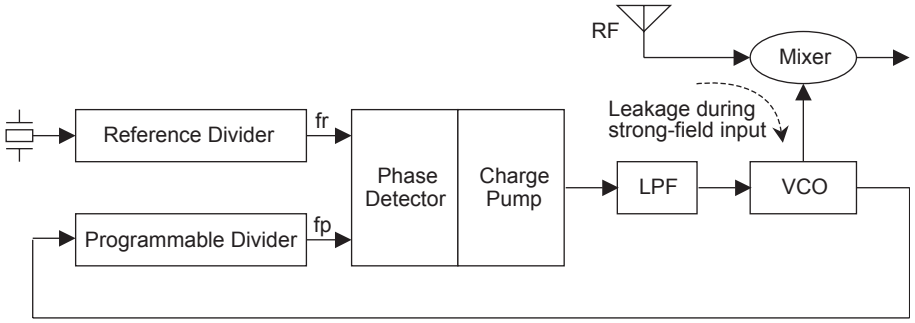
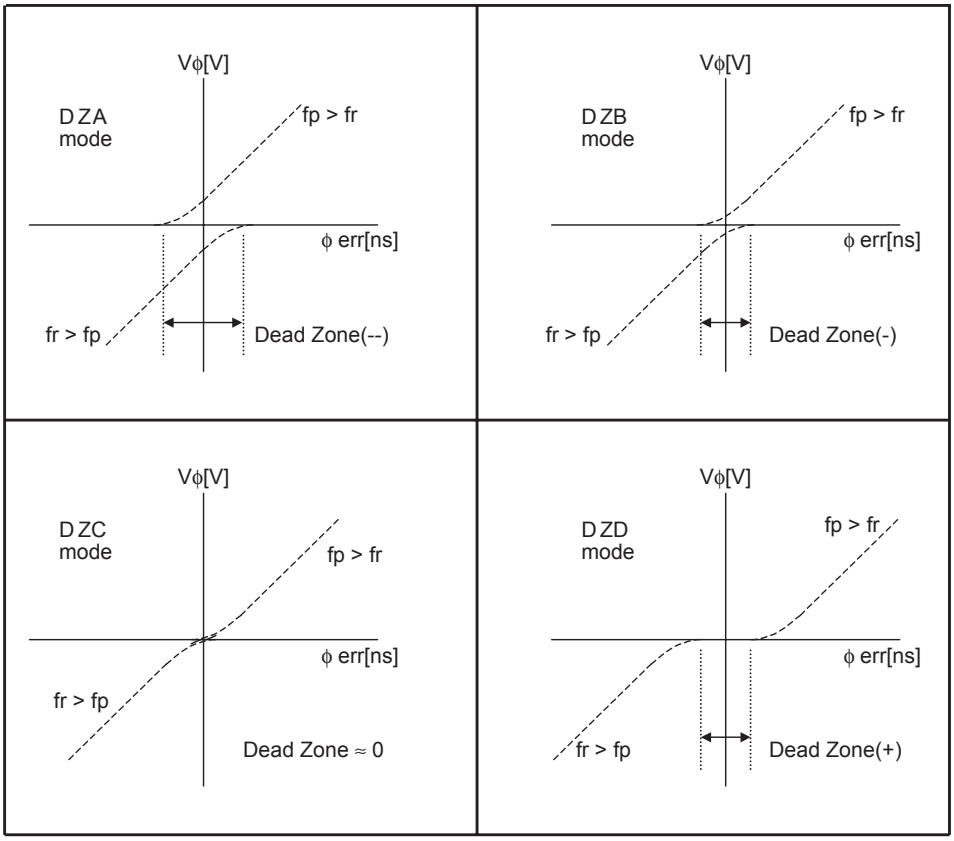


Figure 2 shows the phase comparator/charge pump output characteristics. The phase comparator outputs a voltage Vϕ that is proportional to the phase difference ϕ between fr and fp. The phase comparator's characteristics can be switched by changing the phase comparator dead zone mode setting. The phase comparator can be set to modes (DZA, DZB) in which both the charge pump p-channel and n-channel sides are turned on when the phase difference is small, or can be set to a mode (DZD) that does not output the phase difference when the phase difference is small.

Figure 2 Phase Comparator/Charge Pump Characteristics



(2) Dead zone mode characteristics and selection criteria

This section describes the characteristics of each dead zone mode and the criteria for selecting that mode.

(1) DZA mode

In DZA mode, the correction signal is output from the charge pump even if the reference frequency (fr) and comparison frequency (fp) match. This results in excellent signal-to-noise ratio characteristics. However, due to the generation of reference frequency component sidebands, beating may occur in the presence of a strong input signal. This is because the PLL loop responds sensitively to leakage components from the RF stage through the mixer and this modulates the VCO.

(2) DZB mode

Like DZA mode, in DZB mode the correction signal is output from the charge pump even if the reference frequency (fr) and comparison frequency (fp) match. However, the correction signal voltage is lower in DZB mode than in DZA mode. The feature of this mode is that it provides a better signal-to-noise ratio than DZC or DZD mode yet is less susceptible to beating than DZA mode.

(3) DZC mode

In DZC mode, a correction signal proportional to the phase difference between the reference frequency (fr) and comparison frequency (fp) is output from the charge pump. A small amount of noise may occur when the phase difference is close to 0 ns. Since the signal-to-noise ratio may degrade significantly at low temperatures (under -30°C), this mode should not be used.

(4) DZD mode

In DZD mode, a correction signal proportional to the phase difference between the reference frequency (fr) and comparison frequency (fp) is output from the charge pump. The correction signal is not output when the phase difference is in the vicinity of ± <a few ns>. As a result the signal-to-noise ratio is worse than the other modes, but the occurrence of beating is suppressed.

Power supply turning on/cutting timing and power-on reset

Recommended operating conditions/Ta=25°C, GND=0V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Operation power-supply voltage	Vcop_H	PIN 3,27,35,54,55,61	7.5		8.5	V
	Vcop_L	PIN 16,25,41	4.5		5.5	V
Internal logic voltage	VREG3	PIN 26	2.7		3.3	V
	VREG4	PIN 15	3.7		4.3	V
Power supply turning on time(8.0V → 5.0V)	T7		10		100	ms
Internal register maintenance voltage	Vhmin3	PIN 26 *1	VREG3		2.2	V
	Vhmin4	PIN 15 *1	VREG4		2.2	V
Internal register reset voltage	Voff	PIN 16,25,41 *1	0		0.2	V
Internal register reset power supply start-up time	tPOR	PIN 16,25,41 *1	0.05		3	ms
Power supply turning on time(5.0V → 8.0V)	T14		10		100	ms

*1: Design reference value

Sample Application Circuit