LZ34B1B

1/4-type Color CMOS Image Sensor with 350 k Pixels

DESCRIPTION

The LZ34B1B is a 1/4-type (4.5 mm) solid-state color image sensor that consists of PN photo-diodes and CMOS (Complementary Metal Oxide Semiconductor) devices. The sensor further includes a timing generator (TG), a correlated double sampling (CDS) circuit, an auto gain control (AGC) circuit and an analog-to-digital converter (ADC) circuit. With approximately 350 000 pixels (703 horizontal x 499 vertical), the sensor provides a stable digital color image with extremely low power consumption.

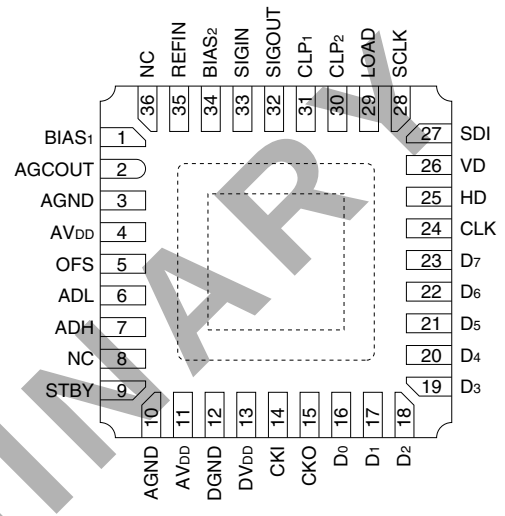
FEATURES

- Progressive scan
- Square pixel
- Compatible with VGA standard
- Number of image pixels : 655 (H) x 493 (V)
- Number of optical black pixels
  - Horizontal : 24 front and 24 rear
  - Vertical : 3 front and 3 rear
- Pixel pitch : 5.6 µm (H) x 5.6 µm (V)
- R, G, and B primary color mosaic filters
- Image inversion function (horizontally and/or vertically)
- Available for two types of power save mode
  - AGC and AD circuits become power-off with serial data
  - All circuits become power-off with STBY pin
- Monitoring mode
- Analog output and 8-bit digital output
- Variable gain control (3 to 30 dB)
- Variable electronic focal plane shutter (1/15 to 1/7 875 s)
- Single +2.8 V power supply
- Package : 36-pin LCC* (N-LCC036-S425B)

* Leadless Chip Carrier

PIN CONNECTIONS

36-PIN LCC TOP VIEW

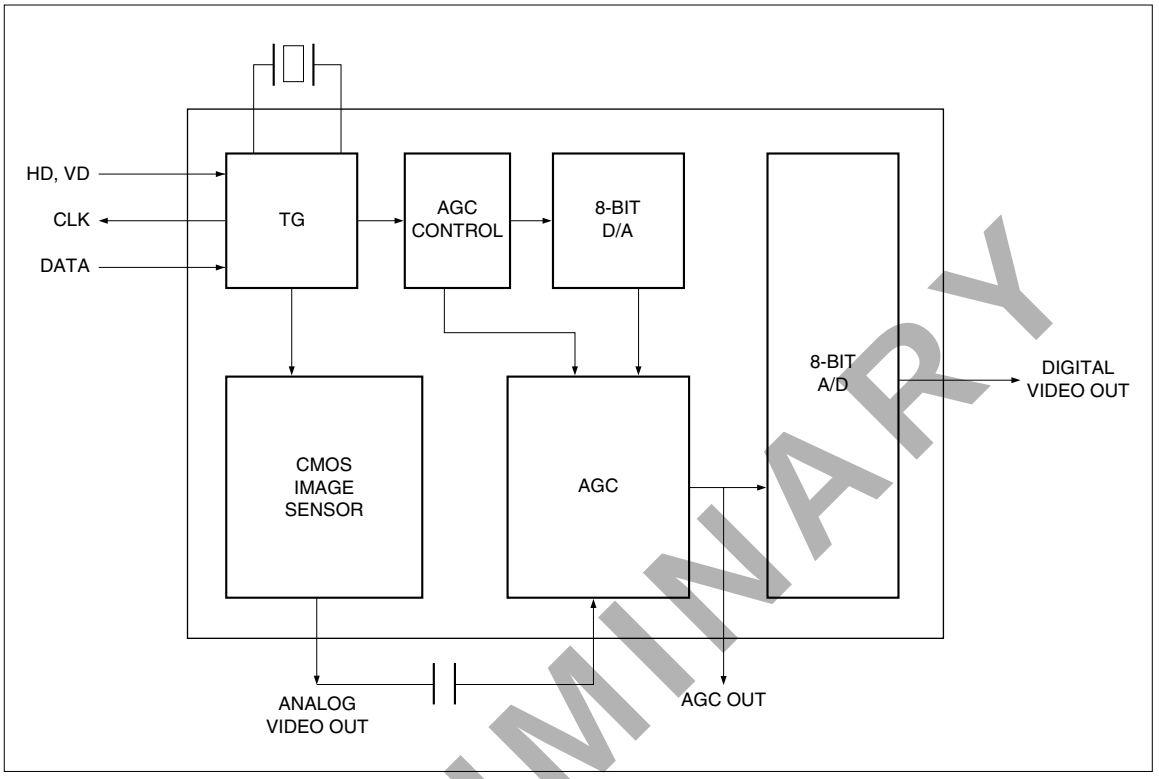


(N-LCC036-S425B)

PRECAUTIONS

- Refer to **"PRECAUTIONS FOR CMOS IMAGE SENSORS"**.

BLOCK DIAGRAM



PIN DESCRIPTION

PIN NO.	SYMBOL	I/O	A/D	DESCRIPTION
1	$BIAS_1$	–	Analog	Analog bias voltage 1 for image sensor
2	AGCOUT	O	Analog	AGC output
3	AGND	–	Analog	Analog ground
4	AV_{DD}	–	Analog	Analog power supply
5	OFS	–	Analog	Offset bias voltage for AGC output
6	ADL	–	Analog	Bottom ADC reference voltage
7	ADH	–	Analog	Top ADC reference voltage
8	NC	–	–	No connection
9	STBY	I	Digital	Standby control mode*
10	AGND	–	Analog	Analog ground
11	AV_{DD}	–	Analog	Analog power supply
12	DGND	–	Digital	Digital ground
13	DV_{DD}	–	Digital	Digital power supply
14	CKI	I	Digital	Clock input for oscillator (12.27 MHz)
15	CKO	O	Digital	Clock output for oscillator
16	D_0	O	Digital	ADC signal output (LSB)
17	D_1	O	Digital	ADC signal output
18	D_2	O	Digital	ADC signal output
19	D_3	O	Digital	ADC signal output
20	D_4	O	Digital	ADC signal output
21	D_5	O	Digital	ADC signal output
22	D_6	O	Digital	ADC signal output
23	D_7	O	Digital	ADC signal output (MSB)
24	CLK	O	Digital	Clock output (6.135 MHz)
25	HD	I	Digital	Horizontal drive pulse input
26	VD	I	Digital	Vertical drive pulse input
27	SDI	I	Digital	Control data input (AGC gain, offset, shutter control, image inversion, etc.)
28	SCLK	I	Digital	Shift clock for data
29	LOAD	I	Digital	Load pulse for data input
30	CLP_2	–	Analog	Analog bias voltage 2 for clamp circuit
31	CLP_1	–	Analog	Analog bias voltage 1 for clamp circuit
32	SIGOUT	O	Analog	Analog image signal output
33	SIGIN	I	Analog	Analog image signal input
34	$BIAS_2$	–	Analog	Analog bias voltage 2 for image sensor
35	REFIN	I	Analog	Reference voltage for analog input
36	NC	–	–	No connection

* Standby mode functions
High level : Standby mode (all circuits power-off), Low level or open : Normal mode (all circuits active)

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT
Power supply voltage	V_{DD}	−0.3 to +4.6	V
Input signal voltage	V_{ϕ}	−0.3 to V_{DD} + 0.3	V
Storage temperature	T_{STG}	−40 to +80	˚C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTE
Power supply voltage		V_{DD}	2.6	2.8	3.0	V	
Operating temperature		T_{OPR}	−20	+25	+50	˚C	
Oscillation frequency	Normal mode	F_{CK}		12.27		MHz	
	Monitoring mode						
Digital input voltage	LOW level	$V_{\phi L}$	0		0.2V_{DD}	V	1
	HIGH level	$V_{\phi H}$	0.8V_{DD}		V_{DD}	V	
Analog input voltage			(Connect to pin through a capacitor)				2
Analog bias voltage			(Connect to GND through a capacitor)				3

NOTES :

1. Applied to input pins STBY, HD, VD, SDI, SCLK and LOAD.
2. Applied to input pins SIGIN and REFIN. Do not connect to DC directly.
3. Applied to pins $BIAS_1$, $BIAS_2$, OFS, ADL, ADH, CLP_1 and CLP_2. Do not connect to GND directly.

CHARACTERISTICS (1/15 s progressive scan readout mode)

(T_A = +25°C, Operating conditions : The typical values specified in "**RECOMMENDED OPERATING CONDITIONS**". Color temperature of light source : 3 200 K, IR cut-off filter (CM-500, 1mmt) is used.)

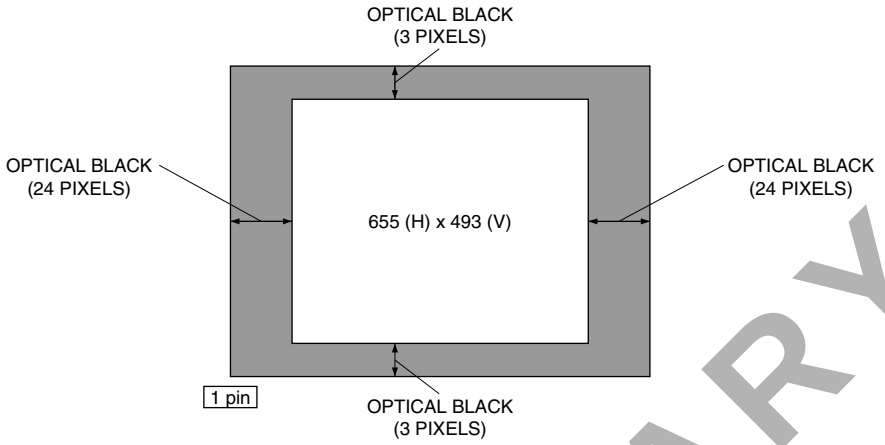
• Measurement point : Analog image signal output (pin No.32), before AGC circuit and AD converter.

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTE
Standard output voltage	V_O		150		mV	1
Photo response non-uniformity	PRNU			14	%	2
Saturation output voltage	V_{SAT}	400	700		mV	3
Dark output voltage	V_{DARK}		2	3	mV	4
Sensitivity (Green channel)	R (G)	150	250		mV	5
Supply current	I_{VDD}		13		mA	6
Standby current	I_{STBY}		1	10	µA	7
Vertical line fixed pattern noise	VFPN		0.5	1.1	mVp-p	8

NOTES :

1. The average output voltage of G signal under uniform illumination. The standard exposure conditions are defined as when V_O is 150 mV.
2. The image area is divided into 10 x 10 segments under the standard exposure conditions. Each segment's voltage is the average output voltage of all pixels within the segment. PRNU is defined by (Vmax – Vmin)/V_O, where Vmax and Vmin are the maximum and minimum values of each segment's voltage respectively.
3. The image area is divided into 10 x 10 segments. Each segment's voltage is the average output voltage of all pixels within the segment. V_{SAT} is the minimum segment's voltage under 10 times exposure of the standard exposure conditions.
4. The difference between average output voltage of the image area and that of the OB area, under non-exposure conditions.
5. The average output voltage of G signal when a 500 lux light source with a 90% reflector is imaged by a lens of F4, F50 mm.
6. Total current of analog and digital power supplies, in the dark and at the standard load conditions.
7. Total current of power supply in standby mode. (Pin No.9 (STBY) is fixed to "H" level and other input pins are fixed to "H" level or "L" level.)
8. One mean horizontal line signal $\langle b_i \rangle$ is obtained by adding all the horizontal line signals $\langle a_{ij} \rangle$ vertically and dividing them by the line number. $\langle x_i \rangle$ is the deviation of the center pixel from the average of successive 5 pixels in $\langle b_i \rangle$. VFPN is the maximum absolute value of $\langle x_i \rangle$.

PIXEL STRUCTURE



COLOR FILTER ARRAY

(1, 493) (655, 493)

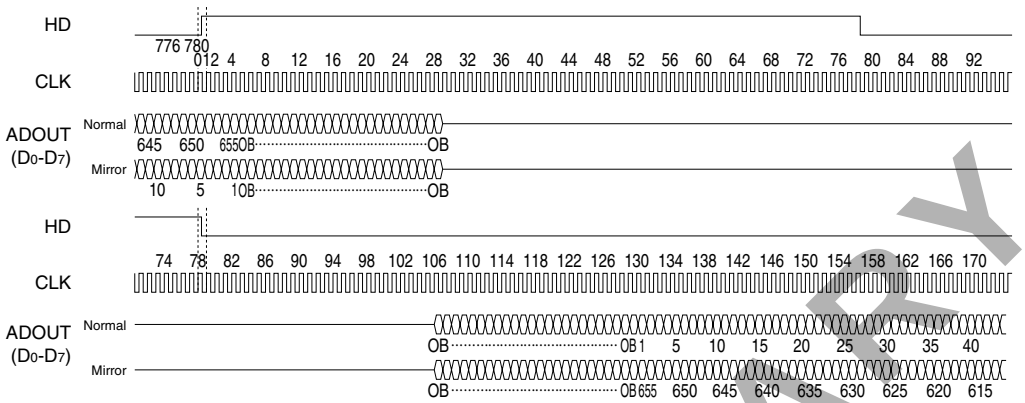
R	G	R	G	R	R	G	R	G	R
G	B	G	B	G	G	B	G	B	G
R	G	R	G	R	R	G	R	G	R
G	B	G	B	G	G	B	G	B	G
R	G	R	G	R	R	G	R	G	R
G	B	G	B	G	G	B	G	B	G
G	B	G	B	G	G	B	G	B	G
R	G	R	G	R	R	G	R	G	R
G	B	G	B	G	G	B	G	B	G
R	G	R	G	R	R	G	R	G	R
G	B	G	B	G	G	B	G	B	G
R	G	R	G	R	R	G	R	G	R

(1, 1) (655, 1)

TIMING CHART

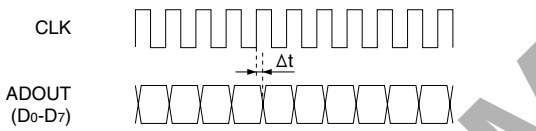
[Normal Mode]

HORIZONTAL PULSE TIMING



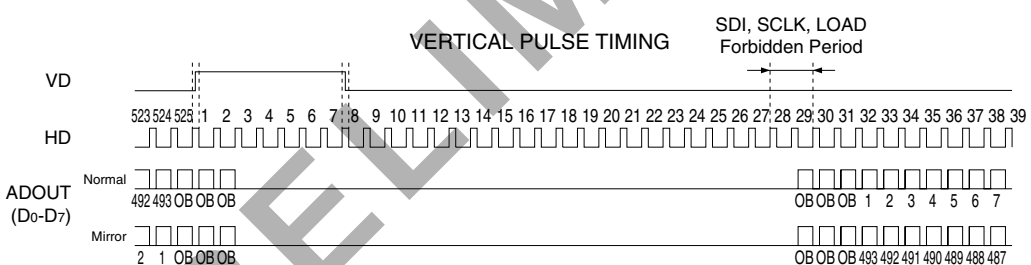
- The rising edge of the HD pulse must be between two rising edges of CLK (0) and CLK (1).
- The falling edge of the HD pulse must be between two rising edges of CLK (78) and CLK (79).

PHASE RELATIONS BETWEEN DIGITAL OUTPUT (ADOUT) AND CLOCK (CLK)



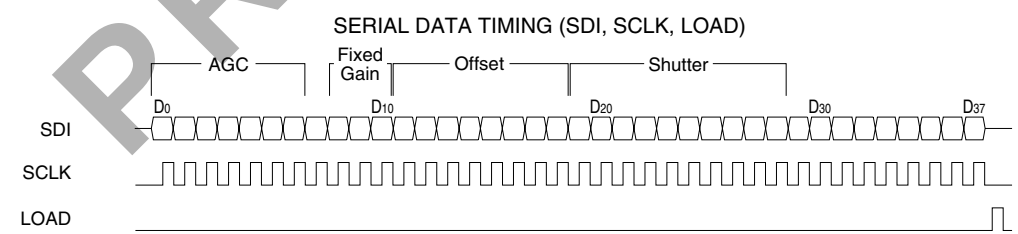
SYMBOL	MIN.	TYP.	MAX.	UNIT
Δt		45		ns

VERTICAL PULSE TIMING



- The rising edge and falling edge of the VD pulse must be in high period of the HD pulses.

SERIAL DATA TIMING (SDI, SCLK, LOAD)

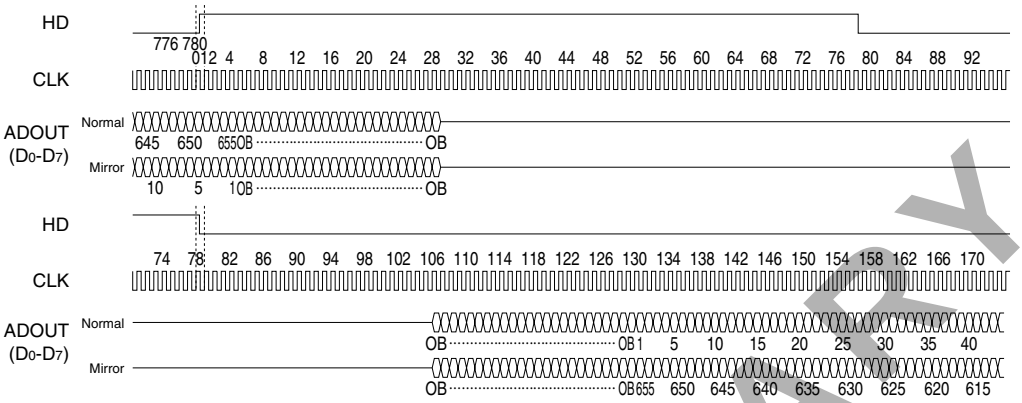


- Data in SDI are taken at the rising edge of SCLK.
- Clock frequency of SCLK should be less than 1/2 of that of CLK.
- Do not insert the SDI, SCLK and LOAD pulses between 28H* and 29H*. Refer to "**VERTICAL PULSE TIMING**".
- Refer to **"SERIAL DATA INPUTS"** for the contents of serial data from D_0 to D_{37}.

* It means ordinal number of the HD pulse.

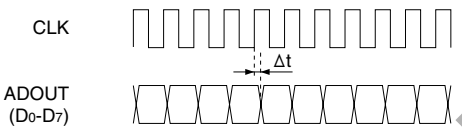
[Monitoring Mode]

HORIZONTAL PULSE TIMING



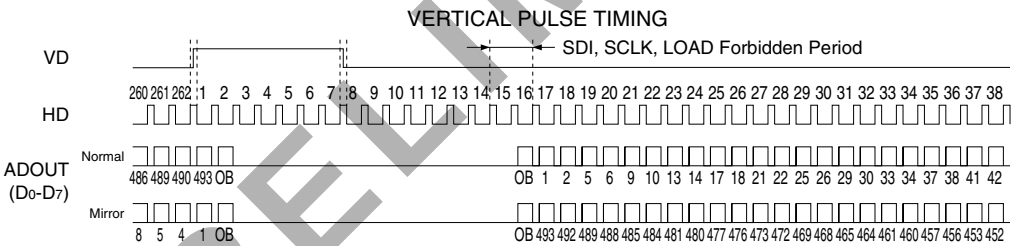
- The rising edge of the HD pulse must be between two rising edges of CLK (0) and CLK (1).
- The falling edge of the HD pulse must be between two rising edges of CLK (78) and CLK (79).

PHASE RELATIONS BETWEEN DIGITAL OUTPUT (ADOUT) AND CLOCK (CLK)



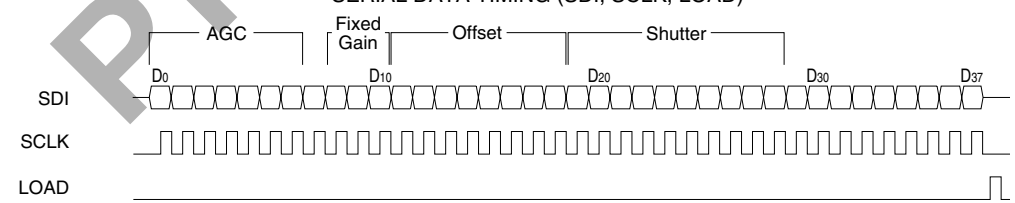
SYMBOL	MIN.	TYP.	MAX.	UNIT
Δt		45		ns

VERTICAL PULSE TIMING



- The rising edge and falling edge of the VD pulse must be in high period of the HD pulses.

SERIAL DATA TIMING (SDI, SCLK, LOAD)



- Data in SDI are taken at the rising edge of SCLK.
- Clock frequency of SCLK should be less than 1/2 of that of CLK.
- Do not insert the SDI, SCLK and LOAD pulses between 15H* and 16H*. Refer to "**VERTICAL PULSE TIMING**".
- Refer to **"SERIAL DATA INPUTS"** for the contents of serial data from D_0 to D_{37}.

* It means ordinal number of the HD pulse.

SERIAL DATA INPUTS

DATA	NAME	FUNCTION
D_0	AGC_6 (MSB)	Auto gain control
D_1	AGC_5	(0 to 20 dB)
D_2	AGC_4	
D_3	AGC_3	
D_4	AGC_2	
D_5	AGC_1	
D_6	AGC_0 (LSB)	
D_7		Not used. (Fix to low level.)
D_8	MAX_2 (MSB)	Selection of fixed gain
D_9	MAX_1	(3 to 10 dB)
D_{10}	MAX_0 (LSB)	
D_{11}	OFS_7 (MSB)	Offset level control of ADC
D_{12}	OFS_6	(0.9 to 1.5 V)
D_{13}	OFS_5	
D_{14}	OFS_4	
D_{15}	OFS_3	
D_{16}	OFS_2	
D_{17}	OFS_1	
D_{18}	OFS_0 (LSB)	
D_{19}	SHT_9 (MSB)	Shutter speed control
D_{20}	SHT_8	(Normal mode : Exposure time is 1 to 1/525 frame period.)
D_{21}	SHT_7	(Monitoring mode : Exposure time is 1 to 1/262 frame period.)
D_{22}	SHT_6	
D_{23}	SHT_5	
D_{24}	SHT_4	
D_{25}	SHT_3	
D_{26}	SHT_2	
D_{27}	SHT_1	
D_{28}	SHT_0 (LSB)	
D_{29}	MIRH	H : Horizontal mirror inversion image, L : Normal image
D_{30}	MIRV	H : Vertical mirror inversion image, L : Normal image
D_{31}	MON	H : Monitoring mode, L : Normal mode
D_{32}	SAD_2 (MSB)	Phase selection of AD clock
D_{33}	SAD_1	$D_{32}/D_{33}/D_{34}$ = L/L/L : −30° $D_{32}/D_{33}/D_{34}$ = L/L/H : −15°
D_{34}	SAD_0 (LSB)	$D_{32}/D_{33}/D_{34}$ = L/H/L : 0° $D_{32}/D_{33}/D_{34}$ = L/H/H : +15°
D_{35}	$LPMD_1$	Power save mode
D_{36}	$LPMD_0$	D_{35}/D_{36} = L/L : Normal mode D_{35}/D_{36} = L/H : AD and AGC off D_{35}/D_{36} = H/L : AD off D_{35}/D_{36} = H/H : Inhibited mode
D_{37}	USB	H : Inhibited mode, L : Normal mode

Setting of Auto Gain Control

- One LSB of the gain code represents approximately 0.156 dB.
- Nominal gain values at typical codes are shown below.

AUTO GAIN CONTROL (dB)	D_0	D_1	D_2	D_3	D_4	D_5	D_6
0	L	L	L	L	L	L	L
1	L	L	L	L	H	H	L
2	L	L	L	H	H	L	H
3	L	L	H	L	L	H	H
4	L	L	H	H	L	L	H
5	L	H	L	L	L	L	L
6	L	H	L	L	H	H	L
7	L	H	L	H	H	L	L
8	L	H	H	L	L	H	H
9	L	H	H	H	L	L	H
10	H	L	L	L	L	L	L
11	H	L	L	L	H	H	L
12	H	L	L	H	H	L	L
13	H	L	H	L	L	H	H
14	H	L	H	H	L	L	H
15	H	L	H	H	H	H	H
16	H	H	L	L	H	H	L
17	H	H	L	H	H	L	L
18	H	H	H	L	L	H	H
19	H	H	H	H	L	L	H
20	H	H	H	H	H	H	H

Setting of Fixed Gain

- One LSB of the gain code represents 1 dB.

FIXED GAIN (dB)	D_8	D_9	D_{10}
3	L	L	L
4	L	L	H
5	L	H	L
6	L	H	H
7	H	L	L
8	H	L	H
9	H	H	L
10	H	H	H

Setting of Offset Level

- One LSB of the offset code represents approximately 0.002 V.
- Nominal offset values at typical codes are shown below.

OFFSET LEVEL (V)	D_{11}	D_{12}	D_{13}	D_{14}	D_{15}	D_{16}	D_{17}	D_{18}
0.9	L	L	L	L	L	L	L	L
1.0	L	L	H	L	H	L	H	H
1.1	L	H	L	H	L	H	L	H
1.2	H	L	L	L	L	L	L	L
1.3	H	L	H	L	H	L	H	L
1.4	H	H	L	H	L	H	L	H
1.5	H	H	H	H	H	H	H	H

Setting of Shutter Speed

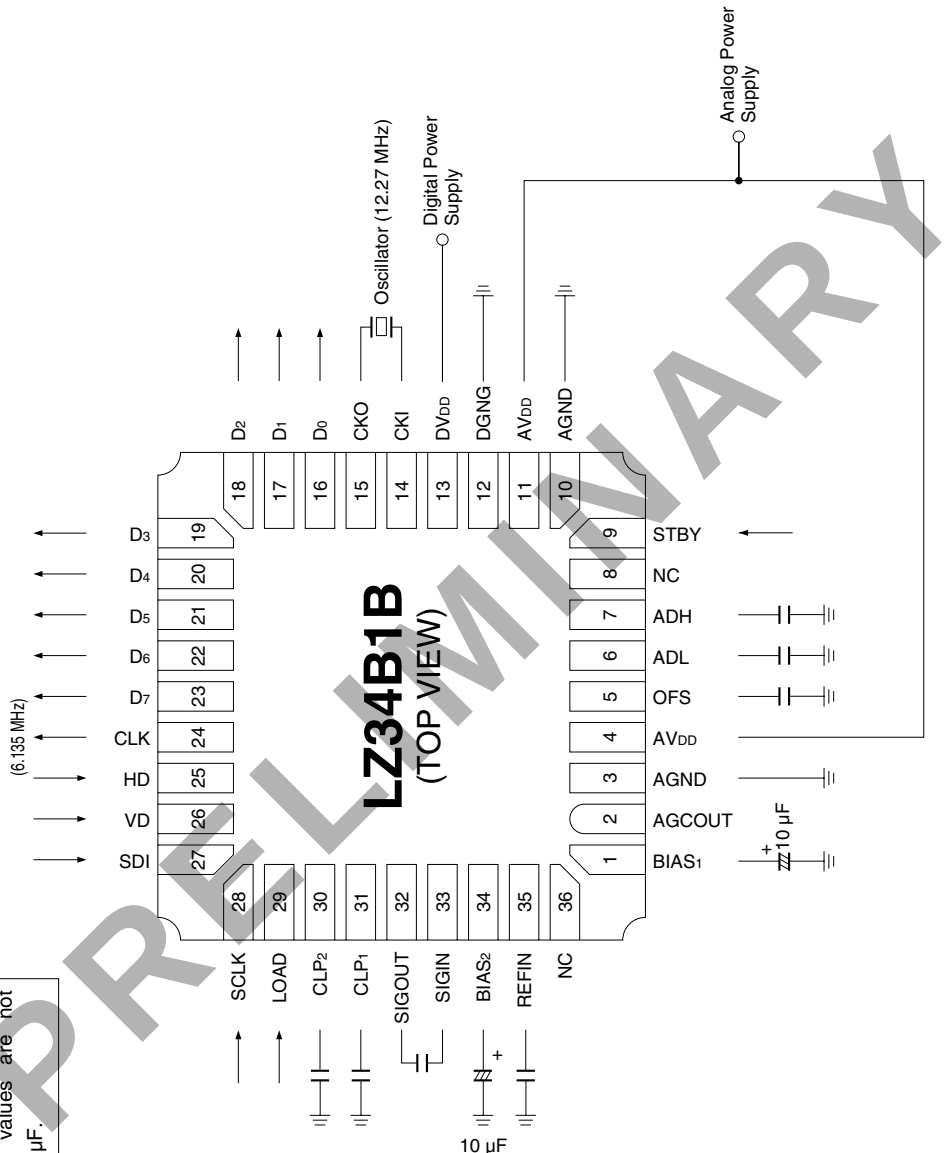
- One LSB of the shutter speed code represents 1H, where 1H is the HD pulse period.
- Shutter speed values at typical codes are shown below in normal mode, monitoring mode and USB mode.

SHUTTER SPEED (Exposure Time Unit : H)		D_{19}	D_{20}	D_{21}	D_{22}	D_{23}	D_{24}	D_{25}	D_{26}	D_{27}	D_{28}
Normal	Monitoring										
525	262	L	L	L	L	L	L	L	L	L	L
•	•										
•	•										
265	2	L	H	L	L	L	L	L	H	L	L
264	1	L	H	L	L	L	L	L	H	L	H
263	262	L	H	L	L	L	L	L	H	H	L
•	•										
•	•										
27	262	L	H	H	H	H	H	L	L	H	L
26	262	L	H	H	H	H	H	L	L	H	H
25	262	L	H	H	H	H	H	L	H	L	L
•	•										
•	•										
2	262	H	L	L	L	L	L	H	L	H	H
1	262	H	L	L	L	L	L	H	H	L	L
525	262	H	L	L	L	L	L	H	H	L	H
•	•										
•	•										
525	262	H	H	H	H	H	H	H	H	H	H

Setting of Driving Modes

FUNCTION	D_{31}	D_{37}
Normal mode	L	L
Monitoring mode	H	L

EXAMPLE OF OPERATION CIRCUIT

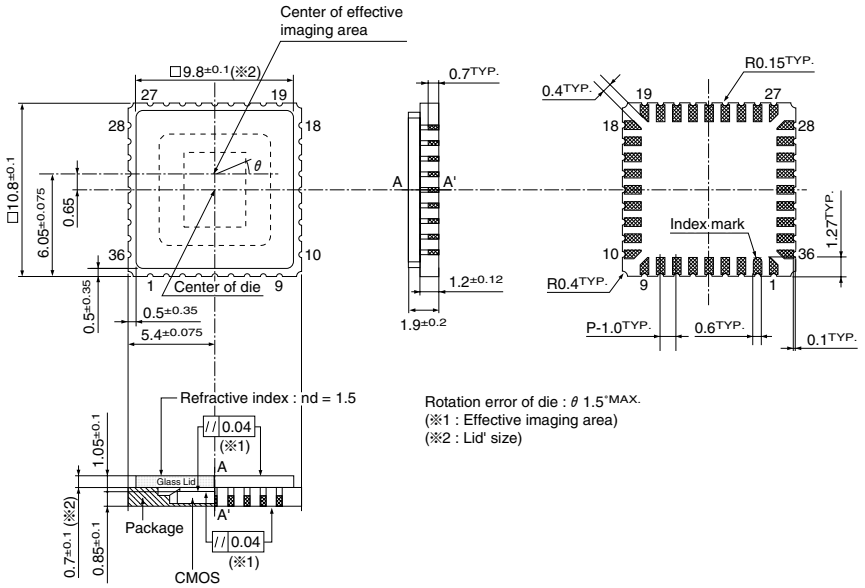


- Insert capacitors more than 10 µF between AV_{DD} and AGND and between DV_{DD} and DGND.
- Capacitors whose values are not shown must be 0.1 µF.

PACKAGE OUTLINES

36 LCC (N-LCC036-S425B)

(Unit : mm)



PRECAUTIONS FOR CMOS IMAGE SENSORS

1. Package Breakage

In order to prevent the package from being broken, observe the following instructions :

1) The CMOS image sensor is a precise optical component and the package material is ceramic.
   Therefore,
   - ● Take care not to drop the device when mounting, handling, or transporting.
   - ● Avoid giving a shock to the package.
     Especially when pins are fixed to the socket or the circuit board, small shock could break the package more easily than when the package isn't fixed.
2) When mounting the package on the housing, be sure that the package is not bent.
   - – If a bent package is forced into place between a hard plate or the like, the package may be broken.
3) If any damage or breakage occurs on the surface of the glass cap, its characteristics could deteriorate.
   Therefore,
   - ● Do not hit the glass cap.
   - ● Do not give a shock large enough to cause distortion.
   - ● Do not scrub or scratch the glass surface.
   - – Even a soft cloth or applicator, if dry, could cause flaws to scratch the glass.

2. Electrostatic Damage

As compared with general MOS-LSI, CMOS image sensor has lower ESD. Therefore, take the following antistatic measures when handling the CMOS image sensor :

1) Always discharge static electricity by grounding the human body and the instrument to be used. To ground the human body, provide resistance of about 1 MΩ between the human body and the ground to be on the safe side.
2) When directly handling the device with the fingers, hold the part without pins and do not touch any pin.
3) To avoid generating static electricity,
   a. do not scrub the glass surface with cloth or plastic.
   b. do not attach any tape or labels.
   c. do not clean the glass surface with dust-cleaning tape.
4) When storing or transporting the device, put it in a container of conductive material.

3. Dust and Contamination

Dust or contamination on the glass surface could deteriorate the output characteristics or cause a scar. In order to minimize dust or contamination on the glass surface, take the following precautions :

1) Handle the CMOS image sensor in a clean environment such as a cleaned booth. (The cleanliness level should be, if possible, class 1 000 at least.)
2) Do not touch the glass surface with the fingers. If dust or contamination gets on the glass surface, the following cleaning method is recommended :
   - ● Dust from static electricity should be blown off with an ionized air blower. For anti-electrostatic measures, however, ground all the pins on the device before blowing off the dust.
   - ● The contamination on the glass surface should be wiped off with a clean applicator soaked in isopropyl alcohol. Wipe slowly and gently in one direction only.
   - – Frequently replace the applicator and do not use the same applicator to clean more than one device.

※ Note : In most cases, dust and contamination are unavoidable, even before the device is first used. It is, therefore, recommended that the above procedures should be taken to wipe out dust and contamination before using the device.

4. Other

1) Soldering should be manually performed within 2 seconds per pin at 400°C maximum at the tip of soldering iron.
2) Avoid using or storing the CMOS image sensor at high temperature or high humidity as it is a precise optical component. Do not give a mechanical shock to the CMOS image sensor.
3) Do not expose the device to strong light. For the color device, long exposure to strong light will fade the color of the color filters.