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## **M5M29KB/T331ATP**

33,554,432-BIT (4,194,304-WORD BY 8-BIT /2,097,152-WORD BY 16-BIT)
CMOS 3.3V-ONLY, BLOCK ERASE FLASH MEMORY

#### **DESCRIPTION**

The M5M29KB/T331ATP are 3.3V-only high speed 33,554,432-bit CMOS boot block FLASH Memories with alternating BGO(Back Ground Operation) feature. The BGO feature of the device allows Program or Erase operations to be performed in one bank while the device simultaneously allows Read operations to be performed on the other bank.

This BGO feature is suitable for mobile and personal computing, and communication products.

The M5M29KB/T331ATP are fabricated by CMOS technology for the peripheral circuit and DINOR IV(Divided bit-line NOR IV) architecture for the memory cell, and are available in a 52-pin TSOP(II) for lead free use.

M5M29KB/T331ATP provides for Software Lock Release function. Usually, all memory blocks are locked and can not be programmed or erased, when WP# is low. Using Software Lock Release function, program or erase operation can be executed.

#### **FEATURES**

Access time Random 70ns (Max.) Page 25ns(Max.)

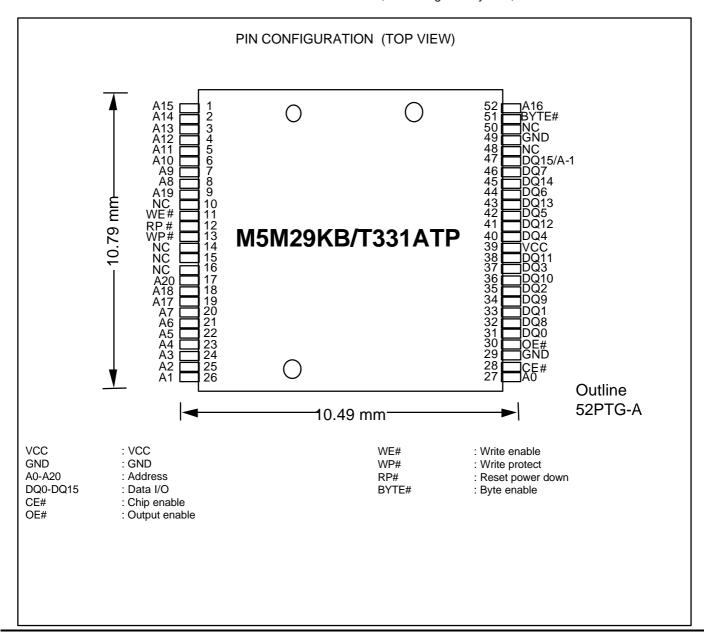
Supply voltage  $VCC = 3.0 \sim 3.6V$ Ambient temperature  $Ta=-40 \sim 85$  °C

Package 52pin TSOP(Type-II), Lead pitch 0.4mm

Outer-lead finishing: Sn-Cu

#### **APPLICATION**

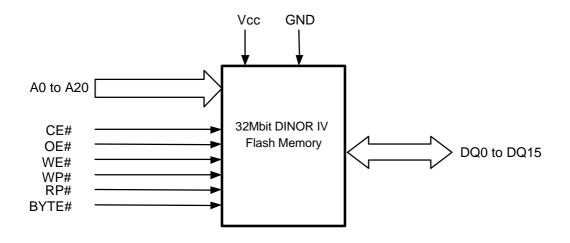
Digital Cellar Phone, Telecommunication, PDA, Car Navigation System, Video Game Machine



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CMOS 3.3V-ONLY, BLOCK ERASE FLASH MEMORY

## 32M Flash Memory Block Diagram



### Capacitance

Symbol		Parameter	Conditions		Unit			
Cymbol		r dramotor	Conditions	Min.	Тур.	Max.	Onne	
CIN	Input	A20-A0, OE#, WE#, CE#, WP#,				12	pF	
CIIV	capacitance	RP#,BYTE#	Ta=25°C, f=1MHz,			12	Pi	
COUT	Output	DQ15-DQ0	Vin=Vout=0V			12	pF	
	Capacitance	DQ15-DQ0				12	рг	

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CMOS 3.3V-ONLY, BLOCK ERASE FLASH MEMORY

### **Flash Memory Part**

### **Description**

The 32M-bit DINOR IV(Divided bit line NOR IV) Flash Memory is 3.3V-only high speed 33,554,432-bit CMOS boot block Flash Memory. Alternating BGO(Back Ground Operation) feature of the device allows Program or Erase operations to be performed in one bank while the device simultaneously allows Read operations to be performed on the other bank. This BGO feature is suitable for communication products and cellular phone. The Flash Memory is fabricated by CMOS technology for the peripheral circuits and DINOR IV architecture for the memory cells.

- Auto Erase

Erase time Main Block 150ms/block (typ.)

Erase unit

Bank(I)

Bank(II)

Bank(III)

Parameter Block 4K-word x6 / 8K-byte x6

Main Block 32K-word x7 / 64K-byte x7

Main Block 32K-word x8 / 64K-byte x8

Main Block 32K-word x24 / 64K-byte x24

4K-word x2/8K-byte x2

Bank(IV) Main Block 32K-word x24 / 64K-byte x24

- Program/Erase cycles 100Kcycles

**Boot Block** 

- Boot Block

Bottom Boot M\*\*\*B33\*\*\*\*\*\*

Top Boot M\*\*\*T33\*\*\*\*\*\*

- The Other Functions

Software Command Control

Software Lock Release(while WP# is low)

Erase Suspend/Resume Program Suspend/Resume Status Register Read

Alternating Back Ground Program/Erase Operation Between Bank(I), Bank(II), Bank(III) and Bank(IV)

Random Page Read

#### **Features**

-Organization 2,097,152-word x 16-bit

4,194,304-byte x 8-bit

- Supply Voltage VCC = 3.0 ~ 3.6V

- Access time

Random Access 70ns(Max.)
Random Page Read 25ns(Max.)

- Read 108mW (Max. at 5MHz)

- Page Read 36mW (Max.)

(After Automatic Power Down) 0.33µW(typ.)

- Program/Erase 126mW(Max.)

Standby 0.33µW(typ.)

Deep Power Down mode 0.33µW(typ.)

- Auto Program for Bank(I) - Bank(IV)

**Program Time** 

Word Program 30µs/word(typ.)

Byte Program 30µs/byte(typ.)

Page Program 4ms(typ.)

Program Unit

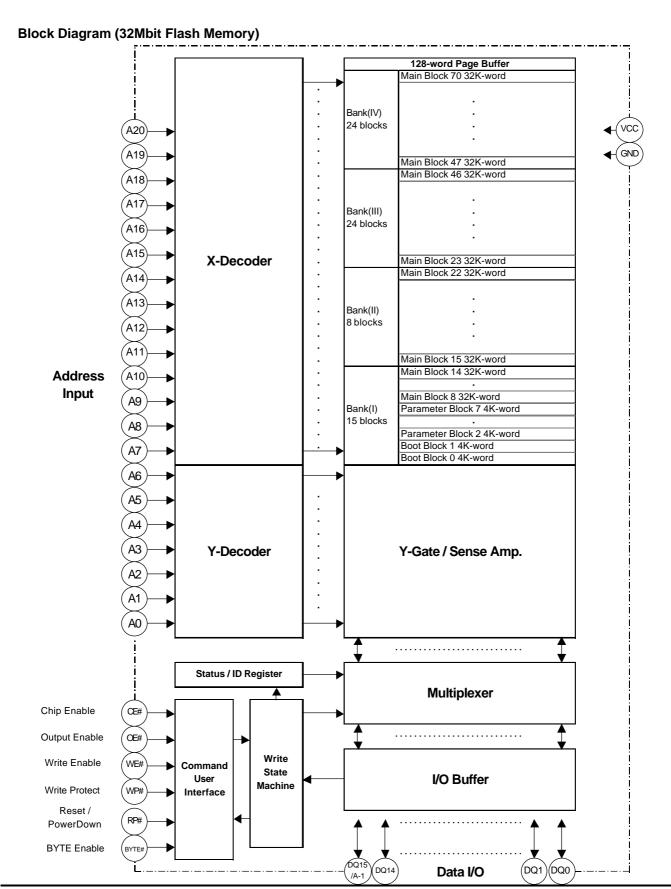
Word/Byte Program 1word/ 1Byte

Page Program 128 words/ 256 bytes

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CMOS 3.3V-ONLY, BLOCK ERASE FLASH MEMORY

### **Function of Flash Memory**

The 32M-bit DINOR IV Flash Memory includes on-chip program/erase control circuitry. The Write State Machine (WSM) controls block erase and word/page program operations. Operational modes are selected by the commands written to the Command User Interface (CUI). The Status Register indicates the status of the WSM and when the WSM successfully completes the desired program or block erase operation.

A Deep Power Down mode is enabled when the RP# pin is at GND, minimizing power consumption.

#### Read

The 32M-bit DINOR IV Flash Memory has four read modes, which accesses to the memory array, the Page Read, the Device Identifier and the Status Register. The appropriate read commands are required to be written to the CUI. Upon initial device power up or after exit from deep power down, the 32M-bit DINOR IV Flash Memory automatically resets to read array mode. In the read array mode and in the conditions are low level input to OE#, high level input to WE# and RP#, low level input to CE# and address signals to the address inputs (A20 - A0: Word mode / A20-A-1: Byte mode) the data of the addressed location to the data input/output (DQ15-DQ0: Word mode / DQ7- DQ0: Byte mode) is output.

### Write

Writes to the CUI enables reading of memory array data, device identifiers and reading and clearing of the Status Register. They also enable block erase and program. The CUI is written by bringing WE# to low level and OE# is at high level, while CE# is at low level. Address and data are latched on the earlier rising edge of WE# and CE#. Standard micro processor write timings are used.

#### Alternating Background Operation (BGO)

The 32M-bit DINOR IV Flash Memory allows to read array from one bank while the other bank operates in software command write cycling or the erasing / programming operation in the background. Array Read operation with the other bank in BGO is performed by changing the bank address without any additional command. When the bank address points the bank in software command write cycling or the erasing / programming operation, the data is read out from the status register. The access time with BGO is the same as the normal read operation. BGO must be between Bank(I), Bank(III) and Bank(IV).

### **Output Disable**

When OE# is at VIH, output from the devices is disabled. Data input/output are in a high-impedance (High-Z) state.

### **Standby**

When CE# is at VIH, the device is in the standby mode and its power consumption is reduced. Data input/output are in a high-impedance (High-Z) state. If the memory is deselected during block erase or program, the internal control circuits remain active and the device consumes normal active power until the operation completes.

### **Deep Power Down**

When RP# is at VIL, the device is in the deep power down mode and its power consumption is substantially low. During read modes, the memory is deselected and the data input/output are in a high-impedance (High-Z) state. After return from power down, the CUI is reset to Read Array, and the Status Register is cleared to value 80H.

During block erase or program modes, RP# low will abort either operation. Memory array data of the block being altered become invalid.

### **Automatic Power Down (Auto-PD)**

The Automatic Power Down minimizes the power consumption during read mode. The device automatically turns to this mode when any addresses or CE# isn't changed more than 200ns after the last alternation. The power consumption becomes the same as the stand-by mode. During this mode, the output data is latched and can be read out. New data is read out correctly when addresses are changed.

#### BBR(Back Bank array Read)

In the 32M-bit DINOR IV Flash Memory , when one memory address is read according to a Read Mode in the case of the same as an access when a Read Mode command is input, an another Bank memory data can be read out (Random or Page Mode) by changing an another Bank address.



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CMOS 3.3V-ONLY, BLOCK ERASE FLASH MEMORY

#### **Software Command Definitions**

The device operations are selected by writing specific software command into the Command User Interface.

### Read Array Command (FFH)

The device is in Read Array mode on initial device power up and after exit from deep power down, or by writing FFH to the Command User Interface. After starting the internal operation the device is set to the read status register mode automatically.

### Read Device Identifier Command (90H)

We can normally read device identifier codes when Read Device Identifier Code Command (90H) is written to the command latch. Following the command write, the manufacturer code and the device code can be read from A0 address 0H and 1H in a bank address, respectively.

### Read Status Register Command (70H)

The Status Register is read after writing the Read Status Register command of 70H to the Command User Interface. Also, after starting the internal operation the device is set to the Read Status Register mode automatically.

The contents of Status Register are latched on the later falling edge of OE# or CE#. When status read is required, OE# or CE# must be toggled every status read.

#### Page Read Command (F3H)

The Page Read command (F3H) timing can be used by writing the first command and CE# falls VIL or changing the address(A20-A2) is necessary to start activating page read mode. This command is fast random 4 words read. During the read cycle operation it is necessary to fix CE# low and change addresses which are defined by A0 and A1(or A-1 to A1) at random continuously.

The mode is kept until RP# is set to VIL or this chip is powered down.

The first read of Page Read timing is the same as normal read (ta(CE)). CE# should be fallen VIL. The read timing after the first is fast read (ta(PAD)).

In the page read mode the upper address(A20-A2) is supposed not to be clocked during read operation. Otherwise the access time is as same as normal read.

### Clear Status Register Command (50H)

The Erase Status, Program Status and Block Status bits are set to "1"s by the Write State Machine and can only be reset by the Clear Status Register command of 50H. These bits indicate various failure conditions.

### Block Erase / Confirm Command (20H/D0H)

Automated block erase is initiated by writing the Block Erase command of 20H followed by the Confirm command of D0H. An address within the block to be erased is required. The WSM executes iterative erase pulse application and erase verify operation.

### **Program Commands**

### A) Word / Byte Program (40H)

Word / Byte program is executed by a two-command sequence. The Word/Byte program Setup command of 40H is written to the Command Interface, followed by a second write specifying the address and data to be written. The WSM controls the program pulse application and verify operation.

### B) Page Program for Data Blocks (41H)

Page Program allows fast programming of 128 words/256 bytes of data. Writing of 41H initiates the page program operation for the Data area. From 2nd cycle to 129th cycle(Word mode)/257th cycle(Byte mode), write data must be serially inputted. Address A6-A0(Word mode)/A6-A-1(Byte mode) have to be incremented from 00H to 7FH. After completion of data loading, the WSM controls the program pulse application and verify operation.

#### C) Single Data Load to Page Buffer (74H)

### / Page Buffer to Flash (0EH/D0H)

Single data load to the page buffer is performed by writing 74H followed by a second write specifying the column address (A6 to A0 or A6 to A-1) and data. Distinct data up to 128word can be loaded to the page buffer by this two-command sequence. On the other hand, all of the loaded data to the page buffer is programmed simultaneously by writing Page Buffer to Flash command of 0EH followed by the confirm command of D0H. After completion of programming the data on the page buffer is cleared automatically.



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CMOS 3.3V-ONLY, BLOCK ERASE FLASH MEMORY

### Flash to Page Buffer Command (F1H/D0H)

Array data load to the page buffer is performed by writing the Flash to Page Buffer command of F1H followed by the Confirm command of D0H. An address within the page to be loaded is required. Then the array data can be copied into the other pages within the same bank by using the Page Buffer to Flash command.

### Clear Page Buffer Command (55H/D0H)

Loaded data to the page buffer is cleared by writing the Clear Page Buffer command of 55H followed by the Confirm command of D0H. This command is valid for clearing data loaded by Single Data Load to Page Buffer command.

#### **Data Protection**

The 32M-bit DINOR IV Flash Memory has a master Write Protect pin (WP#). When WP# is at VIH, all blocks can be programmed or erased. When WP# is low, all blocks are in locked mode which prevents any modifications to memory blocks. Software Lock Release function is only command which allows to program or erase.

### Suspend/Resume Command (B0H/D0H)

Writing the Suspend command of B0H during block erase operation interrupts the block erase operation and allows read out from another block of memory. Writing the Suspend command of B0H during program operation interrupts the program operation and allows read out from another block of memory. The Bank address is required when writing the Suspend/Resume Command. The device continues to output Status Register data when read, after the Suspend command is written to it. Polling the WSM Status and Suspend Status bits will determine when the erase operation or program operation has been suspended. At this point, writing of the Read Array command to the CUI enables reading data from blocks other than that which is suspended. When the Resume command of D0H is written to the CUI, the WSM will continue with the erase or program processes.

#### **Erase All Unlocked Blocks Command (A7H/D0H)**

The command sequence enable us to erase all blocks. The command can be used by writing Setup command A7H(1st cycle) and confirm command D0H(2nd cycle). The sequence is not valid in case of WP#=VIL.

### **Power Supply Voltage**

When the power supply voltage is less than VLKO, Low VCC Lock-Out voltage, the device is set to the Read-only mode.

A delay time of 2µs is required before any device operation is initiated. The delay time is measured from the time Flash VCC reaches Flash VCCmin (3.0V).

During power up, RP# = GND is recommended. Falling in Busy status is not recommended for possibility of damaging the device.

### **Memory Organization**

The 32M-bit DINOR IV Flash Memory is constructed by 2 boot blocks of 4K words/ 8K bytes, 6 parameter blocks of 4K words/ 8K bytes and 7 main blocks of 32K words/ 64K bytes in Bank(I), by 8 main blocks of 32K words/ 64K bytes in Bank(II) and by 24 main blocks of 32K words/ 64K bytes in Bank(III) and Bank(IV).



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CMOS 3.3V-ONLY, BLOCK ERASE FLASH MEMORY

### **Block Organization**

## 32M-bit DINOR(IV) Flash Memory Map (Bottom Boot)

Mode   Mode   180000H   18000H	x8 (Byte	x16 (Word	
BBFFFFH	-		
1AFFFFH D7FFFH 190000H 19FFFFH C7FFFH 190000H 19FFFFH C7FFFH 19FFFFH 190000H 190000H 19FFFFH 190000H 19FFFFH 190000H 190000H 19FFFFH 19FFFH 190000H 190000H 190000H 19FFFFH 19FFFH 19FFFH 190000H 1900			32Kw ord MAIN BLOCK 34
190000+ 19FFFFH CFFFFH 190000+ 19FFFFFH C7FFFH 17FFFH BFFFFH 17FFFH BFFFFH 160000+ 18FFFFH AFFFFH 180000+ 18FFFFH AFFFFH 180000+ 18FFFFH BFFFFH 180000+ 180000+ 18FFFFH BFFFFH 180000+ 180000+ 180000+ 180000+ 18FFFFH BFFFH 180000+			32Kw ord MAIN BLOCK 33
18000H- 18FFFFH C7FFFH 18F0FFH BFFFFH 160000H- 10FFFFH BFFFFH 160000H- 10FFFFH BFFFFH 160000H- 16FFFFH BFFFFH 150000H- 16FFFFH BFFFFH 150000H- 16FFFFH AFFFFH 150000H- 16FFFFH AFFFFH 140000H- 16FFFFH AFFFFH 120000H- 18FFFFH SFFFFH 120000H- 18FFFFH SFFFFH 120000H- 18FFFFH SFFFFH 10000H- 18FFFFH SFFFFH 10000H- 16FFFFH SFFFFH 10000H- 16FFFFH SFFFFH 10000H- 10FFFFH SFFFFH 10000H- 10FFFFH SFFFFH 10000H- 10FFFFH SFFFFH 10000H- 10000H- 10FFFFH SFFFFH 10000H- 10000H- 10FFFFH SFFFFH 10000H- 10000H- 10FFFFH SFFFFH 10000H- 1			
18FFFFH C7FFFH BF000H 170000H B8000H 17FFFFH BFFFFH BF7FFH 180000H B0000H 15FFFFH AF0FFFH 150000H A8000H 15FFFFH AF0FFFH 140000H A0000H 15FFFFH AF0FFFH 140000H A7000H 15FFFFH AF0FFFH 140000H A7000H 15FFFFH AF0FFFH 140000H A7000H 12FFFFH AF0FFFH 120000H 90000H 12FFFFH 97FFFH 120000H 90000H 12FFFFH 87FFFH 100000H 80000H 16FFFFH 87FFFH 100000H 70000H 16FFFFH 70000H 16FFFFH 70000H 16FFFH 70000H 16FFFFH 70000H 16FFFH 70000H 16FFFFH 70000H 16FFFFH 70000H 16FFFH 7	19FFFFH	CFFFFH	32Kw ord MAIN BLOCK 32
170000H 17FFFFH BFFFFH 160000H 160000H 16FFFH B7FFFH 150000H 15FFFFH AFFFFH 140000H 140000H 14000H 13FFFFH AFFFFH 120000H 13FFFFH 9F0FFH 120000H 12000H 1200H 12000H 12000H 12000H 12000H 12000H 12000H 12000H 12000H 12000H			32Kw ord MAIN BLOCK 31
160000H 16FFFFH B7FFFH 16F0000H 16FFFFH A8F00H 15FFFFH A8F0FH 140000H 14FFFFH A7FFFH 14FFFH A7FFFH 132KW ord MAIN BLOCK 28 132KW ord MAIN BLOCK 27 13000H 13FFFFH 97FFFH 120000H 12FFFFH 97FFFH 110000H 12FFFFH 97FFFH 12FFFH 12FFFH 97FFFH 12FFFH 97FFH 12FFFH 97FFFH 12FFFH 97FFFH 12FFFH 97FFFH 12FFFH 97FFFH	170000H-	B8000H-	
150000H 15FFFFH 15FFFFH 15FFFFH 14FFFFH 150000H 13FFFFH 15FFFH 15FFFH 15FFFH 15FFFH 15FFFH 15FFFH 10000H 1000H 10000H 10000H 10000H 10000H 10000H 10000H 10000H 10000H 1000H 100H 1000H 100H 1000H 100H 1000H			32KW OID IVIAIN BLOCK 30
15FFFFH AFFFFH A7FFFH A7F7FH A77FFH A			32Kw ord MAIN BLOCK 29
14FFFFH A7FFFH 130000H- 98000H- 12FFFFH 9FFFFH 32KW ord MAIN BLOCK 26 12000H- 90000H- 12FFFFH 8FFFFH 32KW ord MAIN BLOCK 25 110000H- 88000H- 10FFFFH 8FFFFH 32KW ord MAIN BLOCK 24 132KW ord MAIN BLOCK 24 132KW ord MAIN BLOCK 24 132KW ord MAIN BLOCK 25 132KW ord MAIN BLOCK 25 132KW ord MAIN BLOCK 25 132KW ord MAIN BLOCK 26 132KW ord MAIN BLOCK 27 132KW ord MAIN BLOCK 21 132KW ord MAIN BLOCK 20 132KW ord MAIN BLOCK 21 132KW ord MAIN BLOCK 20 132KW ord MAIN BLOCK 20 132KW ord MAIN BLOCK 21 132KW ord MAIN BLOCK 20 132KW ord MAIN BLOCK 30 132KW ord MAIN BLOCK 40 132KW ord MAIN BLOCK 50 132KW ord MAIN BLOC	15FFFFH		32Kw ord MAIN BLOCK 28
13FFFFH 9FFFH 120000H- 9000H- 11FFFFH 8FFFFH 8F0000H- 8000H- 10000H- 87000H- 8			32Kw ord MAIN BLOCK 27
12000H- 12FFFFH 97FFFH 110000H- 18000H- 11000H- 18000H- 10FFFFH 87FFFH 10FFFFH 77FFFH 10FFFFH 77FFFH 10FFFFH 77FFFH 10FFFFH 87FFFH 10FFFFH 87FFFH 10FFFFH 87FFFH 10FFFFH 87FFFH 10FFFFH 87FFFH 10FFFFH 87FFFFH 10FFFFH 87FFFH 10FFFFH 87FFFH 10FFFFH 87FFFH 10FFFFH 87FFFH 10FFFFH 87FFFH 10FFFH 87FFFH 10FFFFH 87FFFH 10FFFFH 87FFFH 10FFFFH 87FFFH 10FFFH 87FFFH 10FFFH	130000H-	98000H-	
12FFFFH 87FFFH 88FFFH 100000H- 88000H- 10FFFFH 87FFFH 87FFFH 87FFFH 32KW ord MAIN BLOCK 24 100000H- 78000H- 78000H- 770000H- 770000H- 88000H- 780000H- 88000H- 780000H- 88000H- 780000H- 88000H- 787FFFH 37FFFH 32KW ord MAIN BLOCK 20 32KW ord MAIN BLOCK 19 32KW ord MAIN BLOCK 19 32KW ord MAIN BLOCK 19 32KW ord MAIN BLOCK 17 32KW ord MAIN BLOCK 16 32KW ord MAIN BLOCK 17 32KW ord MAIN BLOCK 17 32KW ord MAIN BLOCK 16 32KW ord MAIN BLOCK 15 32KW ord MAIN BLOCK 15 32KW ord MAIN BLOCK 15 32KW ord MAIN BLOCK 16 32KW ord MAIN BLOCK 11 32KW ord MAIN BLOCK 12 32KW ord MA	13FFFFH	9FFFFH	32Kw ord MAIN BLOCK 26
110000H 11FFFFH 10000H 1000H 10000H 1000H 10000H 1000H 10000H 100			OOK MAIN DI OOK OF
11FFFFH 8FFFH 100000H- 80000H- 17000H-			32KW ord MAIN BLOCK 25
10000H- 10FFFH 87FFH 87FFH 87FFH 77FFFH 77FFH 77FFFH 77FFH 77FH 77FH 77FH 77FH 77FH 77FH 77FH 77FH 77FH 77FFH 77F			32Kw ord MAIN BLOCK 24
10FFFFH 87FFFH 70000H- FFFFFH 77FFFH 77FFH 77FFH 77FFH 77FFFH 77FFFH 77FFFH 77FFH 77FFFH 77FFH 77F			32KW OIU WAIN BLOCK 24
### STEFFH   32Kw ord MAIN BLOCK 22			32Kw ord MAIN BLOCK 23
EFFFFH         77FFFH         32Kw ord MAIN BLOCK 21           D0000H-         68000H-         32Kw ord MAIN BLOCK 20           C0000H-         68000H-         68000H-           CFFFFH         67FFFH         32Kw ord MAIN BLOCK 19           B0000H-         58000H-         58000H-           BFFFFH         57FFFH         32Kw ord MAIN BLOCK 18           A0000H-         58000H-         32Kw ord MAIN BLOCK 17           90000H-         48000H-         32Kw ord MAIN BLOCK 16           80000H-         47FFFH         32Kw ord MAIN BLOCK 15           70000H-         38000H-         32Kw ord MAIN BLOCK 15           70000H-         38000H-         32Kw ord MAIN BLOCK 14           60000H-         30000H-         32Kw ord MAIN BLOCK 13           50000H-         28000H-         32Kw ord MAIN BLOCK 12           40000H-         2000H-         32Kw ord MAIN BLOCK 11           30000H-         10000H-         32Kw ord MAIN BLOCK 10           20000H-         10000H-         32Kw ord MAIN BLOCK 11           32Kw ord MAIN BLOCK 10         32Kw ord MAIN BLOCK 10           40000H-         3000H-         32Kw ord MAIN BLOCK 10           40000H-         3000H-         32Kw ord MAIN BLOCK 10           40			32Kw ord MAIN BLOCK 22
DOUOOH-		, 00001	22Kw ard MAIN PLOCK 21
C0000H- CFFFFH 67FFFH B0000H- BFFFFH 5FFFFFH B0000H- SB000H- SB000H- SB000H- SBFFFFH 5FFFFFH B0000H- AFFFFH 5FFFFFH B0000H- B0000H- B0000H- B0000H- B0000H- B0000H- B0000H- B0000H- BFFFFH 4FFFFFH B0000H- B0000H- B0000H- B0000H- B0000H- B0000H- B0000H- B0000H- B0000H- B000H- B00H- B000H- B0			32RW OID IVIAIN BLOCK 21
CFFFFH         67FFFH           B0000H-         58000H-           BFFFFH         5FFFFH           A0000H-         58000H-           AFFFFH         57FFFH           90000H-         48000H-           9FFFFH         4FFFFH           32Kw ord MAIN BLOCK 16           80000H-         48000H-           9FFFFH         47FFFH           70000H-         38000H-           7FFFFH         3FFFFH           32Kw ord MAIN BLOCK 15           30000H-         38000H-           5FFFFH         3FFFFH           32Kw ord MAIN BLOCK 14           60000H-         30000H-           5FFFFH         3FFFFH           32Kw ord MAIN BLOCK 13           32Kw ord MAIN BLOCK 12           40000H-         2000H-           4FFFFH         32Kw ord MAIN BLOCK 11           32Kw ord MAIN BLOCK 11         32Kw ord MAIN BLOCK 10           32Kw ord MAIN BLOCK 10         32Kw ord MAIN BLOCK 10           40000H-         3000H-           4FFFFH         32Kw ord MAIN BLOCK 10           32Kw ord MAIN BLOCK 11         32Kw ord MAIN BLOCK 10           4FFFFH         32Kw ord MAIN BLOCK 1           4Kword PARAMETER BLOCK 2 <td></td> <td>-</td> <td>32Kw ord MAIN BLOCK 20</td>		-	32Kw ord MAIN BLOCK 20
BFFFFH         5FFFFH         32Kw ord MAIN BLOCK 18           A0000H-         50000H-         32Kw ord MAIN BLOCK 17           90000H-         49000H-         32Kw ord MAIN BLOCK 16           80000H-         49000H-         32Kw ord MAIN BLOCK 15           70000H-         38000H-         32Kw ord MAIN BLOCK 15           70000H-         30000H-         32Kw ord MAIN BLOCK 14           60000H-         30000H-         32Kw ord MAIN BLOCK 13           50000H-         28000H-         32Kw ord MAIN BLOCK 12           40000H-         20000H-         32Kw ord MAIN BLOCK 11           30000H-         18000H-         32Kw ord MAIN BLOCK 11           32Kw ord MAIN BLOCK 11         32Kw ord MAIN BLOCK 10           32Kw ord MAIN BLOCK 10         32Kw ord MAIN BLOCK 10           32Kw ord MAIN BLOCK 10         32Kw ord MAIN BLOCK 6           40000H-         32Kw ord MAIN BLOCK 6           40000H-         32Kw ord MAIN BLOCK 7           40000H-         32Kw ord MAIN BLOCK 8           40000H-         32Kw ord MAIN BLOCK 6           40000H-         46kword PARAMETER BLOCK 7           40000H-         46kword PARAMETER BLOCK 6           40000H-         46kword PARAMETER BLOCK 4           40000H-         46kword PARAMETER BLO		000001	32Kw ord MAIN BLOCK 19
AFFFFH         57FFFH         32Kw ord MAIN BLOCK 17           90000H-         49000H-         32Kw ord MAIN BLOCK 16           80000H-         40000H-         32Kw ord MAIN BLOCK 15           70000H-         38000H-         32Kw ord MAIN BLOCK 14           60000H-         30000H-         32Kw ord MAIN BLOCK 14           60000H-         32Kw ord MAIN BLOCK 13           50000H-         28000H-           5FFFFH         27FFFH           32Kw ord MAIN BLOCK 12           40000H-         20000H-           4FFFFH         27FFFH           32Kw ord MAIN BLOCK 11           30000H-         18000H-           32FFFFH         17FFFH           32Kw ord MAIN BLOCK 10           32Kw ord MAIN BLOCK 5           32Kw ord MAIN BLOCK 6           4Kword PARAMETER BLOCK 7           4Kword PARAMETER BLOCK 6           4Kword PARAMETER BLOCK 6           4Kword PARAMETER BLOCK 6           4Kword PARAMETER BLOCK 6           4Kword PARAMETER BLOCK 1           4Kword PARAMETER BLOCK 1           4Kword PARAMETER BLOCK 2           4Kword PARAMETER BLOCK 1			32Kw ord MAIN BLOCK 18
90000H 48000H 9FFFFH 4FFFFH 32Kw ord MAIN BLOCK 16 80000H 40000H 3000H 7FFFFH 3FFFFH 32Kw ord MAIN BLOCK 15 70000H 30000H 30000H 37FFFH 32Kw ord MAIN BLOCK 14 60000H 20000H 28000H 32Kw ord MAIN BLOCK 13 50000H 20000H 27FFFH 32Kw ord MAIN BLOCK 12 40000H 20000H 30000H 32Kw ord MAIN BLOCK 11 32Kw ord MAIN BLOCK 12 32Kw ord MAIN BLOCK 11 32Kw ord MAIN BLOCK 11 32Kw ord MAIN BLOCK 11 32Kw ord MAIN BLOCK 10 45FFFH 17FFFH 32Kw ord MAIN BLOCK 9 32Kw ord MAIN BLOCK 10 45FFFH 07FFFH 32Kw ord MAIN BLOCK 9 45W ord MAIN BLOCK 9 45W ord MAIN BLOCK 6 45W ord MAIN BLOCK 6 45W ord MAIN BLOCK 8 45W ord MAIN BLOCK 6 45W ord MAIN BLOCK 6 45W ord MAIN BLOCK 6 45W ord MAIN BLOCK 7 45W ord MAIN BLOCK 7 45W ord MAIN BLOCK 8 45W ord MAIN BLOCK 9 45W ord MAIN BLOCK 10 45W ord MAIN BLOCK 11 45W ord PARAMETER BLOCK 2 45W ord MAIN BLOCK 11 45W ord PARAMETER BLOCK 2 45W ord PARAMETER BLOCK 2 45W ord BOOT BLOCK 1 45W ord BOOT BLOCK 1			32Kw ord MAIN BLOCK 17
80000H 8FFFFH 47FFH 47FFFH 47FFFH 70000H 38000H 7FFFFFH 3000H 3000H 8FFFFFH 37FFFFH 37FFFFH 37FFFFH 3000H 28000H 28000H 28000H 28000H 28000H 28000H 28000H 30000H 32Kw ord MAIN BLOCK 12  32Kw ord MAIN BLOCK 11  32Kw ord MAIN BLOCK 11  32Kw ord MAIN BLOCK 10  32Kw ord MAIN BLOCK 50  32Kw ord MAIN BLOCK 10  48Word PARAMETER BLOCK 6  48Word PARAMETER BLOCK 1			
8FFFFH         47FFFH         32Kw ord MAIN BLOCK 15           70000H-         38000H-         35FFFH         32Kw ord MAIN BLOCK 14           60000H-         30000H-         32Kw ord MAIN BLOCK 13         32Kw ord MAIN BLOCK 13           50000H-         28000H-         32Kw ord MAIN BLOCK 12           40000H-         20000H-         32Kw ord MAIN BLOCK 11           30000H-         18000H-         32Kw ord MAIN BLOCK 10           32FFFFH         1FFFFH         32Kw ord MAIN BLOCK 10           20000H-         10000H-         32Kw ord MAIN BLOCK 9           10000H-         08000H-         32Kw ord MAIN BLOCK 8           10FFFH         0FFFFH         32Kw ord MAIN BLOCK 9           10000H-         08000H-         32Kw ord MAIN BLOCK 9           10000H-         07000H-         32Kw ord MAIN BLOCK 9           10000H-         07000H-         4Kword PARAMETER BLOCK 6           0A000H-         08000H-         4Kword PARAMETER BLOCK 6           0A000H-         03000H-         4Kword PARAMETER BLOCK 4           06000H-         03FFFH         4Kword PARAMETER BLOCK 3           04000H-         02FFFH         4Kword PARAMETER BLOCK 2           02FFFH         02FFFH         4Kword PARAMETER BLOCK 2 <td< td=""><td></td><td></td><td>32Kw ord MAIN BLOCK 16</td></td<>			32Kw ord MAIN BLOCK 16
7FFFFH 3FFFH 60000H- 30000H- 6FFFFH 2FFFFH 37FFFH 32KW ord MAIN BLOCK 13  32KW ord MAIN BLOCK 13  32KW ord MAIN BLOCK 12  32KW ord MAIN BLOCK 12  32KW ord MAIN BLOCK 11  32KW ord MAIN BLOCK 10  32KW ord MAIN BLOCK 10  32KW ord MAIN BLOCK 10  32KW ord MAIN BLOCK 6  32KW ord MAIN BLOCK 6  4KWord PARAMETER BLOCK 7  4KWord PARAMETER BLOCK 6  4KWORD PARAMETER BLOCK 1	8FFFFH	47FFFH	32Kw ord MAIN BLOCK 15
6FFFFH 37FFFH 32KW ord MAIN BLOCK 13 50000H- 28000H- 4FFFFH 2FFFFH 32KW ord MAIN BLOCK 12 40000H- 20000H- 4FFFFH 27FFFH 32KW ord MAIN BLOCK 11 30000H- 18000H- 2FFFFH 1FFFFH 32KW ord MAIN BLOCK 10 20000H- 10000H- 2FFFFH 0FFFFH 32KW ord MAIN BLOCK 9 10000H- 08000H- 0FFFFH 0FFFFH 32KW ord MAIN BLOCK 8 10000H- 07000H- 0FFFFH 07FFFH 4Kword PARAMETER BLOCK 7 10000H- 08000H- 0BFFFH 05FFFH 4Kword PARAMETER BLOCK 6 10000H- 03000H- 0BFFFH 04FFFH 4Kword PARAMETER BLOCK 5 10000H- 03000H- 07FFFH 03FFFH 4Kword PARAMETER BLOCK 3 10000H- 03000H- 03FFFH 03FFFH 4KWord PARAMETER BLOCK 3 10000H- 03000H- 03FFFH 03FFFH 4KWord PARAMETER BLOCK 3 10000H- 03000H- 03FFFH 03FFFH 03FFFH 4KWord BOOT BLOCK 1 10000H- 03000H- 03FFFH 03FFH 03			32Kw ord MAIN BLOCK 14
50000H 28000H 32KW ord MAIN BLOCK 12 40000H 20000H 32KW ord MAIN BLOCK 11 32KW ord MAIN BLOCK 11 32KW ord MAIN BLOCK 11 32KW ord MAIN BLOCK 10 32KW ord MAIN BLOCK 8 32KW ord MAIN BLOCK 9 32KW ord MAIN BLOCK 9 46000H 07000H 07000H 07000H 07FFFH 07FFH 0			33Kw ord MAIN BLOCK 13
40000H 4FFFFH 27FFFH 3000H 3000H 18000H 30FFFFH 1FFFFFH 10000H 10000H 2FFFFFH 10000H 10000H 2FFFFFH 10000H 10000H 2FFFFFH 10000H 1000H			321W Old WAIN BEGGIN 13
4FFFFH 27FFFH 30000H- 18000H- 1FFFH 1FFFFH 17FFFH 10000H- 17FFFH 10000H- 17FFFH 10000H- 17FFFH 10000H- 17FFFH 10000H- 17FFFH 10FFFFH 10FFFH 10FFFFH 10FFFH 10FFFFH 10FFFH 10			32Kw ord MAIN BLOCK 12
30000H- 18000H- 32Kw ord MAIN BLOCK 10 20000H- 10000H- 32Kw ord MAIN BLOCK 9 10000H- 08000H- 0FFFFH 0FFFFH 0FFFFH 0FFFFH 0FFFFH 0FFFFH 0FFFFH 0FFFFH 0FFFFH 0FFFH			32Kw ord MAIN BLOCK 11
20000H- 10000H- 2FFFFH 17FFFH 10000H- 08000H- 10000H- 07000H- 06000H- 07000H- 06000H-			
2FFFFH 17FFFH 10000H- 08000H- 10000H- 07000H-	3FFFFH	1FFFFH	32Kw ord MAIN BLOCK 10
10000H 08000H 1FFFFH 0FFFFH 0FFFFH 0C000H-07000H-06			22Kw ord MAIN PLOCK 0
1FFFFH 0FFFFH 0F000H- 07000H- 07000H- 07000H- 08000H- 08000H- 08000H- 08000H- 08000H- 08000H- 08000H- 08000H- 08000H- 04000H- 04000H- 04000H- 03000H- 03000H- 07FFFH 03FFFH 4Kword PARAMETER BLOCK 5 08000H- 07FFFH 03FFFH 4Kword PARAMETER BLOCK 4 04000H- 02000H- 07FFFH 02FFFH 4Kword PARAMETER BLOCK 3 04000H- 02000H- 01000H- 02000H- 01000H- 03000H- 030			32KW OIG WAIN BLOCK 9
0E000H- 07000H- 0707FFH 0C000H- 06000H- 06000H- 05000H- 05000H- 05000H- 05000H- 05000H- 05000H- 05000H- 05000H- 04000H- 04000H- 04000H- 04000H- 03000H- 03000H- 07FFFH 03FFFH 04FFFH 04FFFH 04FFFH 04FFFH 04F0H- 04000H- 02000H- 02000H- 02000H- 03000H- 02000H- 03000H- 02000H- 03000H- 03000			32Kw ord MAIN BLOCK 8
0C000H- 0DFFFH         066FFFH         4Kword PARAMETER BLOCK 6           0A000H- 0BFFFH         05FFFH         4Kword PARAMETER BLOCK 5           08000H- 09FFFH         04FFFH         4Kword PARAMETER BLOCK 4           06000H- 06000H- 07FFFH         03FFFH         4Kword PARAMETER BLOCK 3           04000H- 05FFFH         02FFFH         4Kword PARAMETER BLOCK 3           04000H- 03FFFH         02FFFH         4Kword PARAMETER BLOCK 2           02000H- 03FFFH         01FFFH         4Kw ord BOOT BLOCK 1           00000H- 01FFFH         00FFFH         4Kw ord BOOT BLOCK 0			
0DFFFH         06FFFH         4Kword PARAMETER BLOCK 6           0A000H-         055000H-         4Kword PARAMETER BLOCK 5           08000H-         04000H-         4Kword PARAMETER BLOCK 4           06000H-         03000H-         4Kword PARAMETER BLOCK 4           06000H-         03000H-         4Kword PARAMETER BLOCK 3           04000H-         0200H-         4Kword PARAMETER BLOCK 2           0200H-         0100H-         4Kword PARAMETER BLOCK 2           0300H-         0300H-         4Kword PARAMETER BLOCK 2           04000H-         04000H-         4Kword PARAMETER BLOCK 2           05FFFH         04FFFH         4Kword PARAMETER BLOCK 3           04FFFH         04FFFH         4Kword PARAMETER BLOCK 3           05FFFH         04FFFH         4Kword PARAMETER BLOCK 3           04FFFH         04FFFH         4Kword PARAMETER BLOCK 3	OFFFFH	07FFFH	4Kword PARAMETER BLOCK 7
0A000H- 05000H- 05000H- 04000H- 05000H- 04000H- 04000H- 03000H- 03000H- 07FFFH 03FFFH 045FFFH 045FFH 04			4Kword BARAMETER BLOCK 6
08000H- 04000H- 04000H- 04000H- 04000H- 03000H- 035FFH 045FFH 025FFH 025FFH 025FFH 025FFH 045Word PARAMETER BLOCK 3 04000H- 035FFH 015FFH 045FFH 045F			4KWOIGT AKAWIETEK BEGOKO
09FFFH         04FFFH         4Kword PARAMETER BLOCK 4           06000H-         03000H-         03FFFH           04000H-         0200H-         02FFFH           05FFFH         02FFFH         4Kword PARAMETER BLOCK 2           02000H-         01000H-           03FFFH         01FFFH           0000H-         0000H-           01FFFH         00FFFH           A20-A-1         A20-A0			4Kword PARAMETER BLOCK 5
06000H 03000H 07FFFH 03FFFH 4Kword PARAMETER BLOCK 3 04000H 02000H 05FFFH 02FFFH 4Kword PARAMETER BLOCK 2 02000H 01000H 03FFFH 01FFFH 4Kw ord BOOT BLOCK 1 00000H 00000H 00FFFH 4Kw ord BOOT BLOCK 0 A20-A-1 A20-A0	08000H-	04000H-	
07FFFH         03FFFH         4Kword PARAMETER BLOCK 3           04000H-         02000H-         02FFFH           05FFFH         02FFFH         4Kword PARAMETER BLOCK 2           02000H-         01FFFH         4Kw ord BOOT BLOCK 1           00000H-         00000H-         00000H-           01FFFH         00FFFH         4Kw ord BOOT BLOCK 0           A20-A-1         A20-A0			4Kword PARAMETER BLOCK 4
05FFFH         02FFFH         4Kword PARAMETER BLOCK 2           02000H-         01000H-         4Kw ord BOOT BLOCK 1           03FFFH         0000H-         4Kw ord BOOT BLOCK 0           01FFFH         4Kw ord BOOT BLOCK 0			4Kword PARAMETER BLOCK 3
02000H- 01000H- 03FFFH 01FFFH 4Kw ord BOOT BLOCK 1 00000H- 00000H- 00FFFH 4Kw ord BOOT BLOCK 0 4Kw ord BOOT BLOCK 0	04000H-	02000H-	
03FFFH 01FFFH 4KW ord BOOT BLOCK 1 00000H- 00000H- 01FFFH 00FFFH A20-A1 A20-A0			4Kword PARAMETER BLOCK 2
00000H- 00000H- 01FFFH 00FFFH 4Kw ord BOOT BLOCK 0 A20-A-1 A20-A0			4Kw ord BOOT BLOCK 1
01FFFH 00FFFH 4Kw ord BOOT BLOCK 0 4Kw ord BOOT BLOCK 0			Sid BOOT BEOOK T
A20-A-1 A20-A0			4Kw ord BOOT BLOCK 0
(D. to Made) (Mord Made)	A20-A-1		

	x8 (Byte	x16 (Word
	Mode)	Mode)
	3F0000H- 3FFFFFH	1F8000H- 1FFFFFH
	3E0000H-	1F0000H-
	3EFFFFH	1F7FFFH
	3D0000H-	1E8000H-
	3DFFFFH	1EFFFFH
	3C0000H- 3CFFFFH	1E0000H- 1E7FFFH
	3B0000H-	1D8000H-
	3BFFFFH	1DFFFFH
0	3A0000H- 3AFFFFH	1D0000H- 1D7FFFH
Ź	390000H-	1C8000H-
<u> </u>	39FFFFH	1CFFFFH
┋	380000H- 38FFFFH	1C0000H- 1C7FFFH
	370000H-	1B8000H-
	37FFFFH	1BFFFFH
	360000H- 36FFFFH	1B0000H- 1B7FFFH
	350000H-	1A8000H-
	35FFFFH	1AFFFFH
	340000H-	1A0000H-
	34FFFFH 330000H-	1A7FFFH 198000H-
	33FFFFH	19FFFFH
	320000H-	190000H-
	32FFFFH	197FFFH 188000H-
	310000H- 31FFFFH	18FFFFH
Ū	300000H-	180000H-
>	30FFFFH	187FFFH
É	2F0000H- 2FFFFFH	178000H- 17FFFFH
È	2E0000H-	170000H-
	2EFFFFH	177FFFH
	2D0000H- 2DFFFFH	168000H- 16FFFFH
	2C0000H-	160000H-
	2CFFFFH	167FFFH
	2B0000H- 2BFFFFH	158000H- 15FFFFH
	2A0000H-	150000H-
	2AFFFFH	157FFFH
	290000H- 29FFFFH	148000H- 14FFFFH
	280000H-	140000H-
	28FFFFH	147FFFH
	270000H-	138000H-
_	27FFFFH 260000H-	13FFFFH 130000H-
>	26FFFFH	137FFFH
2	250000H-	128000H-
	25FFFFH 240000H-	12FFFFH 120000H-
7	24FFFFH	127FFFH
	230000H-	118000H-
	23FFFFH	11FFFFH
	220000H- 22FFFFH	110000H- 117FFFH
	210000H-	108000H-
	21FFFFH	10FFFFH
	200000H- 20FFFFH	100000H- 107FFFH
	1F0000H-	F8000H-
	1FFFFFH	FFFFFH
	1E0000H- 1EFFFFH	F0000H- F7FFFH
	1D0000H-	E8000H-
	1DFFFFH	EFFFFH
	1C0000H-	E0000H-
	1CFFFFH A20-A-1	E7FFFH A20-A0
	(Byte Mode)	(Word Mod

_
32Kw ord MAIN BLOCK 70
32Kw ord MAIN BLOCK 69
32Kw ord MAIN BLOCK 68
32Kw ord MAIN BLOCK 67
32Kw ord MAIN BLOCK 66
32Kw ord MAIN BLOCK 65
32Kw ord MAIN BLOCK 64
32Kw ord MAIN BLOCK 63
32Kw ord MAIN BLOCK 62
32Kw ord MAIN BLOCK 61
32Kw ord MAIN BLOCK 60
32Kw ord MAIN BLOCK 59
32Kw ord MAIN BLOCK 58
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32Kw ord MAIN BLOCK 51
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32Kw ord MAIN BLOCK 48
32Kw ord MAIN BLOCK 47
32Kw ord MAIN BLOCK 46
32Kw ord MAIN BLOCK 45
32Kw ord MAIN BLOCK 44
32Kw ord MAIN BLOCK 43
32Kw ord MAIN BLOCK 42
32Kw ord MAIN BLOCK 41
32Kw ord MAIN BLOCK 40
32Kw ord MAIN BLOCK 39
32Kw ord MAIN BLOCK 38
32Kw ord MAIN BLOCK 37
32Kw ord MAIN BLOCK 36
32Kw ord MAIN BLOCK 35

BANK(IV)

SANK(III)

(Byte Mode)

(Word Mode)

(Byte Mode) (Word Mode)

Notice: This is not a final specification. Some parametric limits are subject to change.

# **M5M29KB/T331ATP**

33,554,432-BIT (4,194,304-WORD BY 8-BIT /2,097,152-WORD BY 16-BIT) CMOS 3.3V-ONLY, BLOCK ERASE FLASH MEMORY

#### **Block Organization** 32M-bit DINOR(IV) Flas

ock Orga	mzation	32W-DIT DINOR(IV
x8 (Byte	x16 (Word	
Mode) 230000H-	Mode) 118000H-	OOK IMAIN DI OOK OF
23FFFFH 220000H-	11FFFFH 110000H-	32Kword MAIN BLOCK 35
22FFFFH	117FFFH	32Kword MAIN BLOCK 34
210000H- 21FFFFH	108000H- 10FFFFH	32Kword MAIN BLOCK 33
200000H- 20FFFFH	100000H- 107FFFH	32Kword MAIN BLOCK 32
1F0000H- 1FFFFFH	F8000H- FFFFFH	32Kword MAIN BLOCK 31
1E0000H-	F0000H-	
1EFFFFH 1D0000H-	F7FFFH E8000H-	32Kword MAIN BLOCK 30
1DFFFFH 1C0000H-	EFFFFH E0000H-	32Kword MAIN BLOCK 29
1CFFFFH	E7FFFH	32Kword MAIN BLOCK 28
1B0000H- 1BFFFFH	D8000H- DFFFFH	32Kword MAIN BLOCK 27
1A0000H- 1AFFFFH	D0000H- D7FFFH	32Kword MAIN BLOCK 26
190000H-	C8000H-	32Kword MAIN BLOCK 25
19FFFFH 180000H-	CFFFFH C0000H-	
18FFFFH 170000H-	C7FFFH B8000H-	32Kword MAIN BLOCK 24
17FFFFH	BFFFFH	32Kword MAIN BLOCK 23
160000H- 16FFFFH	B0000H- B7FFFH	32Kword MAIN BLOCK 22
150000H- 15FFFFH	A8000H- AFFFFH	32Kword MAIN BLOCK 21
140000H- 14FFFFH	A0000H- A7FFFH	32Kword MAIN BLOCK 20
130000H-	98000H-	32Kword MAIN BLOCK 19
13FFFFH 120000H-	9FFFFH 90000H-	
12FFFFH 110000H-	97FFFH 88000H-	32Kword MAIN BLOCK 18
11FFFFH	8FFFFH	32Kword MAIN BLOCK 17
100000H- 10FFFFH	80000H- 87FFFH	32Kword MAIN BLOCK16
F0000H- FFFFFH	78000H- 7FFFFH	32Kword MAIN BLOCK 15
E0000H- EFFFFH	70000H- 77FFFH	32Kword MAIN BLOCK 14
D0000H-	68000H- 6FFFFH	32Kword MAIN BLOCK 13
DFFFFH C0000H-	60000H-	
CFFFFH B0000H-	67FFFH 58000H-	32Kword MAIN BLOCK 12
BFFFFH A0000H-	5FFFFH 50000H-	32Kword MAIN BLOCK 11
AFFFFH	57FFFH	32Kword MAIN BLOCK 10
90000H- 9FFFFH	48000H- 4FFFFH	32Kword MAIN BLOCK 9
80000H- 8FFFFH	40000H- 47FFFH	32Kword MAIN BLOCK 8
70000H- 7FFFFH	38000H- 3FFFFH	32Kword MAIN BLOCK 7
60000H-	30000H-	
6FFFFH 50000H-	37FFFH 28000H-	32Kword MAIN BLOCK 6
5FFFFH 40000H-	2FFFFH 20000H-	32Kword MAIN BLOCK 5
4FFFFH	27FFFH	32Kword MAIN BLOCK 4
30000H- 3FFFFH	18000H- 1FFFFH	32Kword MAIN BLOCK 3
20000H- 2FFFFH	10000H- 17FFFH	32Kword MAIN BLOCK 2
10000H-	08000H-	32Kword MAIN BLOCK 1
1FFFFH 00000H-	OFFFFH 00000H-	
0FFFFH A20-A-1 (Byte	07FFFH A20-A0 (Word	32Kword MAIN BLOCK 0
Mode)	Mode)	

sh Memo	ry Map (	Top Boot)
x8 (Byte	x16 (Word	
Mode)	Mode)	
3FE000H-	1FF000H-	414   10007.0
3FFFFFH	1FFFFFH	4Kword BOOT B
3FC000H-	1FE000H-	416
3FDFFFH	1FEFFFH	4Kword BOOT B
3FA000H-	1FD000H-	416 marel DADAMETER
3FBFFFH 3F8000H-	1FDFFFH	4Kword PARAMETER
3F9FFFH	1FC000H- 1FCFFFH	4Kword PARAMETER
3F6000H-	1FB000H-	-i Wold i 7 ii V ii Vill I Li I
3F7FFFH	1FBFFFH	4Kword PARAMETER
3F4000H-	1FA000H-	
3F5FFFH	1FAFFFH	4Kword PARAMETER
3F2000H-	1F9000H-	
3F3FFFH	1F9FFFH	4Kword PARAMETER
3F0000H-	1F8000H-	ALC: Level DADAMETER
3F1FFFH 3E0000H-	1F8FFFH 1F0000H-	4Kword PARAMETER
3EFFFFH	1F7FFFH	32Kword MAIN E
3D0000H-	1E8000H-	
3DFFFFH	1EFFFFH	32Kword MAIN E
3C0000H-	1E0000H-	
3CFFFFH	1E7FFFH	32Kword MAIN E
3B0000H-	1D8000H-	0014 1144111
3BFFFFH	1DFFFFH	32Kword MAIN E
3A0000H-	1D0000H-	32Kword MAIN E
3AFFFFH	1D7FFFH	32KWOIU IVIAIIN E
390000H- 39FFFFH	1C8000H- 1CFFFFH	32Kword MAIN E
380000H-	1C0000H-	OZITIVOTO IVIJ III V Z
38FFFFH	1C7FFFH	32Kword MAIN E
370000H-	1B8000H-	
37FFFFH	1BFFFFH	32Kword MAIN E
360000H-	1B0000H-	
36FFFFH	1B7FFFH	32Kword MAIN E
350000H-	1A8000H-	2017 word MAIN F
35FFFFH	1AFFFFH	32Kword MAIN E
340000H- 34FFFFH	1A0000H- 1A7FFFH	32Kword MAIN E
330000H-	198000H-	OZI (WOIG IVI) (II V Z
33FFFFH	19FFFFH	32Kword MAIN E
320000H-	190000H-	
32FFFFH	197FFFH	32Kword MAIN E
310000H-	188000H-	0014
31FFFFH	18FFFFH	32Kword MAIN E
300000H-	180000H-	32Kword MAIN E
30FFFFH	187FFFH	32KWOIU IVIAIIN E
2F0000H- 2FFFFFH	178000H- 17FFFFH	32Kword MAIN E
2E0000H-	170000H-	02:11:0:0:1::::::::::
2EFFFFH	177FFFH	32Kword MAIN E
2D0000H-	168000H-	
2DFFFFH	16FFFFH	32Kword MAIN E
2C0000H-	160000H-	0014
2CFFFFH	167FFFH	32Kword MAIN E
2B0000H-	158000H-	32Kword MAIN E
2BFFFFH	15FFFFH	32KWOIU WAIN L
2A0000H- 2AFFFFH	150000H- 157FFFH	32Kword MAIN E
290000H-	148000H-	02:1110:0:1111111111
29FFFFH	14FFFFH	32Kword MAIN E
280000H-	140000H-	
28FFFFH	147FFFH	32Kword MAIN E
270000H-	138000H-	OOK and MANINE
27FFFFH	13FFFFH	32Kword MAIN E
260000H- 26FFFFH	130000H-	32Kword MAIN E
250000H-	137FFFH 128000H-	OZITWOIU IVIAIN E
25FFFFH	128000FF 12FFFFH	32Kword MAIN E
240000H-	120000H-	
24FFFFH	127FFFH	32Kword MAIN E
A20-A-1 (Byte	A20-A0 (Word	
Mode)	Mode)	

4Kword BOOT BLOCK 70  4Kword BOOT BLOCK 69  4Kword PARAMETER BLOCK 68  4Kword PARAMETER BLOCK 66  4Kword PARAMETER BLOCK 66  4Kword PARAMETER BLOCK 63  32Kword PARAMETER BLOCK 63  32Kword MAIN BLOCK 61  32Kword MAIN BLOCK 59  32Kword MAIN BLOCK 57  32Kword MAIN BLOCK 55  32Kword MAIN BLOCK 55  32Kword MAIN BLOCK 54  32Kword MAIN BLOCK 55  32Kword MAIN BLOCK 54  32Kword MAIN BLOCK 55  32Kword MAIN BLOCK 54  32Kword MAIN BLOCK 54  32Kword MAIN BLOCK 51  32Kword MAIN BLOCK 51  32Kword MAIN BLOCK 50  32Kword MAIN BLOCK 49  32Kword MAIN BLOCK 49  32Kword MAIN BLOCK 48  32Kword MAIN BLOCK 48  32Kword MAIN BLOCK 44  32Kword MAIN BLOCK 41  32Kword MAIN BLOCK 41  32Kword MAIN BLOCK 40  32Kword MAIN BLOCK 40  32Kword MAIN BLOCK 39  32Kword MAIN BLOCK 37  32Kword MAIN BLOCK 37  32Kword MAIN BLOCK 37		
4Kword PARAMETER BLOCK 68 4Kword PARAMETER BLOCK 66 4Kword PARAMETER BLOCK 65 4Kword PARAMETER BLOCK 64 4Kword PARAMETER BLOCK 64 4Kword PARAMETER BLOCK 63 32Kword MAIN BLOCK 61 32Kword MAIN BLOCK 60 32Kword MAIN BLOCK 59 32Kword MAIN BLOCK 57 32Kword MAIN BLOCK 55 32Kword MAIN BLOCK 55 32Kword MAIN BLOCK 54 32Kword MAIN BLOCK 55 32Kword MAIN BLOCK 55 32Kword MAIN BLOCK 55 32Kword MAIN BLOCK 54 32Kword MAIN BLOCK 55 32Kword MAIN BLOCK 54 32Kword MAIN BLOCK 54 32Kword MAIN BLOCK 54 32Kword MAIN BLOCK 49 32Kword MAIN BLOCK 48 32Kword MAIN BLOCK 47 32Kword MAIN BLOCK 44 32Kword MAIN BLOCK 43 32Kword MAIN BLOCK 40 32Kword MAIN BLOCK 40 32Kword MAIN BLOCK 40 32Kword MAIN BLOCK 39 32Kword MAIN BLOCK 38	4Kword BOOT BLOCK 70	
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32Kword MAIN BLOCK 37	32Kword MAIN BLOCK 39	
	32Kword MAIN BLOCK 38	
32Kword MAIN BLOCK 36	32Kword MAIN BLOCK 37	
	32Kword MAIN BLOCK 36	

Mode)

Mode)

# Preliminary Notice: This is not a final specification.

Notice: This is not a final specification. Some parametric limits are subject to change.

# **M5M29KB/T331ATP**

33,554,432-BIT (4,194,304-WORD BY 8-BIT /2,097,152-WORD BY 16-BIT)
CMOS 3.3V-ONLY, BLOCK ERASE FLASH MEMORY

## **Bus Operation**

### BYTE#=VIH

Pins		CE#	OE#	WE#	RP#	DQ0-15
Array		VIL	VIL	VIH	VIH	Data Output
Read	Page	VIL	VIL	VIH	VIH	Data Output
Neau	Status Register	VIL	VIL	VIH	VIH	Status Register Data
	Identifier Code	VIL	VIL	VIH	VIH	Identifier Code
Output	Disable	VIL	VIH	VIH	VIH	High-Z
	Program	VIL	VIH	VIL	VIH	Command/Data in
Write	Erase	VIL	VIH	VIL	VIH	Command
	Others	VIL	VIH	VIL	VIH	Command
Stand by		VIH	X <sup>1)</sup>	X <sup>1)</sup>	VIH	High-Z
Deep Power Down		X <sup>1)</sup>	X <sup>1)</sup>	X <sup>1)</sup>	VIL	High-Z

### BYTE#=VIL

Pins		CE#	OE#	OE# WE# RP#		DQ0-7	
	Array	VIL	VIL	VIH	VIH	Data Output	
Read	Page	VIL	VIL	VIH	VIH	Data Output	
Neau	Status Register	VIL	VIL	VIH	VIH	Status Register Data	
	Identifier Code	VIL	VIL	VIH	VIH	Identifier Code	
Output	Disable	VIL	VIH	VIH	VIH	High-Z	
	Program	VIL	VIH	H VIL VIH Co		Command/Data in	
Write	Erase	VIL	VIH	VIL	VIH	Command	
	Others	VIL	VIH	VIL	VIH	Command	
Stand by		VIH	X <sup>1)</sup>	X <sup>1)</sup>	VIH	High-Z	
Deep Power Down		X <sup>1)</sup>	X <sup>1)</sup>	X <sup>1)</sup>	VIL	High-Z	

1) X can be VIH or VIL for control pins.

## **M5M29KB/T331ATP**

33,554,432-BIT (4,194,304-WORD BY 8-BIT /2,097,152-WORD BY 16-BIT)
CMOS 3.3V-ONLY, BLOCK ERASE FLASH MEMORY

# Software Command Definition Command List (WP# =VIH or VIL)

Command		1st B	us Cycle	2nd Bus Cycle					3rd-5th Bus Cycles (Word mode) 3rd-9th Bus Cycles (Byte mode)			
Command	Mode	Address	Data <sup>1)</sup>	Mode	Addres	s	Data	Mode	Address	Data		
	Wode	Address	(DQ0-15),(DQ0-7)	Wiode	A20-A18	A0	(DQ0-15),(DQ0-7)	Wiode	Address	(DQ0-15),(DQ0-7)		
Read Array	Write	Х	FFH									
Page Read	Write	Х	F3H	Read	SA <sup>5)</sup>		RD0 <sup>5)</sup>	Read	SA+i <sup>6)</sup>	RDi <sup>6)</sup>		
Device Identifier	Write	Bank <sup>2)</sup>	90H	Read	Bank <sup>2)</sup>	IA <sup>3)</sup>	ID <sup>3)</sup>					
Read Status Register	Write	Bank <sup>2)</sup>	70H	Read	Bank <sup>2</sup>	)	SRD <sup>4)</sup>					
Clear Status Register	Write	X	50H									
Suspend	Write	Bank <sup>2)</sup>	B0H									
Resume	Write	Bank <sup>2)</sup>	D0H									

- 1) In the case of Word mode(BYTE#=VIH), upper byte data (DQ15-DQ8) is ignored.
- 2) Bank=Bank address (Bank(I)-Bank(IV): A20-18)
- 3) IA=ID code address: A0=VIL (Manufacturer's code): A0=VIH (Device code), ID=ID code
- 4) SRD=Status Register Data
- 5) SA=A20-A2: Page Address, A1, A0(A1-A-1):voluntary address / RD0=1st Page read data
- 6) SA+i: Page address(is equal to 1st Page Address of A20-A2), A1,A0(A1-A-1): voluntary address / RDi: 2nd Page read data

### Command List (WP# =VIH)

Command	1st Bus Cycle			2nd Bus Cycle			3rd-129th Bus Cycles (Word mode) 3rd-257th Bus Cycles (Byte mode)		
Command	Mode	Address	Data <sup>1)</sup> (DQ0-15),(DQ0-7)	Mode	Address	Data <sup>1)</sup> (DQ0-15),(DQ0-7)	Mode	Address	Data <sup>1)</sup> (DQ0-15),(DQ0-7)
Word Program	Write	Bank <sup>2)</sup>	40H	Write	WA <sup>3)</sup>	WD <sup>3)</sup>			
Page Program	Write	Bank <sup>2)</sup>	41H	Write	WA0 <sup>4)</sup>	WD0 <sup>4)</sup>	Write	WAn <sup>4)</sup>	WDn <sup>4)</sup>
Page Buffer to Flash	Write	Bank <sup>2)</sup>	0EH	Write	WA <sup>5)</sup>	D0H <sup>1)</sup>			
Block Erase/Confirm	Write	Bank <sup>2)</sup>	20H	Write	BA <sup>6)</sup>	D0H <sup>1)</sup>			
Erase All Unlocked Blocks	Write	Х	A7H	Write	Х	D0H <sup>1)</sup>			
Clear Page Buffer	Write	Х	55H	Write	Х	D0H <sup>1)</sup>			
Single Data Load to Page Buffer	Write	Bank <sup>2)</sup>	74H	Write	WA <sup>3)</sup>	WD <sup>3)</sup>			
Flash to Page Buffer	Write	Bank <sup>2)</sup>	F1H	Write	RA <sup>7)</sup>	D0H <sup>1)</sup>			

- 1) In the case of Word mode(BYTE#=VIH), Upper byte data (DQ15-DQ8) is ignored.
- 2) Bank=Bank address (Bank(I)-Bank(IV): A20-A18)
- 3) WA=Write Address, WD=Write Data
- 4) WA0, WAn=Write Address, WD0, WDn=Write Data.

Word mode (BYTE#=VIH): Write address and write data must be provided sequentially from 00H to 7FH for A6-A0. Page size is 128 words (128-word x 16-bit), and also A20-A7 (block address, page address) must be valid.

Byte mode (BYTE#=VIL): Write address and write data must be provided sequentially from 00H to FFH for A6-A-1. Page size is 256 Bytes (256-byte x 8-bit), and also A20-A7 (block address, page address) must be valid.

- 5) WA=Write Address: A20-A7 (block address, page address) must be valid.
- 6) BA=Block Address: A20-A12[Bank(I)], A20-A15 [Bank(II), Bank(III), Bank(IV)] must be valid.
- 7) RA=Read Address: A20-A7 (block address, page address) must be valid.



Notice: This is not a final specification. Some parametric limits are subject to change.

# **M5M29KB/T331ATP**

33,554,432-BIT (4,194,304-WORD BY 8-BIT /2,097,152-WORD BY 16-BIT)
CMOS 3.3V-ONLY, BLOCK ERASE FLASH MEMORY

# Software Command Definition Command List (WP# =VIL)

Software lock release operation needs following consecutive 7bus cycles. Moreover, additional 127(255) bus cycles are needed for page program operation.

Setup Command for	1st Bus Cycle			2nd Bus Cycle			3rd Bus Cycle		
Software Lock Release	Mode	Address	Data 1)	Mode	Address	Data 1)	Mode	Address	Data 1)
Contraro 200k residuos	Wiode	riadrooo	(DQ0-15/DQ0-7)		Address	(DQ0-15/DQ0-7)	Wiode	ridarooo	(DQ0-15/DQ0-7)
Word/Byte Program	Write	Bank	60H	Write	Bank	Block <sup>6)</sup>	Write	Bank	ACH
Page Program	Write	Bank	60H	Write	Bank	Block <sup>6)</sup>	Write	Bank	ACH
Page Buffer to Flash	Write	Bank	60H	Write	Bank	Block <sup>6)</sup>	Write	Bank	ACH
Block Erase/Confirm	Write	Bank	60H	Write	Bank	Block <sup>6)</sup>	Write	Bank	ACH
Clear Page Buffer	Write	Bank	60H	Write	Bank	Block <sup>6)</sup>	Write	Bank	ACH
Single Data Load to Page Buffer	Write	Bank	60H	Write	Bank	Block <sup>6)</sup>	Write	Bank	ACH
Flash to Page Buffer	Write	Bank	60H	Write	Bank	Block <sup>6)</sup>	Write	Bank	ACH

Catura Carrana addan		4th B	us Cycle		5th Bu	s Cycle
Setup Command for Software Lock Release	Mode	Address	Data 1)	Mode	Address	Data 1)
Software Lock Release	Mode	Address	(DQ0-15/DQ0-7)	Wiode	Address	(DQ0-15/DQ0-7)
Word/Byte Program	Write	Bank	Block# <sup>6)</sup>	Write	Bank	7BH
Page Program	Write	Bank	Block# <sup>6)</sup>	Write	Bank	7BH
Page Buffer to Flash	Write	Bank	Block# <sup>6)</sup>	Write	Bank	7BH
Block Erase/Confirm	Write	Bank	Block# <sup>6)</sup>	Write	Bank	7BH
Clear Page Buffer	Write	Bank	Block# <sup>6)</sup>	Write	Bank	7BH
Single Data Load to Page Buffer	Write	Bank	Block# <sup>6)</sup>	Write	Bank	7BH
Flash to Page Buffer	Write	Bank	Block# <sup>6)</sup>	Write	Bank	7BH

Setup Command for	6th Bus Cycle			7th Bus Cycle			8th-134th Bus Cycles(Word mode) 8th-262th Bus Cycles(Byte mode)			
Program or Erase Operations	Mode	Address	Data <sup>1)</sup> (DQ0-15/DQ0-7)	Mode	Address	Data (DQ0-15/DQ0-7)	Mode	Address	Data (DQ0-15/DQ0-7)	
Word/Byte Program	Write	Bank	40H	Write	WA <sup>2)</sup>	WD <sup>2)</sup>				
Page Program	Write	Bank	41H	Write	WA0 <sup>3)</sup>	WD0 <sup>3)</sup>	Write	WAn <sup>3)</sup>	WDn <sup>3)</sup>	
Page Buffer to Flash	Write	Bank	0EH	Write	WA <sup>4)</sup>	D0H <sup>1)</sup>				
Block Erase/Confirm	Write	Bank	20H	Write	BA <sup>5)</sup>	D0H <sup>1)</sup>				
Clear Page Buffer	Write	Х	55H	Write	Х	D0H <sup>1)</sup>				
Single Data Load to Page Buffer	Write	Bank	74H	Write	WA <sup>2)</sup>	WD <sup>2)</sup>				
Flash to Page Buffer	Write	Bank	F1H	Write	RA <sup>7)</sup>	D0H <sup>1)</sup>				

- 1) In the case of word mode(BYTE#=VIH) upper byte data (DQ15-DQ8) is ignored.
- 2) WA=Write Address, WD=Write Data
- 3) WA0, WAn=Write Address, WD0, WDn=Write Data. Write address and write data must be provided sequentially from 00H to 7FH for A6-A0(word mode) and from 00H to FFH for A6-A-1(byte mode), respectively. Page size is 128 words (128-word x 16-bit/ word mode) or Page size is 256 bytes (256-word x 8-bit/ byte mode), and also A20-A7 (block address, page address) must be valid.
- 4) WA=Write Address: A20-A7 (block address, page address) must be valid.
- 5) BA=Block Address: A20-A12[Bank(I)], A20-A15 [Bank(II), Bank(III), Bank(IV)]
- 6) Block=Block Address: A20-A15, Block#=A20#-A15# must be valid.

Address	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0
Block	fixed 0	fixed 0	A20	A19	A18	A17	A16	A15
Block#	fixed 0	fixed 0	A20#	A19#	A18#	A17#	A16#	A15#

7) RA=Read Address: A20-A7 (block address, page address) must be valid.

Notice: This is not a final specification.

Some parametric limits are subject to change.

# **M5M29KB/T331ATP**

33,554,432-BIT (4,194,304-WORD BY 8-BIT /2,097,152-WORD BY 16-BIT)
CMOS 3.3V-ONLY, BLOCK ERASE FLASH MEMORY

## **Block Locking**

			Write Pr	otection Provi	ided		
RP#	WP#		Bank(I)		Bank(III)	Bank(IV)	Notes
		Boot	Parameter/Main	Main	Main	Main	
VIL	Х	Locked	Locked	Locked	Locked	Locked	Deep Power Down Mode
VIH	VIL	Locked	Locked	Locked	Locked	Locked	All Blocks Locked(Valid to operate Software Lock Release)
	VIH	Unlocked	Unlocked	Unlocked	Unlocked	Unlocked	All Blocks Unlocked

WP# pin must not be switched during performing Read / Write operations or WSM busy (WSMS=0).

### **Status Register**

Symbol	Status		Definition
(I/O Pin)		"1"	"O"
S.R. 7 (DQ7)	Write State Machine Status	Ready	Busy
S.R. 6 (DQ6)	Suspend Status	Suspended	Operation in Progress/Completed
S.R. 5 (DQ5)	Erase Status	Error	Successful
S.R. 4 (DQ4)	Program Status	Error	Successful
S.R. 3 (DQ3)	Block Status after Erase	Error	Successful
S.R. 2 (DQ2)	Reserved	-	-
S.R. 1 (DQ1)	Reserved	-	-
S.R. 0 (DQ0)	Reserved	-	-

Notice: This is not a final specification. Some parametric limits are subject to change.

# **M5M29KB/T331ATP**

33,554,432-BIT (4,194,304-WORD BY 8-BIT /2,097,152-WORD BY 16-BIT)
CMOS 3.3V-ONLY, BLOCK ERASE FLASH MEMORY

#### **Device ID Code**

Pins	AO	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	Hex. Data
Manufacturer Code	VIL	"0"	"0"	"0"	"1"	"1"	"1"	"0"	"0"	1CH
Device Code (Top Boot)	VIH	"0"	"0"	"1"	"1"	"1"	"0"	"0"	"0"	38H
Device Code (Bottom Boot)	VIH	"0"	"0"	"1"	"1"	"1"	"0"	"0"	"1"	39H

In the case of word mode, The output of upper byte data (DQ15-DQ8) is "0H".

### **Absolute Maximum Ratings**

Symbol	Parameter	Conditions	Min.	Max.	Units
VCC	VCC Voltage	With Pospert to CND	-0.2	4.6	V
VI1	All Input or Output Voltage1)	With Respect to GND		4.6	V
Ta	Ambient Temperature		-40	85	°C
Tbs	Temperature under Bias		-50	95	°C
Tstg	Storage Temperature		-65	125	°C
lout	Output Short Circuit Current			100	mA

<sup>1)</sup>Minimum DC voltage is -0.5V on input / output pins. During transitions, the level may undershoot to -2.0V for periods <20ns. Maximum DC voltage on input / output pins is VCC+0.5V which, during transitions, may overshoot to VCC+1.5V for periods <20ns.

#### **DC** electrical characteristics

(Ta= -40 ~85 °C and Flash VCC=3.0V~3.6V, unless otherwise noted)

Symbol	Parameter	Test Conditions			Limits		Units
Cymbol	i arameter	rest conditions		Min.	Typ.1)	Max.	Onits
ILI	Input Leakage Current	0V≤ VIN≤ VCC		-1.0		+1.0	μA
ILO	Output Leakage Current	0V <u>&lt;</u> VOUT <u>&lt;</u> VCC		-10		+10	μA
ISB2	VCC Stand by Current	VCC= 3.6V, VIN= GND/VCC, CE#= RF ±0.3V	P#= VCC		0.1	6	μA
ISB3		VCC= 3.6V, VIN= VIL/VIH, RP#= VIL			5	25	μA
ISB4	VCC Deep Power Down Current	VCC= 3.6V, VIN= GND or VCC, RP#= 0.3V	GND±		0.1	6	μΑ
ICC1	VCC Read Current for Word / byte	Vcc = 3.6V, VIN = VIL/VIH, RP# = OE# = WE# = VIH, CE# = VIL, lout = 0mA	5MHz		20	30	mA
1001	Voo redu current for Word, byte	VVE# = VIII, GE# = VIE, IOUL = OIIIA	1MHz		4	8	mA
ICC1P	VCC Page Read Current	Vcc = 3.6V, VIN = VIL/VIH, RP# = OE# = WE# = VIH, CE# = VIL, lout = 0mA	· · · · · · · · · · · · · · · · · · ·		5	10	mA
ICC2	VCC Write Current for Word / byte	Vcc = 3.6V, VIN = VIL/VIH, RP# = OE# = V WE# = VIL	IH, CE# =			15	mA
ICC3	VCC Program Current	VCC = 3.6V, VIN = VIL/VIH, CE#= RP#	= VIH			35	mA
ICC4	VCC Erase Current	VCC = 3.6V, VIN = VIL/VIH, CE#= RP#	= VIH			35	mA
ICC5	VCC Suspend Current	VCC = 3.6V, VIN = VIL/VIH, CE#= RP#	= VIH			200	μA
VIL	Input Low Voltage			-0.5		0.4	V
VIH	Input High Voltage		2.4		VCC+0.5	V	
VOL	Output Low Voltage	IOL = 4.0mA			0.45	V	
VOH1	Output High Voltage		0.85xVCC			V	
VOH2	Output i ligit voltage	IOH = -100uA	VCC-0.4			V	
VLKO	Low VCC Lock Out Voltage <sup>2)</sup>			1.5		2.2	V

All currents are in RMS unless otherwise noted.

<sup>2)</sup> To protect against initiation of write cycle during Flash VCC power up / down, a write cycle is locked out for Flash VCC less than VLKO. If Flash VCC is less than VLKO, Write State Machine is reset to read mode. When the Write State Machine is in Busy state, if Flash VCC is less than VLKO, the alteration of memory contents may occur.



<sup>1)</sup> Typical values at Flash VCC=3.3V, Ta=25 °C.

Notice: This is not a final specification.

Some parametric limits are subject to change.

# **M5M29KB/T331ATP**

33,554,432-BIT (4,194,304-WORD BY 8-BIT /2,097,152-WORD BY 16-BIT)
CMOS 3.3V-ONLY, BLOCK ERASE FLASH MEMORY

### **AC** electrical characteristics

(Ta=-40 ~85 °C and Flash VCC=3.0V~3.6V, unless otherwise noted)

### **Read Only Mode**

S	ymbol	Parameter	Fla	Limits	.6V	Units
	,	T draineter	Min.	Тур.	Max.	
tRC	tAVAV	Read Cycle Time	70			ns
ta(AD)	tAVQV	Address Access Time			70	ns
ta(CE)	tELQV	Chip Enable Access Time			70	ns
ta(OE)	tGLQV	Output Enable Access Time			30	ns
ta(PAD)		Page Read Access Time (after 2nd access)			25	ns
tCEPH		CE# "H"Pulse width	30			ns
tCLZ	tELQX	Chip Enable to Output in Low-Z	0			ns
tDF(CE)	tEHQZ	Chip Enable High to Output in High-Z			25	ns
tOLZ	tGLQX	Output Enable to Output in Low-Z	0			ns
tDF(OE)	tGHQZ	Output Enable to High to Output in High-Z			25	ns
tPHZ	tPLQZ	RP# Low to Output High-Z			150	ns
ta(BYTE)	tFL/HQV	BYTE# access time			70	ns
tBHZ	tFLQZ	BYTE# low to output high-Z			25	ns
tOH	tOH	Output Hold from CE#, OE# and Address	0			ns
tBCD	tELFL/H	CE# low to BYTE# high or low			5	ns
tBAD	tAVFL/H	Address to BYTE# high or low			5	ns
tOEH	tWHGL	OE# Hold from WE# High	10			ns
tPS	tPHEL	RP# Recovery to CE# Low	150			ns

<sup>-</sup>Timing measurements are made under AC waveforms for read operations.

Notice: This is not a final specification. Some parametric limits are subject to change.

## **M5M29KB/T331ATP**

33,554,432-BIT (4,194,304-WORD BY 8-BIT /2,097,152-WORD BY 16-BIT)
CMOS 3.3V-ONLY, BLOCK ERASE FLASH MEMORY

AC electrical characteristics (Ta=-40 ~85 °C and Flash VCC=3.0V~3.6V, unless otherwise noted)

Read / Write Mode (WE# control)

				Limits		
S	Symbol	Parameter	Flas	sh VCC=3.0-3	3.6V	Units
			Min.	Тур.	Max.	1
tWC	tAVAV	Write Cycle Time	70			ns
tAS	tAVWH	Address Setup Time	35			ns
tAH	tWHAX	Address Hold Time	0			ns
tDS	tDVWH	Data Setup Time	35			ns
tDH	tWHDX	Data Hold Time	0			ns
tOEH	tWHGL	OE# Hold from WE# High	10			ns
tCS	tELWL	Chip Enable Setup Time	0			ns
tCH	tWHEH	Chip Enable Hold Time	0			ns
tWP	tWLWH	Write Pulse Width	35			ns
tWPH	tWHWL	Write Pulse Width High	30			ns
tBS	tFL/HWH	Byte enable high or low set-up time	50			ns
tBH	tWFL/H	Byte enable high or low hold time	70			ns
tGHWL	tGHWL	OE# Hold to WE# Low	0			ns
tBLS	tPHHWH	Block Lock Setup to Write Enable High	70			ns
tBLH	tQVPH	Block Lock Hold from Valid SRD	0			ns
tDAP	tWHRH1	Duration of Auto Program Operation(Byte Mode)		30	300	μs
tDAP	tWHRH1	Duration of Auto Program Operation(Word Mode)		30	300	μs
tDAP	tWHRH1	Duration of Auto Program Operation(Page Mode)		4	80	ms
tDAE	tWHRH2	Duration of Auto Block Erase Operation		150	600	ms
tWHRL	tWHRL	Delay Time During Internal Operation			70	ns
tPS	tPHWL	RP# Recovery to WE# Low	150			ns

<sup>-</sup>Read timing parameters during command write operations mode are the same as during read only operation mode.

## Read / Write Mode (CE# control)

				Limits		
S	ymbol	Parameter	Fla	ash VCC=3.0-3	3.6V	Units
			Min.	Тур.	Max.	
tWC	tAVAV	Write Cycle Time	70			ns
tAS	tAVEH	Address Setup Time	35			ns
tAH	tEHAX	Address Hold Time	0			ns
tDS	tDVEH	Data Setup Time	35			ns
tDH	tEHDX	Data Hold Time	0			ns
tOEH	tEHGL	OE# Hold from CE# High	10			ns
tWS	tWLEL	Write Enable Setup Time	0			ns
tWH	tEHWH	Write Enable Hold Time	0			ns
tCEP	tELEH	CE# Pulse Width	35			ns
tCEPH	tEHEL	CE#"H" Pulse Width	30			ns
tBS	tFL/HEH	Byte enable high or low set-up time	50			ns
tBH	tEHFL/H	Byte enable high or low hold time	70			ns
tGHEL	tGHEL	OE# Hold to CE# Low	0			ns
tBLS	tPHHEH	Block Lock Setup to Chip Enable High	70			ns
tBLH	tQVPH	Block Lock Hold from Valid SRD	0			ns
tDAP	tEHRH1	Duration of Auto Program Operation(Byte Mode)		30	300	μs
tDAP	tEHRH1	Duration of Auto Program Operation(Word Mode)		30	300	μs
tDAP	tEHRH1	Duration of Auto Program Operation(Page Mode)		4	80	ms
tDAE	tEHRH2	Duration of Auto Block Erase Operation		150	600	ms
tEHRL	tEHRL	Delay Time During Internal Operation			70	ns
tPS	tPHEL	RP# Recovery to CE# Low	150			ns

<sup>-</sup>Timing measurements are made under AC waveforms for read operations.

<sup>-</sup>Typical values at Flash VCC=3.3V and Ta=25 °C.



<sup>-</sup>Typical values at Flash VCC=3.3V and Ta=25 °C.

Notice: This is not a final specification. Some parametric limits are subject to change.

# **M5M29KB/T331ATP**

33,554,432-BIT (4,194,304-WORD BY 8-BIT /2,097,152-WORD BY 16-BIT)
CMOS 3.3V-ONLY, BLOCK ERASE FLASH MEMORY

### **Program / Erase Time**

Parameter	Min.	Тур.	Max.	Units
Block Erase Time		150	600	ms
Main Block Write Time (Byte Mode)		2	8	sec
Main Block Write Time (Word Mode)		1	4	sec
Page Write Time		4	80	ms
Flash to Page Buffer Time		100	150	μs

### **Program Suspend / Erase Suspend Time**

Parameter	Min.	Тур.	Max.	Unit
Program Susupend Time			15	μs
Erase Susupend Time			15	μs

### Flash VCC Power Up / Down Timing

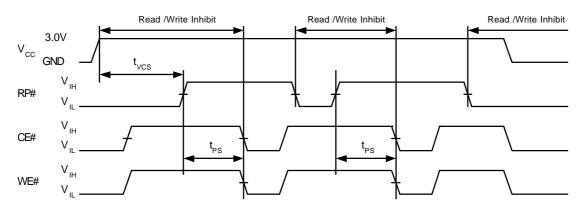
symbol	Parameter	Min.	Тур.	Max.	Unit
tVCS	RP#=VIH Setup Time from Flash VCC min.	2			μs

During power up / down, by the noise pulses on control pins, the device has possibility of accidental erase of programming. The device must be protected against initiation of write cycle for memory contents during power up / down. The delay time of min. 2 µsec is always required before read operation or write operation is initiated from the time Flash VCC reaches Flash VCC min. during power up /down. By holding RP#=VIL, the contents of memory is protected during Flash VCC power up / down. During power up, RP# must be held VIL for min. 2µs from the time Flash VCC reaches Flash VCC min.. During power down, RP# must be held VIL until Flash VCC reaches GND. RP# doesn't have latch mode, therefore RP# must be held VIH during read operation or erase / program operation.

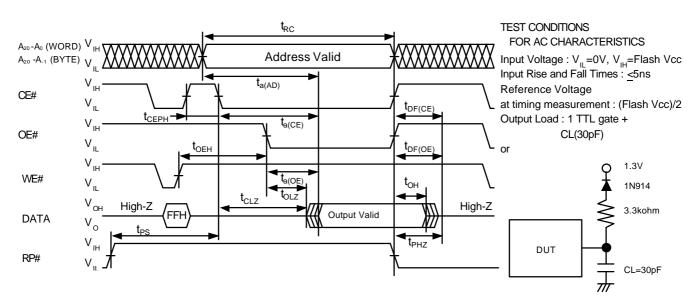
## **M5M29KB/T331ATP**

33,554,432-BIT (4,194,304-WORD BY 8-BIT /2,097,152-WORD BY 16-BIT)
CMOS 3.3V-ONLY, BLOCK ERASE FLASH MEMORY

### Flash VCC Power up / down Timing



### **AC Waveforms for Read Operation and Test Conditions**



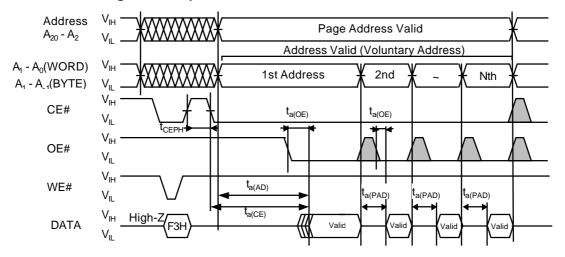
- After inputting Read Array Command FFH, it is necessary to make CE# "H" pulse more than 30ns (tCEPH).

And after inputting Read Array Command FFH, it is also necessary to keep 30ns to recover before starting read after WE# rises "H" in case of changing address(es) and CE#="L".

## **M5M29KB/T331ATP**

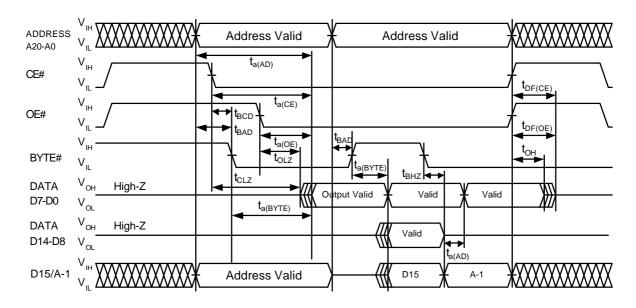
33,554,432-BIT (4,194,304-WORD BY 8-BIT /2,097,152-WORD BY 16-BIT)
CMOS 3.3V-ONLY, BLOCK ERASE FLASH MEMORY

### **AC waveforms for Page Read Operation**



- After inputting Page Read Command F3H, it is necessary to make CE# "H" pulse more than 30ns (tCEPH). And after inputting Page Read Command F3H, it is also necessary to keep 30ns to recover before starting read after WE# rises "H" in case of changing address(es) and CE#="L".
- Once Page Read mode is valid, the mode is kept until RP# is set to VIL or the chip is powered off.
- Word mode(BYTE#=VIH):N=4, Byte mode(BYTE#=VIL):N=8

### Byte AC Waveforms for Read Operation

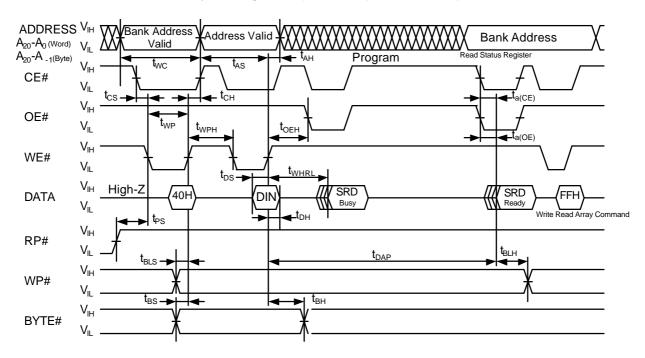


When BYTE# = VIH, CE# = OE# = VIL, D15/A-1 is output status. At this time, input signal must not be applied.

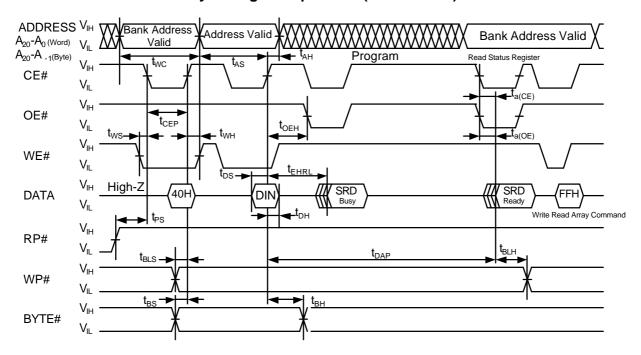
## **M5M29KB/T331ATP**

33,554,432-BIT (4,194,304-WORD BY 8-BIT /2,097,152-WORD BY 16-BIT)
CMOS 3.3V-ONLY, BLOCK ERASE FLASH MEMORY

## AC Waveforms for Word / Byte Program Operation (WE# Control)



### AC Waveforms for Word / Byte Program Operation (CE# Control)

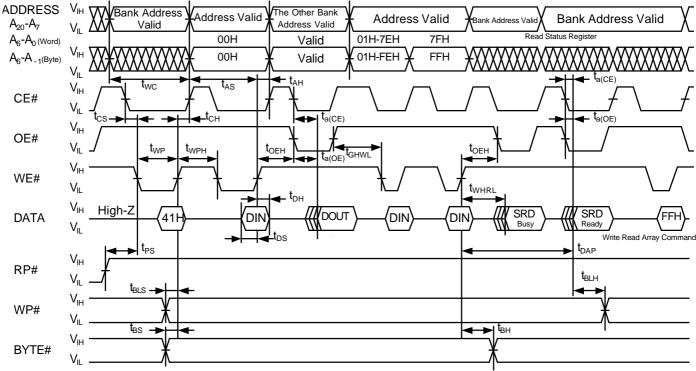


Notice: This is not a final specification. Some parametric limits are subject to change.

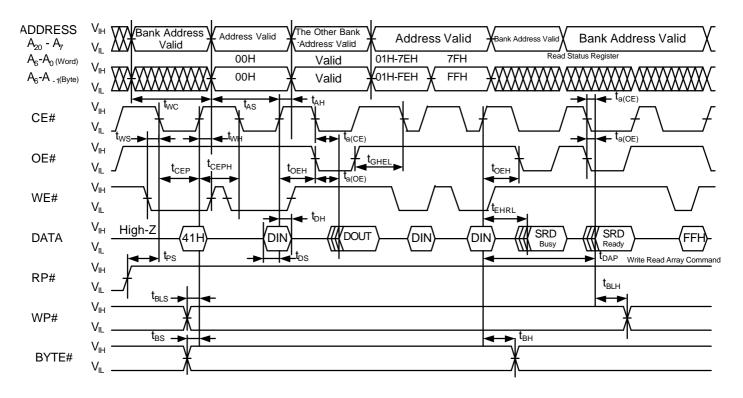
# **M5M29KB/T331ATP**

33,554,432-BIT (4,194,304-WORD BY 8-BIT /2,097,152-WORD BY 16-BIT)
CMOS 3.3V-ONLY, BLOCK ERASE FLASH MEMORY

## **AC Waveforms for Page Program Operation (WE# Control)**



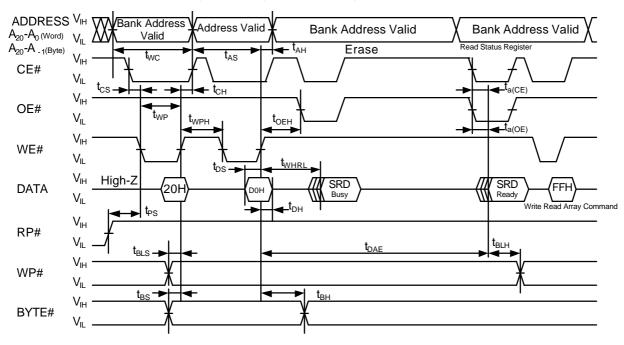
### **AC Waveforms for Page Program Operation (CE# Control)**



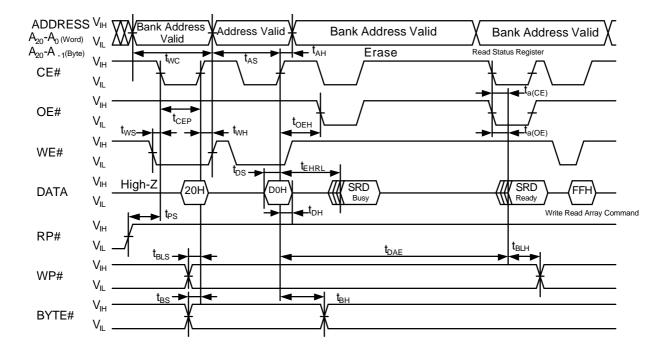
## **M5M29KB/T331ATP**

33,554,432-BIT (4,194,304-WORD BY 8-BIT /2,097,152-WORD BY 16-BIT)
CMOS 3.3V-ONLY, BLOCK ERASE FLASH MEMORY

## **AC Waveforms for Erase Operation (WE# Control)**



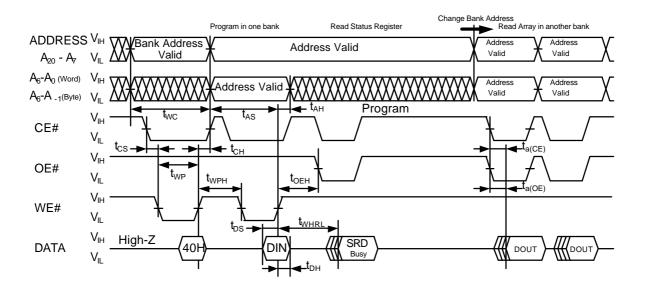
## **AC Waveforms for Erase Operation (CE# Control)**



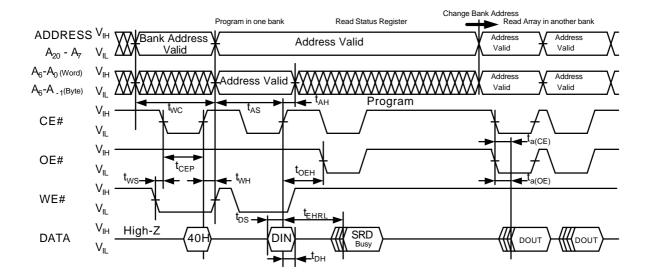
## **M5M29KB/T331ATP**

33,554,432-BIT (4,194,304-WORD BY 8-BIT /2,097,152-WORD BY 16-BIT)
CMOS 3.3V-ONLY, BLOCK ERASE FLASH MEMORY

### AC Waveforms for Word / Byte Program Operation with BGO (WE# Control)



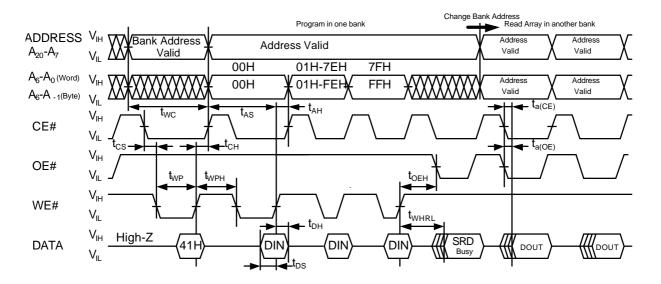
### AC Waveforms for Word / Byte Program Operation with BGO (CE# Control)



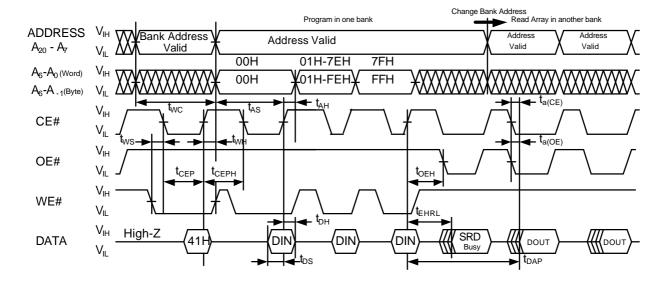
## **M5M29KB/T331ATP**

33,554,432-BIT (4,194,304-WORD BY 8-BIT /2,097,152-WORD BY 16-BIT)
CMOS 3.3V-ONLY, BLOCK ERASE FLASH MEMORY

### AC Waveforms for Page Program Operation with BGO (WE# Control)



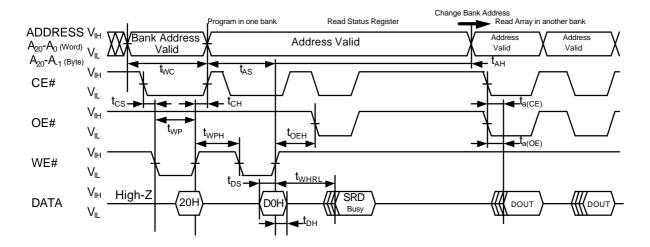
### AC Waveforms for Page Program Operation with BGO (CE# Control)



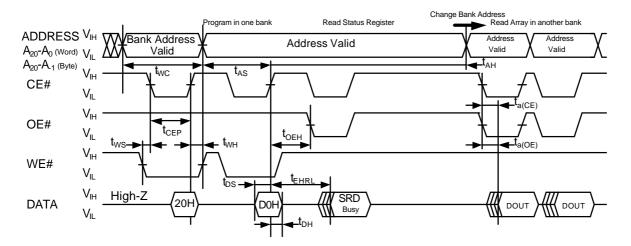
## **M5M29KB/T331ATP**

33,554,432-BIT (4,194,304-WORD BY 8-BIT /2,097,152-WORD BY 16-BIT)
CMOS 3.3V-ONLY, BLOCK ERASE FLASH MEMORY

## AC Waveforms for Erase Operation with BGO (WE# Control)



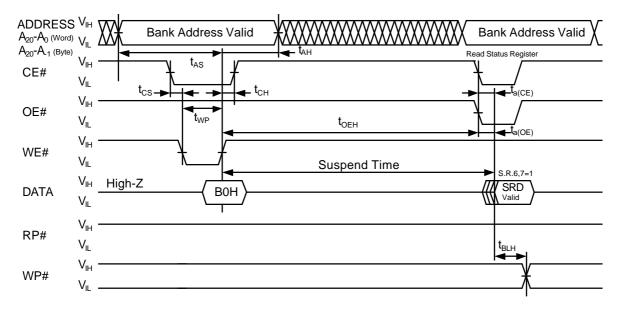
### AC Waveforms for Erase Operation with BGO (CE# Control)



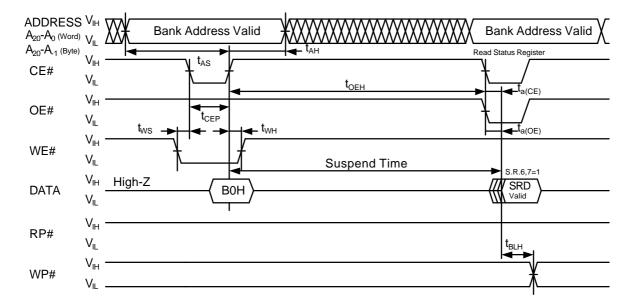
# **M5M29KB/T331ATP**

33,554,432-BIT (4,194,304-WORD BY 8-BIT /2,097,152-WORD BY 16-BIT)
CMOS 3.3V-ONLY, BLOCK ERASE FLASH MEMORY

## **AC Waveforms for Suspend Operation (WE# Control)**



### **AC Waveforms for Suspend Operation (CE# Control)**

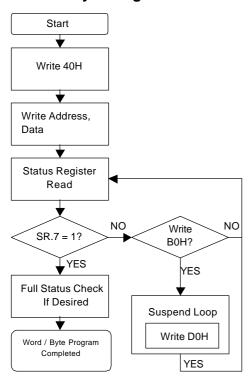


Notice: This is not a final specification. Some parametric limits are subject to change.

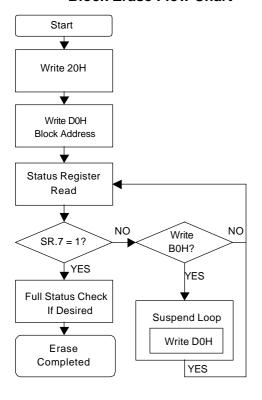
## **M5M29KB/T331ATP**

33,554,432-BIT (4,194,304-WORD BY 8-BIT /2,097,152-WORD BY 16-BIT)
CMOS 3.3V-ONLY, BLOCK ERASE FLASH MEMORY

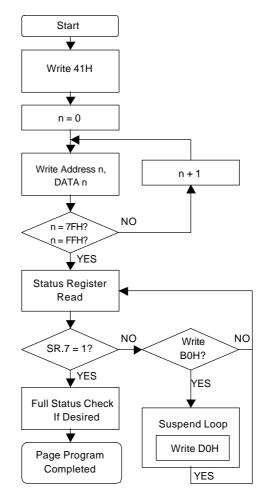
### **Word / Byte Program Flow Chart**



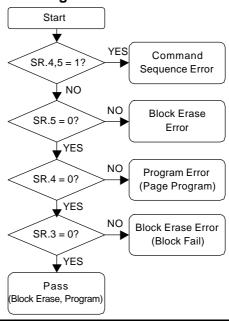
### **Block Erase Flow Chart**



## **Page Program Flow Chart**



### **Status Register Check Flow Chart**

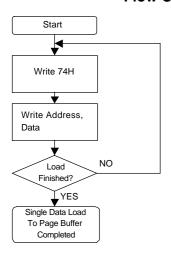


Notice: This is not a final specification. Some parametric limits are subject to change.

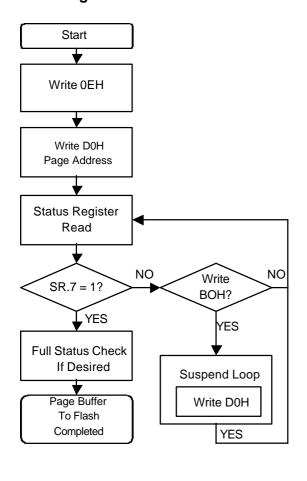
## **M5M29KB/T331ATP**

33,554,432-BIT (4,194,304-WORD BY 8-BIT /2,097,152-WORD BY 16-BIT)
CMOS 3.3V-ONLY, BLOCK ERASE FLASH MEMORY

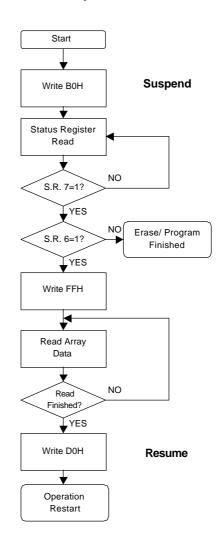
# Single Data Load to Page Buffer Flow Chart



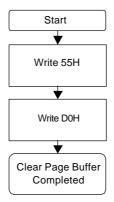
### Page Buffer to Flash Flow Chart



### Suspend / Resume Flow Chart



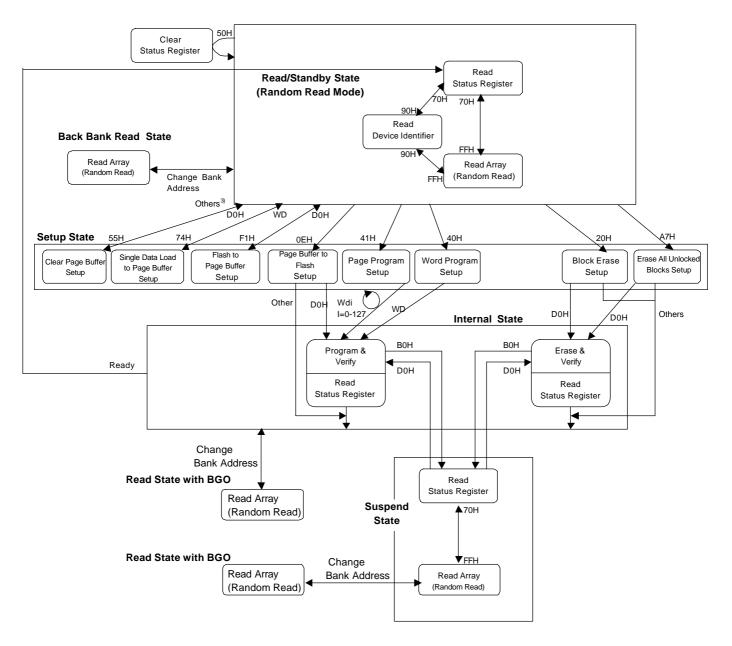
### **Clear Page Buffer Flow Chart**



## **M5M29KB/T331ATP**

33,554,432-BIT (4,194,304-WORD BY 8-BIT /2,097,152-WORD BY 16-BIT)
CMOS 3.3V-ONLY, BLOCK ERASE FLASH MEMORY

## **Operation Status (WP#=VIH)**



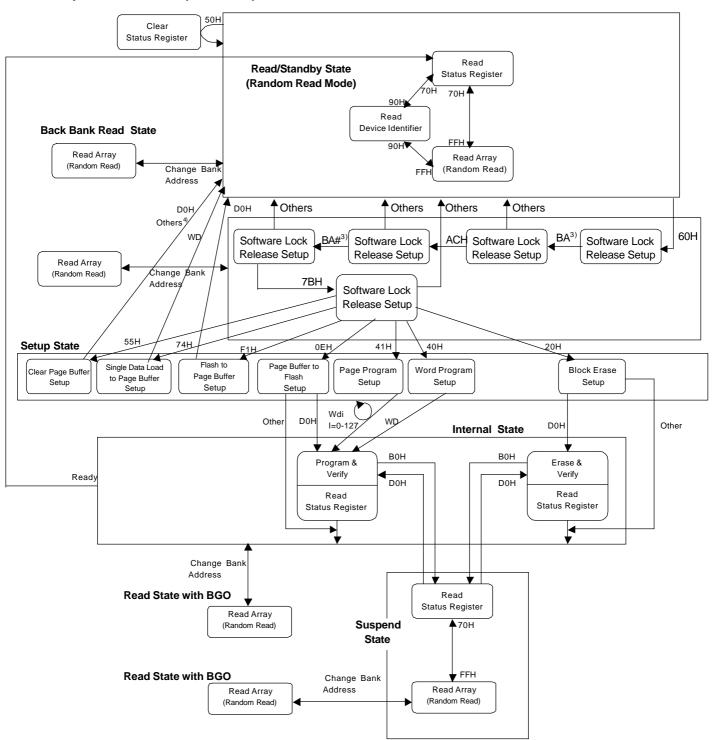
- 1) In case of Page Read, F3H is used instead of FFH in Operation Status (WP#=VIH).
- 2) Once Page Read mode is set, Page Read mode is kept until power off or RP# is set to VIL.
- 3) After setting up Clear Page Buffer, D0H enables to clear Page Buffer.
- 4) To access any bank during Erase All Unlocked Block results Status Register Read.
  Although Read Status Register Command and Read Array Command can be issued under Suspend State, output data make no sense.



## **M5M29KB/T331ATP**

33,554,432-BIT (4,194,304-WORD BY 8-BIT /2,097,152-WORD BY 16-BIT)
CMOS 3.3V-ONLY, BLOCK ERASE FLASH MEMORY

### Operation Status (WP#=VIL)



- 1) In case of Page Read, F3H is used instead of FFH in Operation Status (WP#=VIL).
- 2) Once Page Read mode is set, Page Read mode is kept until power off or RP# is set to VIL.
- 3) BA, BA#: Block Address, Block Address# (Shown in Command List(WP#=VIL) in detail).
- 4) After setting up Clear Page Buffer, D0H enables to clear Page Buffer.



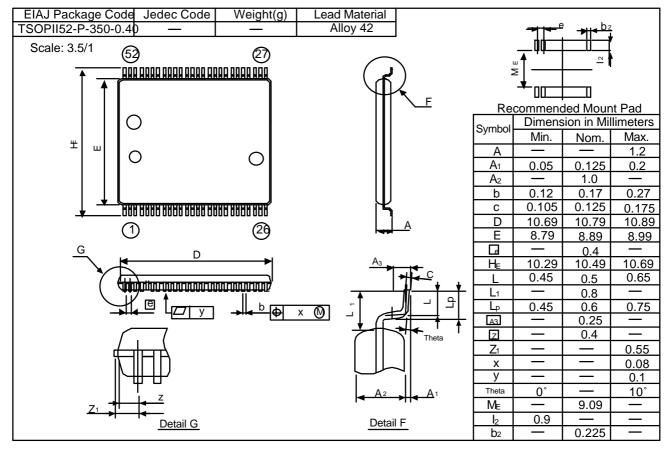
Notice: This is not a final specification. Some parametric limits are subject to change.

## **M5M29KB/T331ATP**

33,554,432-BIT (4,194,304-WORD BY 8-BIT /2,097,152-WORD BY 16-BIT)
CMOS 3.3V-ONLY, BLOCK ERASE FLASH MEMORY

### **Package Dimension**

52PTG-A



Notice: This is not a final specification. Some parametric limits are subject to change.

## M5M29KB/T331ATP

33,554,432-BIT (4,194,304-WORD BY 8-BIT /2,097,152-WORD BY 16-BIT) CMOS 3.3V-ONLY, BLOCK ERASE FLASH MEMORY

# Renesas Technology Corp.

Nippon Bldg.,6-2,Otemachi 2-chome,Chiyoda-ku,Tokyo,100-0004 Japan

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