TOSHIBA

TC203 Series CMOS ASIC Family

0.4µm, Mixed 3.3/5.0V I/O

The TC203 series is a high speed, high density 0.4µm CMOS Family of ASICs for mixed 3/5V operation.

Benefits

– True, no compromise, mixed 3/5V operation
  - Achieved by technology, not by circuit compromise
  - Inexpensive extra technology step
  - No restrictions in 3V or 5V I/O buffer placement
– True 3.3V, 0.4µm CMOS technology
  - Process optimized for 3.3V operation
  - No external components required
  - Full performance core with full 3.3V and 5V drive I/O
  - Typical loaded gate delay = 230ps
  - 690K usable gates
– Low power
  - 20% less than 0.5µm ASICs
– Advanced packaging
  - HQFP, BGA
  - High density pad option for pad limited designs
    • 62µm inner lead TAB
– New accurate delay model with commercial sign-off
– A Toshiba System ASIC product

Features

– Macrocell libray contains both normal and low power basic macrocells ie:

Cell Type	Delay	Power
Low-power type*	290ps*	2.80µW/MHz/gate
Normal type	190ps*	3.55µW/MHz/gate

* 2-input NAND, fanout=2 plus typical interconnect load

– Multilevel 5V/3V I/O buffers
– Over 450 I/O cells including high drive (upto 24mA), slew rate control, and high speed output buffers
– Compiled cells including asynchronous and synchronous RAM, single and dual port RAM and ROM
– Hard macrocells including those for PCI bus interface are available. Some fast multipliers, adders, ALUs, UARTs timers and special I/O cells are in development.
– Supports R3900 MIPS processor core

ASIC Methodologies Support

– Gate array: 14 master sizes
– Embedded array and Standard cell: 30 master sizes

Gate Array Master Lineup

Reference	Usable Gates		I/O Pads		
	Double Layer Metal	Triple Layer Metal	Wirebond Pads	TAB 62µm	TAB 83µm
TC203G02/52	11K	20K	80	152	N/A
TC203G04/54	20K	35K	104	200	N/A
TC203G06.56	29K	50K	128	248	N/A
TC203G08/58	37K	64K	144	288	N/A
TC203G10/60	44K	77K	160	316	N/A
TC203G12/62	54K	94K	176	348	N/A
TC203G14/64	64K	112K	192	380	N/A
TC203G16/66	78K	137K	208	420	N/A
TC203G20/70	95K	165K	240	-	N/A
TC203G24/74	122K	211K	272	-	N/A
TC203G32/82	171K	300K	336	-	N/A
TC203G36/86	224K	390K	384	-	N/A
TC203G40/90	284K	494K	432	-	N/A
TC203G42/92	398K	694K	512	-	N/A

Note: DLM=Double Layer Metal, TLM=Triple Layer Metal

Applications

– PC chipsets
– PC graphics
– Telecommunications
– Notebooks/PDA
– Multimedia (ie: Set Top Boxes)
– 5V migrating to 3V memory
– High gate count - therefore high power - 5V designs using 3V core for performance and power saving
– Laser printers

Accurate Models

TC203 incorporates the new Toshiba highly accurate delay model which includes the following new features:

– Pin to pin type
– State Dependent Delay
– Table Look Up Delay
– Input Slew
– Non-Linear Equation

Verilog Sign-off

TC203 is supported by Toshiba's Verilog Sign-off. This leads to the following benefits:

– Sign-off convenience at designer's site
– Shorter design cycle time
– Higher design efficiency
– Highly accurate simulation model
– Faster time-to-market

Design Kit Support

The Toshiba Design Environment provides support for a wide range of EDA tools.

DFT Support

DFT support is offered from Toshiba for full scan, partial scan, boundary scan and built-in self test (BIST).

Megacells

TC203 supports a wide rande of megacells including the 3V, 5V and Universal PCI buffers and Analog Phase Lock Loops.

Toshiba 0.4μm ASIC family

The Toshiba 0.4μ ASIC family consists of the TC200 series for pure 3V applications and the TC203 series for mixed 3/5V applications. They both use a 0.36μ drawn gate lengths and are available as Gate array, Embedded array and Standard cell (TC200G, TC200E, TC200C and TC203G, TC203E,TC203C).

Technology Resource Centers provide technical support and design expertise

Toshiba ASIC Technology Resource Centers are located throughout the U.S. and provide a high level of technical expertise for support before and during a customer ASIC design. This includes support issues dealing with EDA environments, design kits, design methodologies, packaging, technologies, and ASIC design implementation. They are also available for design consultation.

The Technology Resource Centers also provide advanced application and development engineering support. They are supported by a U.S. engineering organization based in the Toshiba Semiconductor Engineering Center in San Jose, California.

High quality, high volume manufacturing capability

Toshiba's ASIC manufacturing plants are among the largest and most advanced in the world. They are all certified to ISO9000. Rigorous production quality control and monitoring coupled with a sophisticated batch tracking system provides Toshiba with the ability to meet the requirements of fast ramping, high volume markets.

Toshiba's advanced ASIC prototype manufacturing facility located in Sunnyvale, CA offers the fastest turnaround ASIC prototypes in the industry.

MAS-3152/7-95

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