

Preliminary W24L01A



128K × 8 HIGH SPEED CMOS STATIC RAM

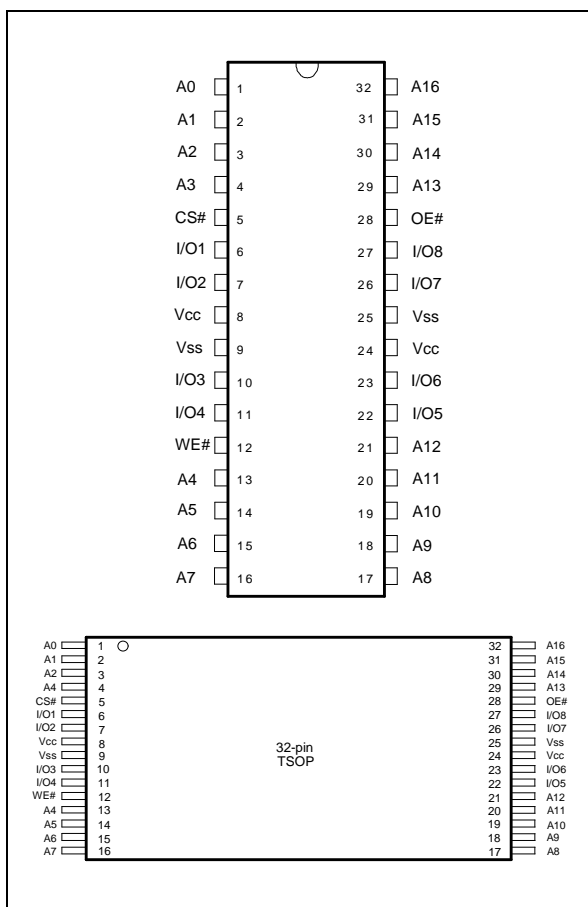
GENERAL DESCRIPTION

The W24L01A is a high speed, low power CMOS static RAM organized as 131072 x 8 bits that operates on a single 3.3-volt power supply. This device is manufactured using Winbond's high performance CMOS technology.

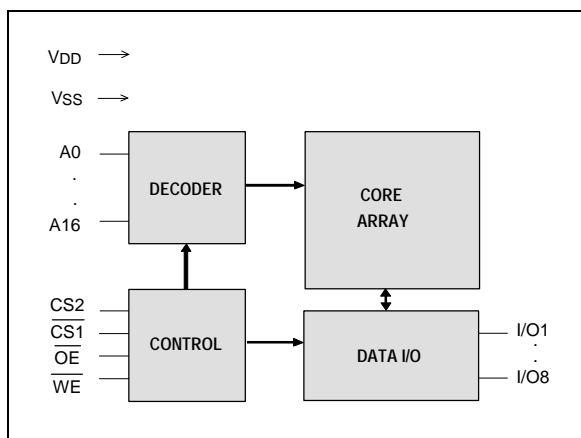
FEATURES

- High speed access time: 10/12/15 nS (max.)
- Low power consumption:
 - Active: 300 mW (typ.)
- Single +3.3V power supply
- Three-state outputs
- All inputs and outputs directly TTL/LVTTL compatible
- Available packages: 32-pin 300 mil SOJ, and TSOP
- Optional temperature range: 0 to 70° C and -20 to 85° C

PIN CONFIGURATIONS



BLOCK DIAGRAM



PIN DESCRIPTION

| SYMBOL | DESCRIPTION |
|-------------|---------------------|
| A0 – A16 | Address Inputs |
| I/O1 – I/O8 | Data Inputs/Outputs |
| CS | Chip Select Inputs |
| WE | Write Enable Input |
| OE | Output Enable Input |
| VDD | Power Supply |
| VSS | Ground |
| NC | No Connection |

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DC CHARACTERISTICS

Absolute Maximum Ratings

| PARAMETER | | RATING | UNIT |
|---------------------------------|-------------|------------------|------|
| Supply Voltage to Vss Potential | | -0.5 to +4.6 | V |
| Input/Output to Vss Potential | | -0.5 to VDD +0.5 | V |
| Allowable Power Dissipation | | 1.0 | W |
| Storage Temperature | | -65 to +150 | °C |
| Operating Temperature | W24L01AXXXX | 0 to +70 | °C |
| | W24L01AXXXE | -20 to +85 | °C |

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

TRUTH TABLE

| CS1 | CS2 | OE | WE | MODE | I/O1 - I/O8 | VDD CURRENT |
|-----|-----|----|----|----------------|-------------|-------------|
| H | X | X | X | Not Selected | High Z | ISB, ISB1 |
| X | L | X | X | Not Selected | High Z | ISB, ISB1 |
| L | H | H | H | Output Disable | High Z | IDD |
| L | H | L | H | Read | Data Out | IDD |
| L | H | X | L | Write | Data In | IDD |

OPERATING CHARACTERISTICS

(VDD = 3.3V ±5%, Vss = 0V, TA = 0 to 70° C for 10/12/15 nS: -20 to 85° C for 12/15 nS)

| PARAMETER | SYM. | TEST CONDITIONS | MIN. | TYP. | MAX. | UNIT | |
|--------------------------------|------|--|------|------|----------|------|----|
| Input Low Voltage | VIL | - | -0.5 | - | +0.8 | V | |
| Input High Voltage | VIH | - | +2.0 | - | VDD +0.5 | V | |
| Input Leakage Current | ILI | VIN = Vss to VDD | -10 | - | +10 | μA | |
| Output Leakage Current | ILO | VI/O = Vss to VDD CS1 = VIH or CS2 = VIL or OE = VIH or WE = VIL | -10 | - | +10 | μA | |
| Output Low Voltage | VOL | IOL = +8.0 mA | - | - | 0.4 | V | |
| Output High Voltage | VOH | IOH = -4.0 mA | 2.4 | - | - | V | |
| Operating Power Supply Current | IDD | CS1 = VIL, CS2 = VIH I/O = 0 mA Cycle = MIN Duty = 100% | 10 | - | - | 130 | mA |
| | | | 12 | - | - | 120 | mA |
| | | | 15 | - | - | 100 | mA |
| Standby Power Supply Current | ISB | CS1 = VIH, or CS2 = VIL | - | - | 15 | mA | |
| | ISB1 | CS1 ≥ VDD -0.2V or CS2 ≤ 0.2V | - | - | 5 | mA | |

Note: Typical characteristics are at VDD = 3.3V, TA = 25° C.

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CAPACITANCE

(V_{DD} = 3.3V, T_A = 25° C, f = 1 MHz)

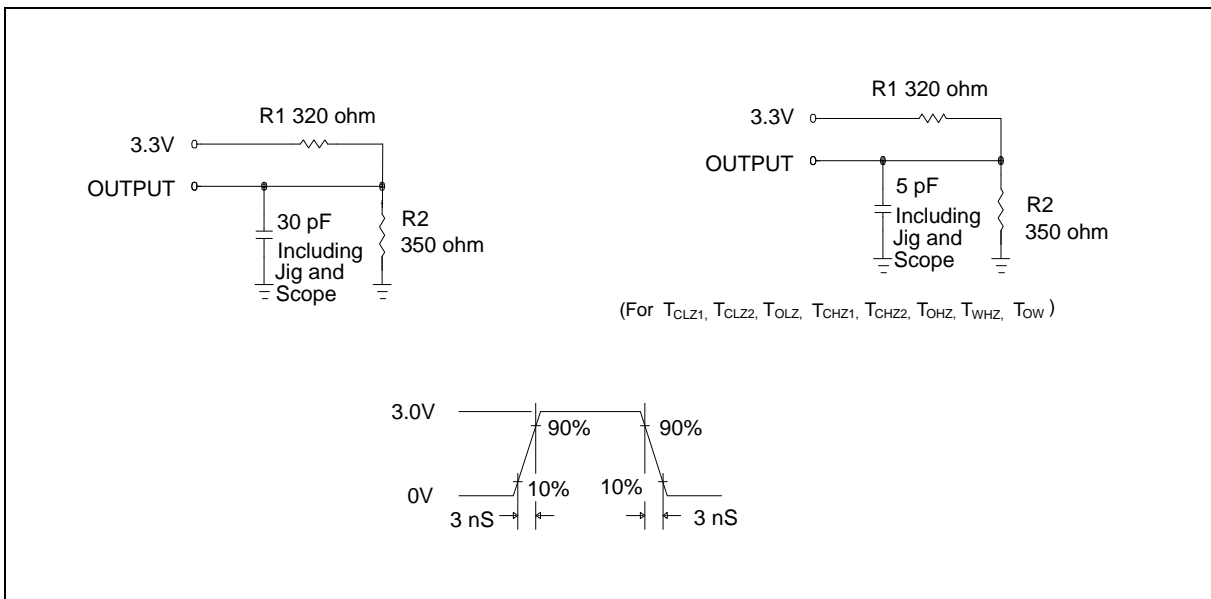
| PARAMETER | SYM. | CONDITIONS | MAX. | UNIT |
|--------------------------|------------------|-----------------------|------|------|
| Input Capacitance | C _{IN} | V _{IN} = 0V | 8 | pF |
| Input/Output Capacitance | C _{I/O} | V _{OUT} = 0V | 10 | pF |

Note: These parameters are sampled but not 100% tested.

AC TEST CONDITIONS

| PARAMETER | CONDITIONS |
|---|---|
| Input Pulse Levels | 0V to 3V |
| Input Rise and Fall Times | 3 nS |
| Input and Output Timing Reference Level | 1.5V |
| Output Load | C _L = 30 pF, I _{OH} /I _{OL} = -4 mA/8 mA |

AC TEST LOADS AND WAVEFORM



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AC CHARACTERISTICS

(V_{DD} = 3.3V ±5%, V_{SS} = 0V, T_A = 0 to 70° C for 10/12/15 nS ; -20 to 85° C for 12/15 nS)

Read Cycle

| PARAMETER | SYM. | W24L01A-10 | | W24L01A-12 | | W24L01A-15 | | UNIT |
|--------------------------------------|-------|------------|------|------------|------|------------|------|------|
| | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| Read Cycle Time | TRC | 10 | - | 12 | - | 15 | - | nS |
| Address Access Time | TAA | - | 10 | - | 12 | - | 15 | nS |
| Chip Select Access Time | TACS | - | 10 | - | 12 | - | 15 | nS |
| Output Enable to Output Valid | TAOE | - | 5 | - | 6 | - | 7 | nS |
| Chip Selection to Output in Low Z | TCLZ* | 3 | - | 3 | - | 3 | - | nS |
| Output Enable to Output in Low Z | TOLZ* | 0 | - | 0 | - | 0 | - | nS |
| Chip Deselection to Output in High Z | TCHZ* | - | 5 | - | 6 | - | 7 | nS |
| Output Disable to Output in High Z | TOHZ* | - | 5 | - | 6 | - | 7 | nS |
| Output Hold from Address Change | TOH | 3 | - | 3 | - | 3 | - | nS |

* These parameters are sampled but not 100% tested.

Write Cycle

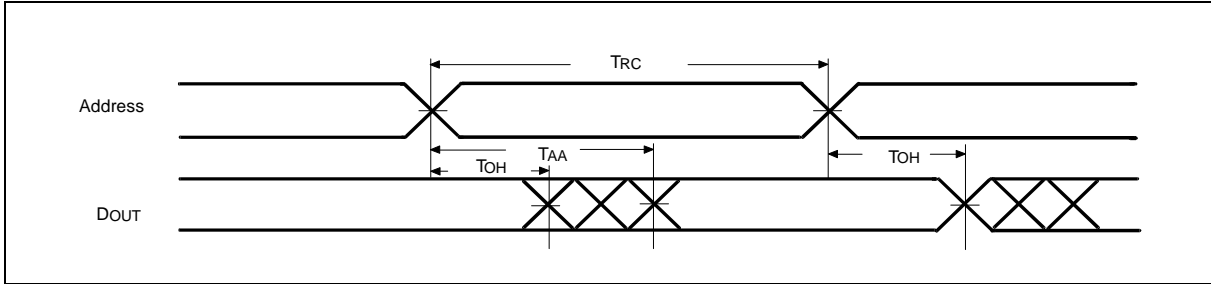
| PARAMETER | SYM. | W24L01A-10 | | W24L01A-12 | | W24L01A-15 | | UNIT |
|------------------------------------|--|------------|------|------------|------|------------|------|------|
| | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| Write Cycle Time | T _{WC} | 10 | - | 12 | - | 15 | - | nS |
| Chip Selection to End of Write | T _{CW1} | 9 | - | 10 | - | 13 | - | nS |
| Address Valid to End of Write | T _{AW} | 9 | - | 10 | - | 13 | - | nS |
| Address Setup Time | T _{AS} | 0 | - | 0 | - | 0 | - | nS |
| Write Pulse Width | T _{WP} | 9 | - | 10 | - | 10 | - | nS |
| Write Recovery Time | $\overline{\text{CS}}, \overline{\text{WE}}$ T _{WR} | 0 | - | 0 | - | 0 | - | nS |
| Data Valid to End of Write | T _{DW} | 5 | - | 7 | - | 9 | - | nS |
| Data Hold from End of Write | T _{DH} | 0 | - | 0 | - | 0 | - | nS |
| Write to Output in High Z | T _{WHZ} * | - | 5 | - | 6 | - | 8 | nS |
| Output Disable to Output in High Z | TOHZ* | - | 5 | - | 6 | - | 8 | nS |
| Output Active from End of Write | T _{OW} | 0 | - | 0 | - | 0 | - | nS |

* These parameters are sampled but not 100% tested.

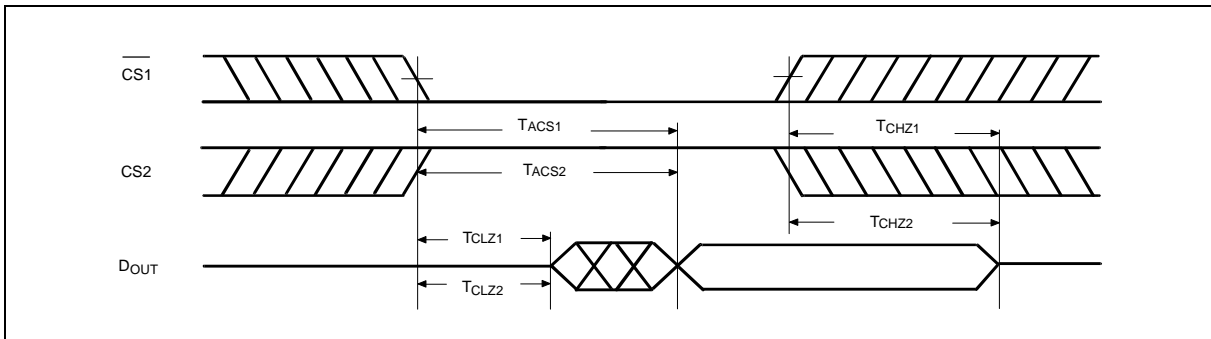


TIMING WAVEFORMS

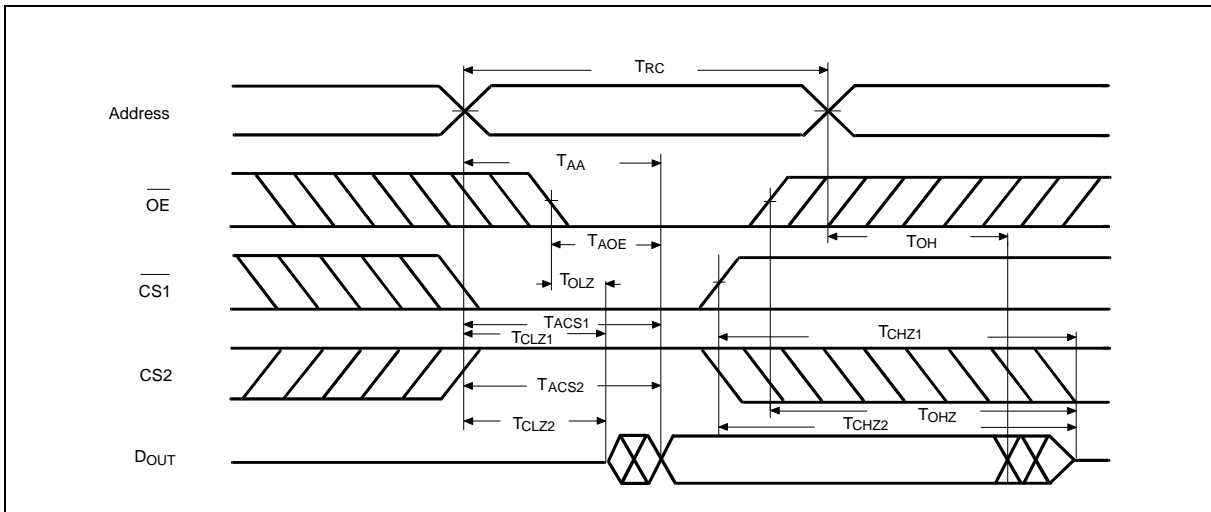
Read Cycle 1 (Address Controlled)



Read Cycle 2 (Chip Select Controlled)



Read Cycle 3 (Output Enable Controlled)

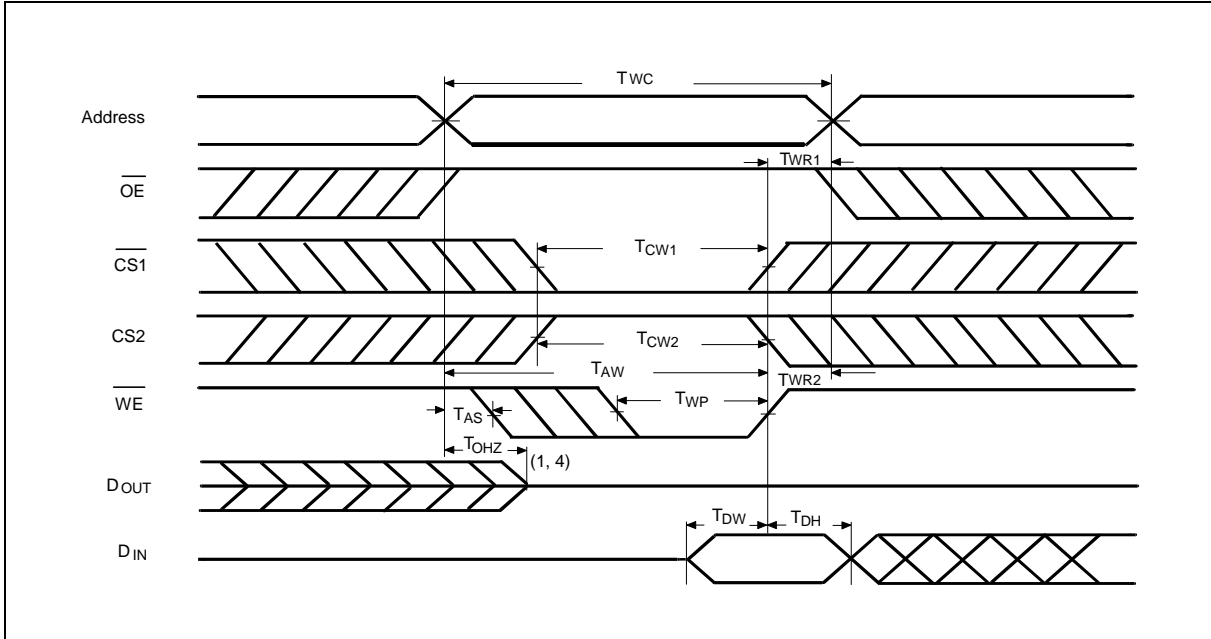


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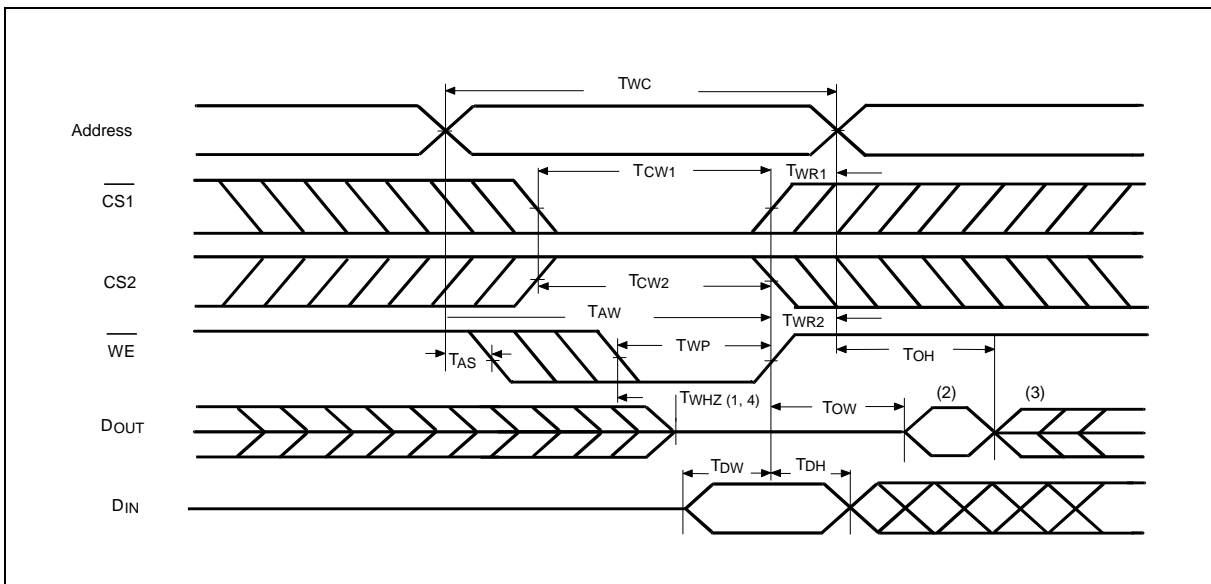


Timing Waveforms, continued

Write Cycle 1 (\overline{OE} Clock)



Write Cycle 2 ($\overline{OE} = V_{IL}$ Fixed)



Notes:

1. During this period, I/O pins are in the output state, so input signals of opposite phase to the outputs should not be applied.
2. The data output from DOUT are the same as the data written to DIN during the write cycle.
3. DOUT provides the read data for the next address.
4. Transition is measured ± 500 mV from steady state with $C_L = 5$ pF. This parameter is guaranteed but not 100% tested.

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ORDERING INFORMATION

| PART NO. | ACCESS TIME (nS) | OPERATING CURRENT Max. (mA) | STANDBY CURRENT Max. (mA) | OPERATION TEMPERATURE (°C) | PACKAGE |
|-------------|------------------|-----------------------------|---------------------------|----------------------------|-----------------------------------|
| W24L01AJ-10 | 10 | 130 | 5 | 0 to +70 | 300 mil SOJ |
| W24L01AJ-12 | 12 | 120 | 5 | 0 to +70 | 300 mil SOJ |
| W24L01AJ-15 | 15 | 100 | 5 | 0 to +70 | 300 mil SOJ |
| W24L01AQ-10 | 10 | 130 | 5 | 0 to +70 | TSOPI (8 x 13.4 mm ²) |
| W24L01AQ-12 | 12 | 120 | 5 | 0 to +70 | TSOPI (8 x 13.4 mm ²) |
| W24L01AQ-15 | 15 | 100 | 5 | 0 to +70 | TSOPI(8 x 13.4 mm ²) |
| W24L01AT-10 | 10 | 130 | 5 | 0 to +70 | TSOPI (8 x 20 mm ²) |
| W24L01AT-12 | 12 | 120 | 5 | 0 to +70 | TSOPI (8 x 20 mm ²) |
| W24L01AT-15 | 15 | 100 | 5 | 0 to +70 | TSOPI (8 x 20 mm ²) |
| W24L01AJ12E | 12 | 120 | 5 | -20 to +85 | 300 mil SOJ |
| W24L01AJ15E | 15 | 100 | 5 | -20 to +85 | 300 mil SOJ |
| W24L01AQ12E | 12 | 120 | 5 | -20 to +85 | TSOPI (8 x 13.4 mm ²) |
| W24L01AQ15E | 15 | 100 | 5 | -20 to +85 | TSOPI (8 x 13.4 mm ²) |
| W24L01AT12E | 12 | 120 | 5 | -20 to +85 | TSOPI (8 x 20 mm ²) |
| W24L01AT15E | 15 | 100 | 5 | -20 to +85 | TSOPI (8 x 20 mm ²) |

Notes:

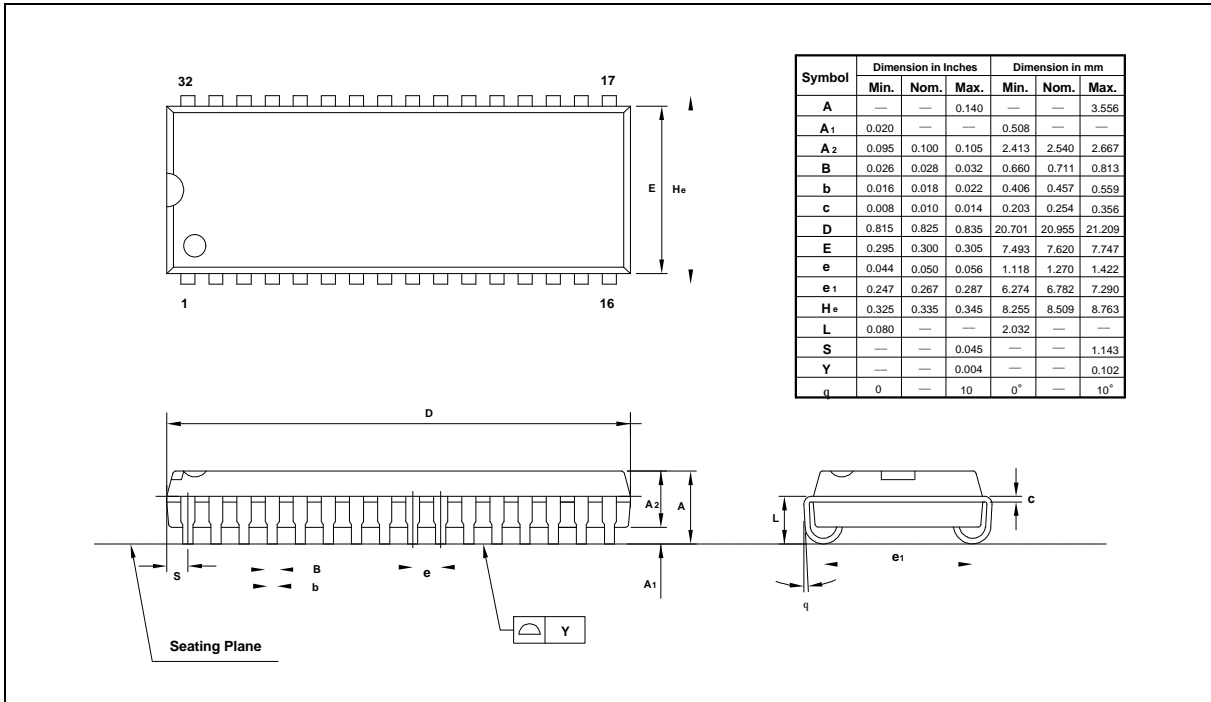
1. Winbond reserves the right to make changes to its products without prior notice.
2. Purchasers are responsible for performing appropriate quality assurance testing on products intended for use in applications where personal injury might occur as a consequence of product failure.

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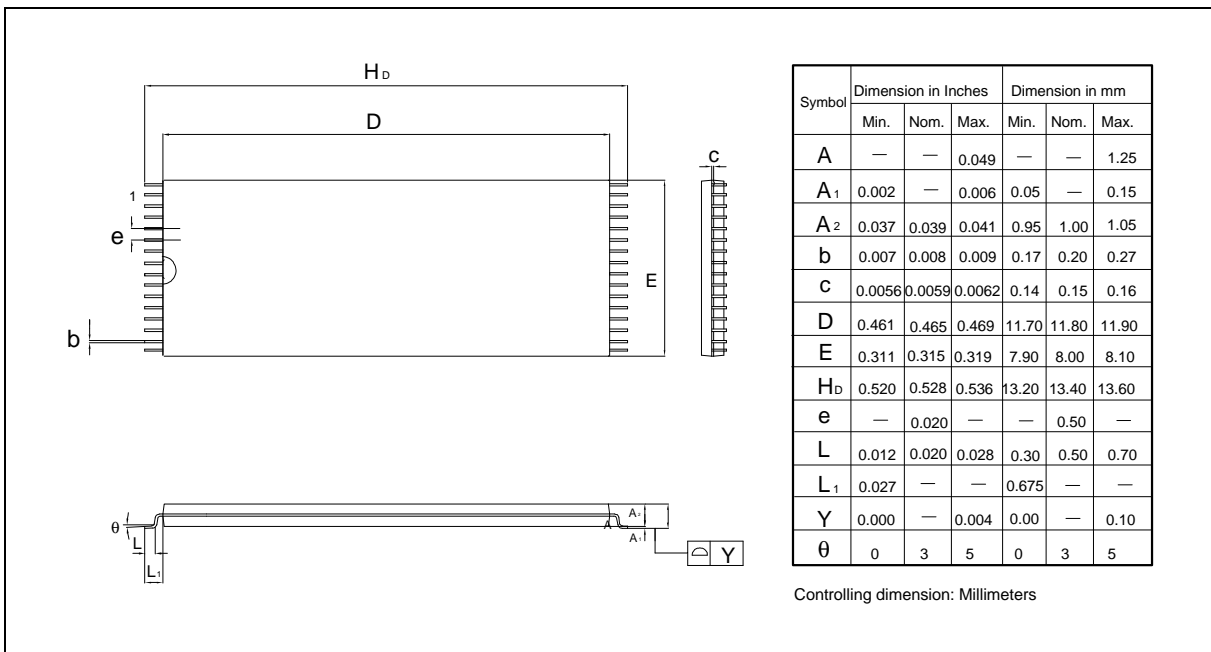


PACKAGE DIMENSIONS

32-pin SOJ

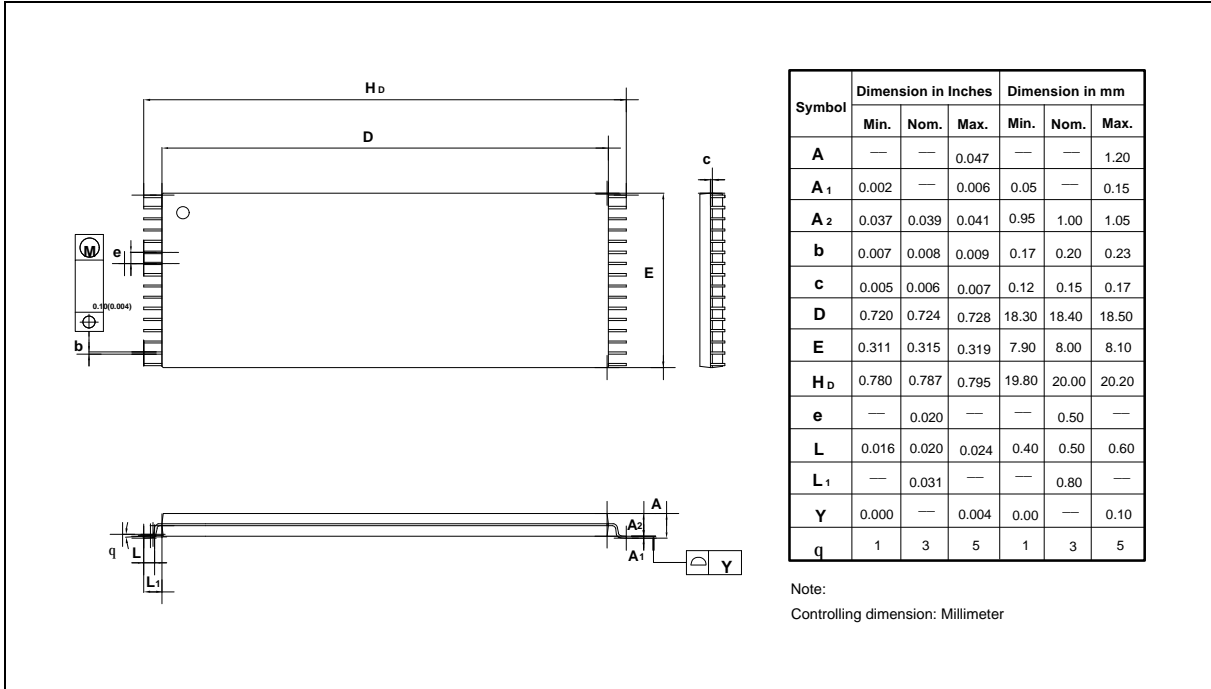


32-Lead Small Type One TSOP (8 x 13.4)



Package Dimensions, continued

32-pin TSOP



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VERSION HISTORY

| VERSION | DATE | PAGE | DESCRIPTION |
|---------|---------------|------|----------------|
| A1 | Apr. 26, 2002 | - | Initial Issued |



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