No.2238A

LC7940A, 7941A

CMOS LSI

Dot Matrix LCD Drivers

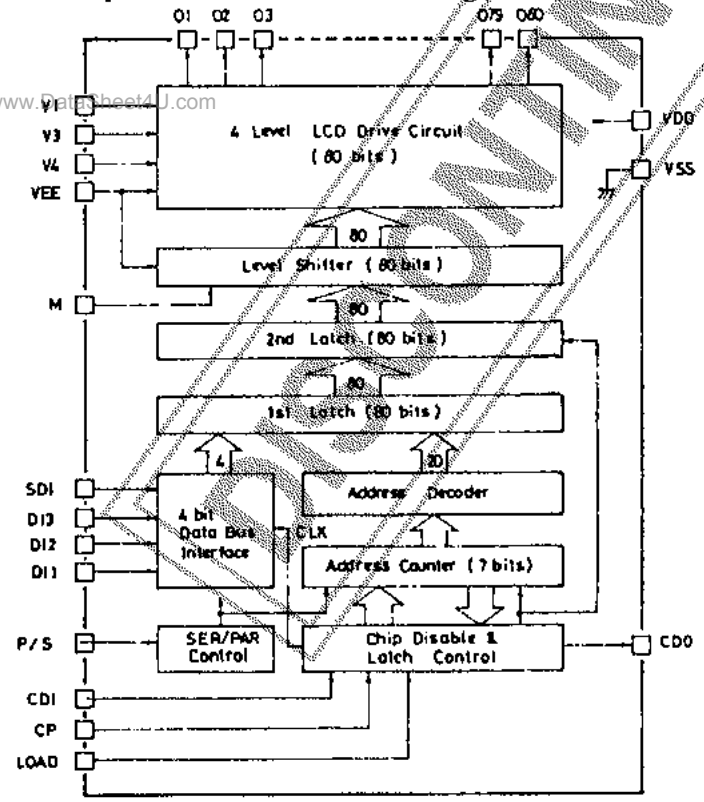
Overview

The LC7940A, 7941A are large-scale dot matrix LCD segment driver LSIs. The LC7940A, 7941A latch display data of 80 bits transferred (serial or 4-bit parallel) from a controller and generate LCD drive signals. The LC7941A is a mirror image pin assignment version of the LC7940A. The LC7940A and LC7941A can be used together to provide high-density packaging. The LC7940A and LC7941A can be used in conjunction with common driver LC7942A (QIP80) to drive a wide-screen LCD panel.

Features

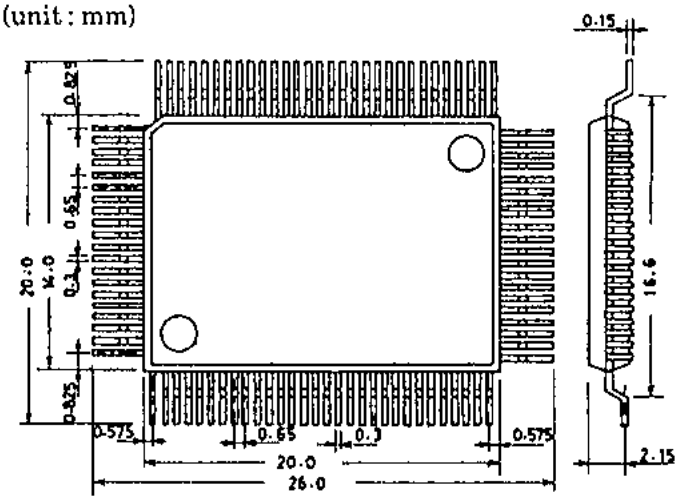
- On-chip LCD drive circuit (80 bits)
- Display duty : 1/8 to 1/128
- Display data may be input in serial or 4-bit parallel (pin-selectable).
- The chip disable pin can be used to reduce the power dissipation of the wide-screen LCD panel.
- Possible to apply the bias voltage externally.
- Operating voltage/operating temperature
  - V_{DD} (logic section) : 5V ± 10%/ − 20 to + 85°C
  - $V_{DD} - V_{EE}$ (LCD section) : V_{DD} to 20V/ − 20 to + 85°C
- Data transfer clock : 3.3MHz max.
- CMOS process
- 100-pin flat plastic package

Equivalent Circuit Block Diagram



Case Outline 3089-Q100ALSI

(unit : mm)



SANYO: QIP100A

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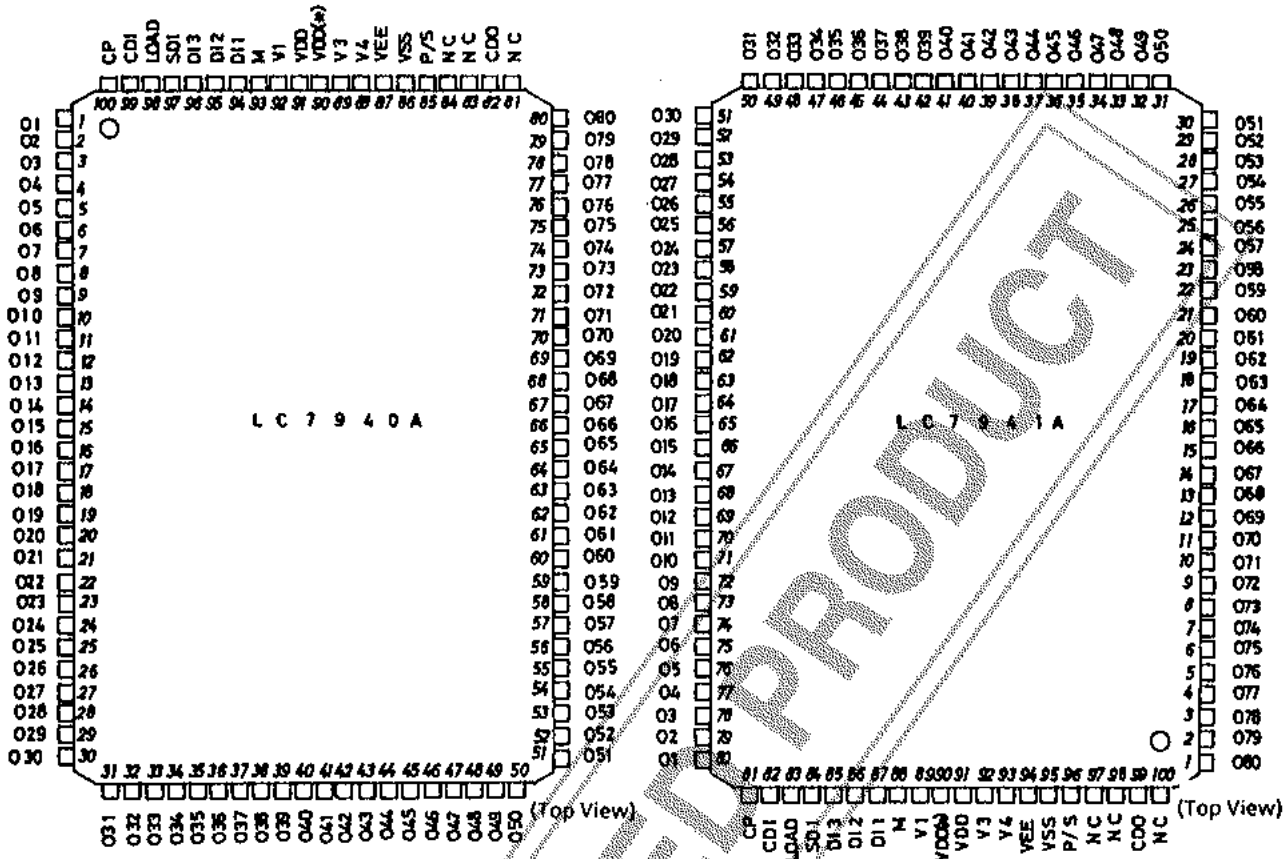
Pin Assignment



Pin Description

Pin Number		Pin Name	Input/ Output	Function
LC7940A	LC7941A			
91 90 86 87	91 90 95 94	V_{DD} V_{DD}* V_{SS} V_{EE}	Power supply	V_{DD} to V_{SS} Power supply for logic section V_{DD} to V_{EE} Power supply for LCD section V_{DD}* : V_{DD} or open
92 89 88	89 92 93	V1 V3 V4	Power supply	Power supply for LCD drive level V1, V_{EE} : Select level V3, V4 : Nonselect level
100	81	CP	Input	Display data shift clock (triggering on the trailing edge)
99	82	CDI	Input	Chip disable input "H" level : Data is not fetched. "L" level : Data is fetched.
98	83	LOAD	Input	Display data latch clock (triggering on the trailing edge) LCD drive signals of display data are output on the trailing edge.
97	84	SDI	Input	Serial data input
96 95 94	85 86 87	DI3 DI2 DI1	Input	4-bit parallel data input pin Data input: SDI, DI3, DI2, DI1 LCD drive output pin: 04 08 → 080; 03 07 → 079; 02 06 → 078; 01 05 → 077 *For serial data input, DI1 to DI3 must be fixed at "H" or "L" level.
93	88	M	Input	Signal to cause LCD drive output to alternate

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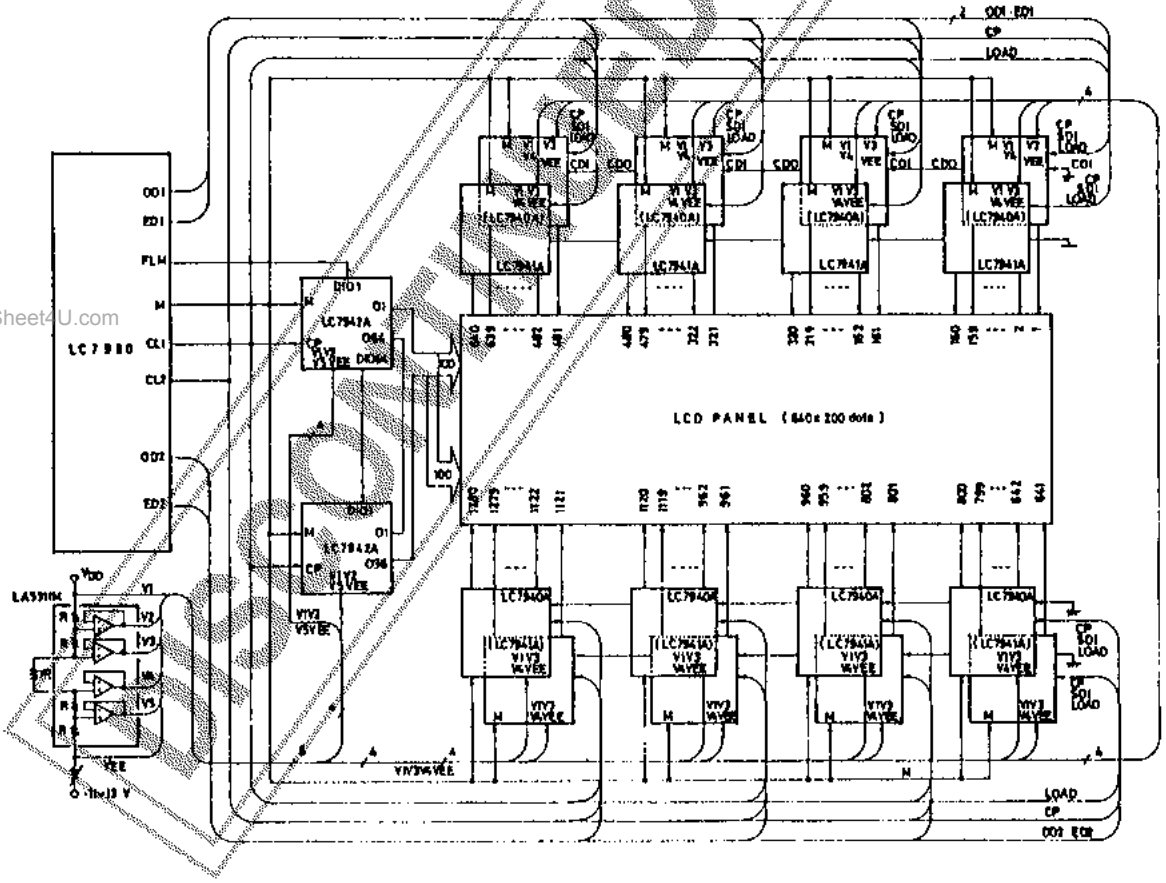
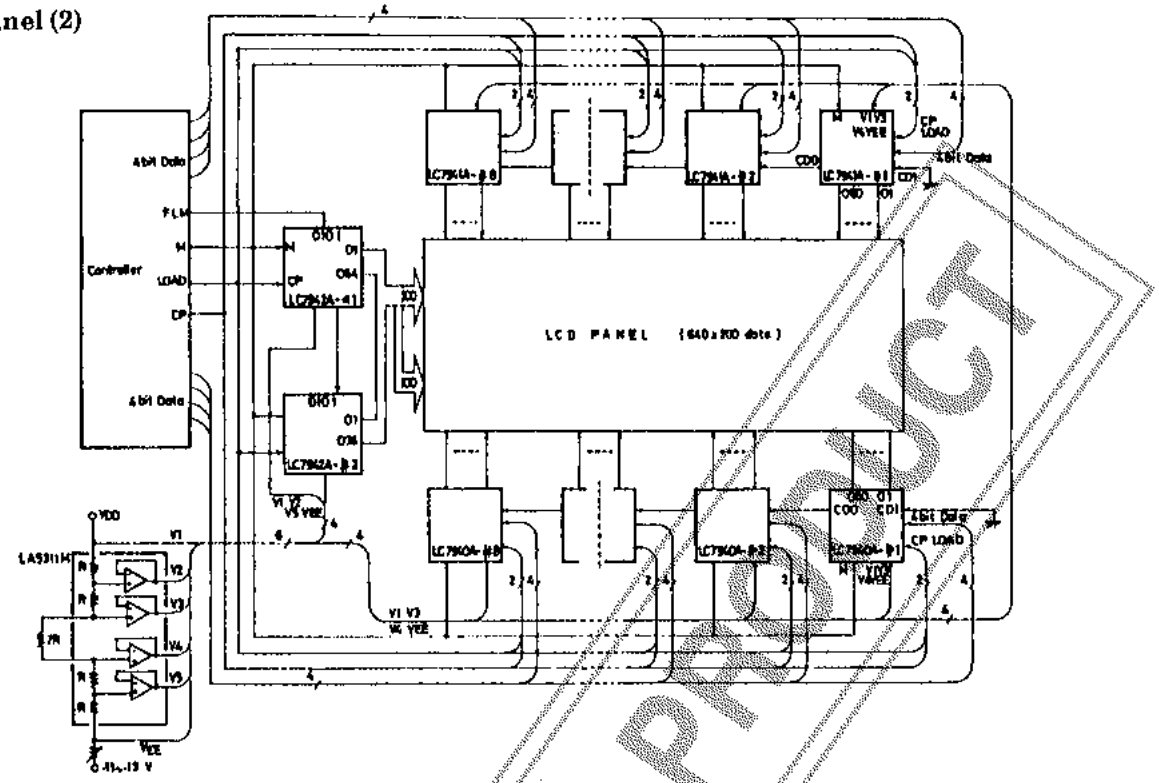
Pin Number		Pin Name	Input/ Output	Function
LC7940A	LC7941A			
85	96	P/S	Input	Data input method selecting pin "H" level : 4-bit parallel input "L" Level : Serial input
82	99	CDO	Output	Used when the LC7940A, 7941A are cascade-connected to increase the number of segments During fetching of data : "H" level Completion of fetching of 80-bit data : "L" level *Connect to the CDI pin of the LC7940A, 7941A at the next stage.
1 2 ↓ 80	80 79 ↓ 1	01 02 ↓ 080	Output	LCD drive output The combination of display data and M signal provides the following output levels. Data \ M: "H" → V_{EE} / V1; "L" → V4 / V3

LCD Panel (1)



LCD Panel (2)



Sample Application Circuit : Operation of LC7940A, 7941A, 7942A and notes

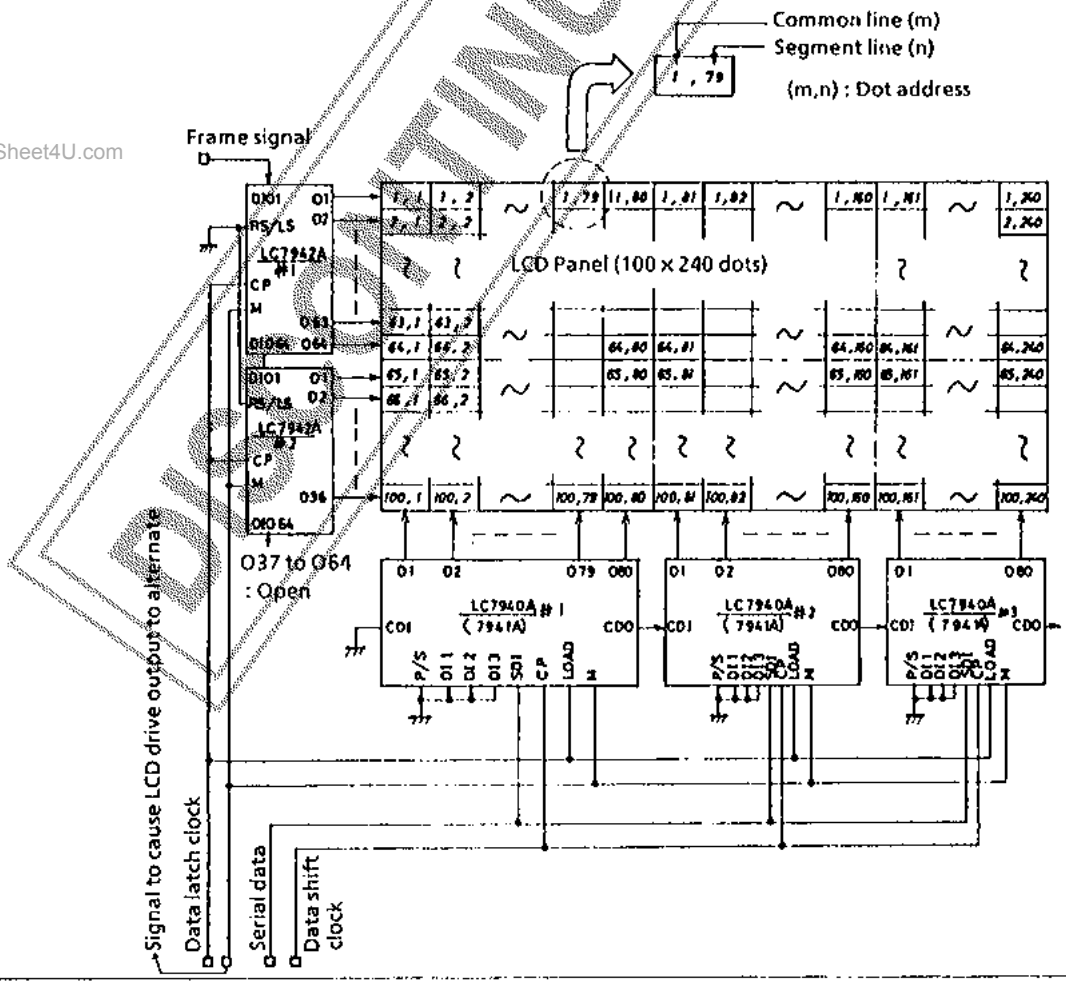
Operation of LC7940A, 7941A, 7942A

100×240-dot LCD panel

LC7940A (or LC7941A) ..... 3pcs.

LC7942A ..... 2pcs.

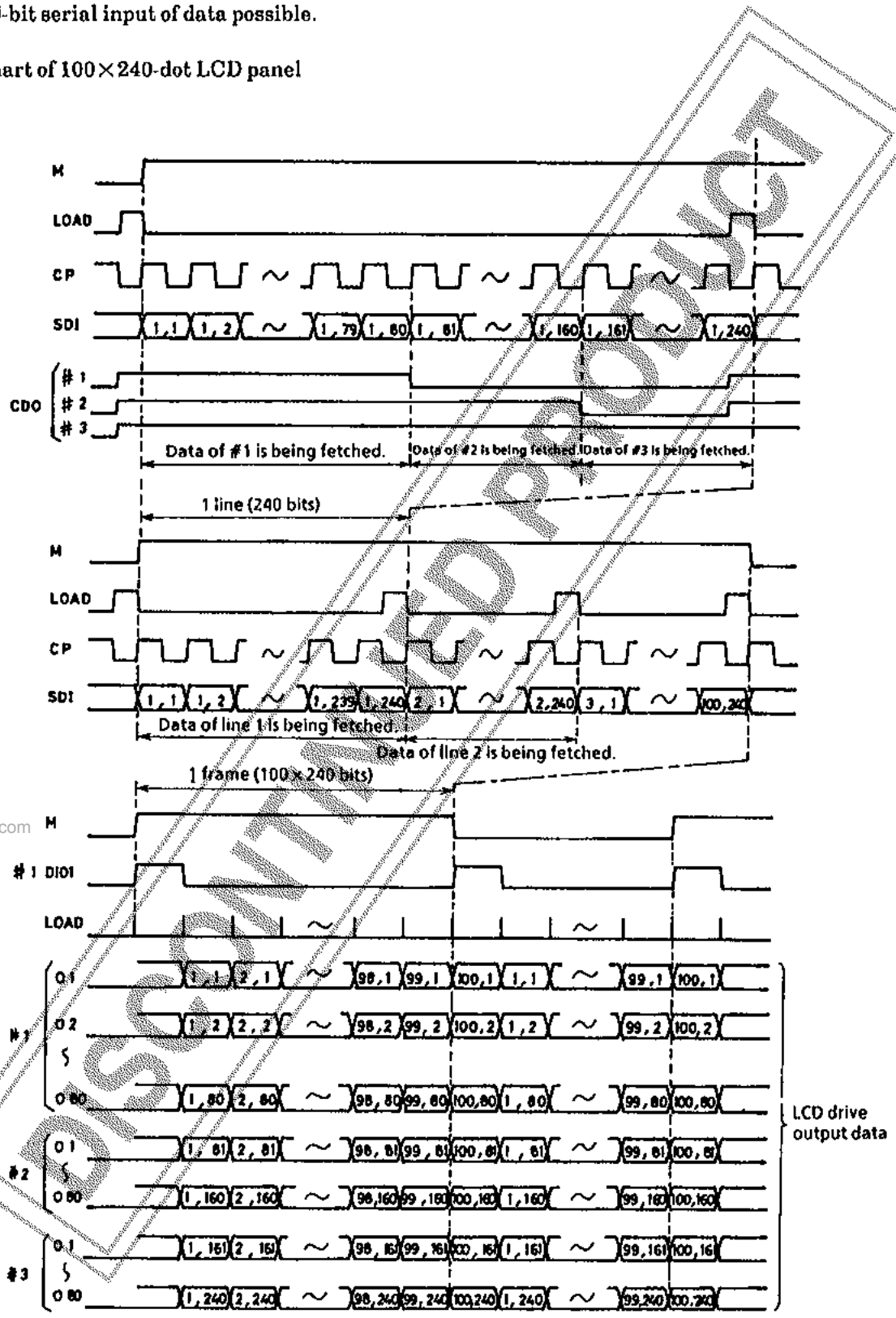
This configuration provides the following sample application of dynamic drive with 1/100 duty.



(1) Two LC7942As cascade-connected (connecting DIO64 of #1 to DIO1 of #2) are used as 100-dot shift register. O37 to O64 of #2 are not used.

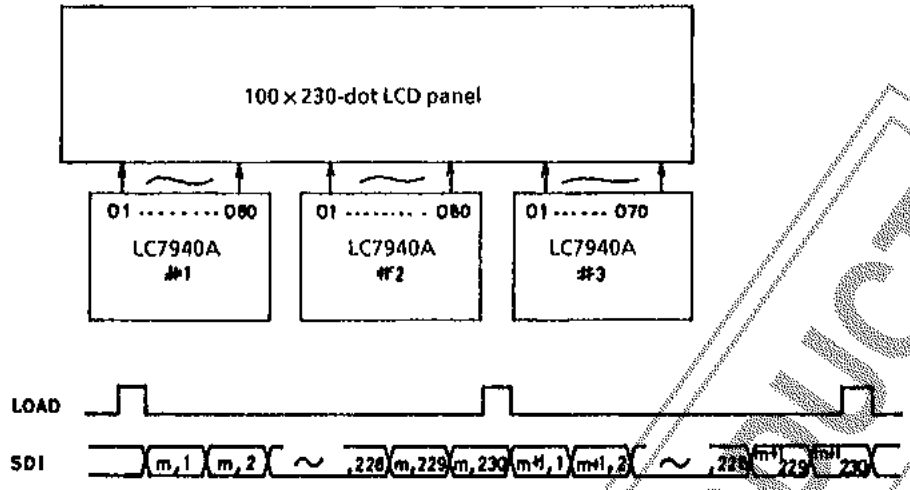
(2) Three LC7940As (or LC7941As) are cascade-connected (connecting CDO of #1 to CDI of #2, and CDO of #2 to #3). CDI of #1 is connected to GND. CDO of #3 is not used. This connection makes 240-bit serial input of data possible.

Timing chart of 100×240-dot LCD panel

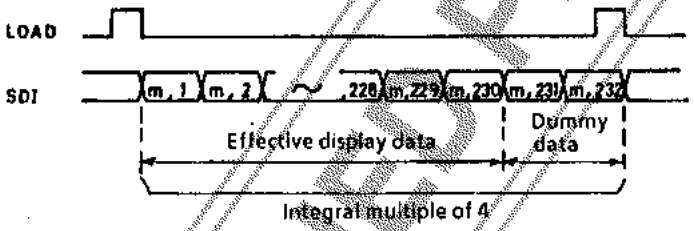


Notes to be observed when the number of lateral dots (segment data) is not an integral multiple of 4

Example



If data is sent in this timing, data of (m,229) (m,230) (m+1,229) (m+1,230) · · · · · does not appear on the outputs (O69, O70 of #3). This is because the LC7940A (LC7941A also) performs serial-parallel conversion in units of 4 bits to reduce power dissipation. Therefore, if the number of lateral dots is not an integral multiple of 4, the following processing must be performed.



This processing causes data of (m,231) to be output at O71 of #3 and data of (m,232) at O72 of #3. However, since no connection is made to the panel, data is invalid.

Absolute Maximum Ratings at Ta = 25±2°C, V_{SS} = 0V

			unit
Maximum Supply Voltage (LOGIC)	V_{DD} max	−0.3 to +7.0	V
Maximum Supply Voltage (LCD)	$V_{DD}-V_{EE}$ max	0 to 22	V
Maximum Input Voltage	V_I max	−0.3 to V_{DD}+0.3	V
Operating Temperature	Topg	−20 to +85	°C
Storage Temperature	Tstg	−40 to +125	°C

Note : With $V_{DD} \geqq V1 > V3 > V4 > V_{EE}$ held

When mounting the QIP package on the board, do not dip it in solder.

Allowable Operating Conditions at Ta = −20 to +85°C, V_{SS} = 0V

		min	typ	max	unit
Supply Voltage (LOGIC)	V_{DD}	4.5		5.5	V
Supply Voltage (LCD)	$V_{DD}-V_{EE}$	V_{DD}		20	V
Input 'H'-Level Voltage	V_{IH}	0.8V_{DD}			V
Input 'L'-Level Voltage	V_{IL}			0.2V_{DD}	V

Electrical Characteristics at Ta = 25±2°C, V_{SS} = 0V, V_{DD} = 5V±0%

			min	typ	max	unit
Input 'H'-Level Current	I_{IH}	$V_{IN}=V_{DD}$: LOAD,CP,CDI,P/S, DI1,DI2,DI3,SDI,M			1	μA
Input 'L'-Level Current	I_{IL}	$V_{IN}=V_{SS}$: LOAD,CP,CDI,P/S, DI1,DI2,DI3,SDI,M	−1			μA
Output 'H'-Level Voltage	V_{OH}	I_{OH} = −400μA (CDO)	V_{DD}−0.4			V
Output 'L'-Level Voltage	V_{OL}	I_{OL} = 400μA (CDO)			0.4	V
Driver ON-State Resistance	R_{ON}	$V_{DD}-V_{EE}$ = 18V, $\lvert V_{DE}-V_O\rvert$ = 0.25V (Note 1) (01 to 80)		2	4	kΩ

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			min	typ	max	unit
Standby Current	I_{ST}	CDI = V_{DD}, $V_{DD} - V_{EE}$ = 18V, CP = 3.3MHz, no-load output			200	μA
Operating Current	I_{SS} (Note 2)	$V_{DD} - V_{EE}$ = 18V, CP = 3.3MHz, LOAD = 5.156kHz, M = 52Hz			1.0	mA
	I_{EE} (Note 3)				0.1	mA
Input Capacitance	C_I	f = 3.3MHz		5		pF
CP (Shift Clock)	f_{CP}				3.3	MHz
CP Pulse Width	t_{WC}		100			ns
LOAD Pulse Width	t_{WL}		100			ns
Setup Time	t_{SETUP}		80			ns
Hold Time	t_{HOLD}		80			ns
CP→LOAD	t_{CL} (1)		0			ns
	t_{CL} (2)		100			ns
LOAD→CP	t_{LC}		100			ns
Rise/Fall Time	t_R				50	ns
	t_F				50	ns
	t_{RL}				50	ns
	t_{FL}				50	ns

(Note 1) : $V_{DE} = V_{DD}$ to V_{EE}, $V1 = V_{DD}$, $V3 = 9/11\,(V_{DD} - V_{EE})$, $V4 = 2/11\,(V_{DD} - V_{EE})$
(Note 2) : I_{SS} flows from V_{DD} to V_{SS}.
(Note 3) : I_{EE} flows from V_{DD} to V_{EE}.

Switching Characteristics			min	typ	max	unit
Output Delay Time	t_D	Load = 30pF			200	ns

Switching Characteristic