AOZ1253

3A EZBuck™ Synchronous Buck Regulator

General Description

The AOZ1253 is a high efficiency, low quiescent current and simple to use 3A synchronous buck regulator. This device operates from 4.5V to 26V input voltage range and provides up to 3A of continuous output current with an adjustable output voltage down to 0.6V.

The AOZ1253 is offered in the Exposed Pad SO-8 package which is rated over a -40°C to +85°C ambient temperature range.

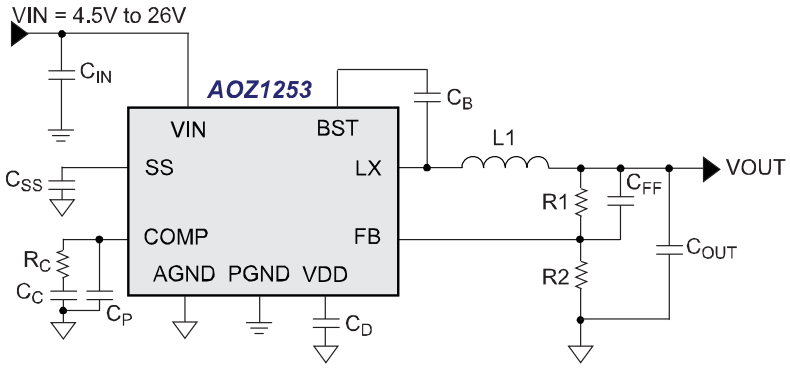
Features

- 4.5V to 26V input voltage operation range
- High efficiency PFM mode light load performance
- Synchronous rectification: 115mΩ integrated high-side switch and 30mΩ internal low-side switch
- Integrated bootstrap diode
- External soft start control
- Adjustable output voltage down to 0.6V
- 3A continuous output current
- Fixed frequency of PWM 620kHz operation
- Tailored for small profile inductor and ceramic capacitors
- Cycle-by-cycle current limit
- Short-circuit protection
- Thermal shutdown
- Standard exposed pad SO-8 package
- -40°C to 150°C operating junction temperature range

Applications

- High performance point-of-load DC/DC converters
- Notebook/ultra mobile PCs/servers
- PCIe graphics cards/set top boxes
- Set top boxes
- DVD drives and HDD
- LCD-TV/displays

Typical Application



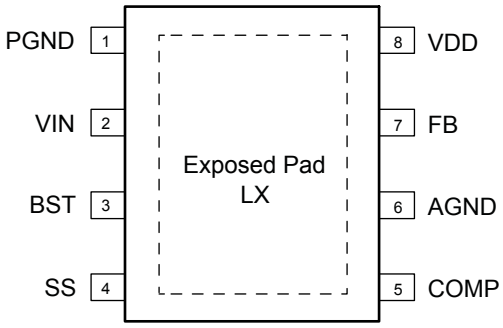
Green

Ordering Information

Part Number	Temperature Range	Package	Environmental
AOZ1253PI	-40°C to +85°C	EPAD SO-8	Green

AOS Green Products use reduced levels of Halogens, and are also RoHS compliant.
Please visit www.aosmd.com/web/quality/rohs_compliant.jsp for additional information.

Pin Configuration

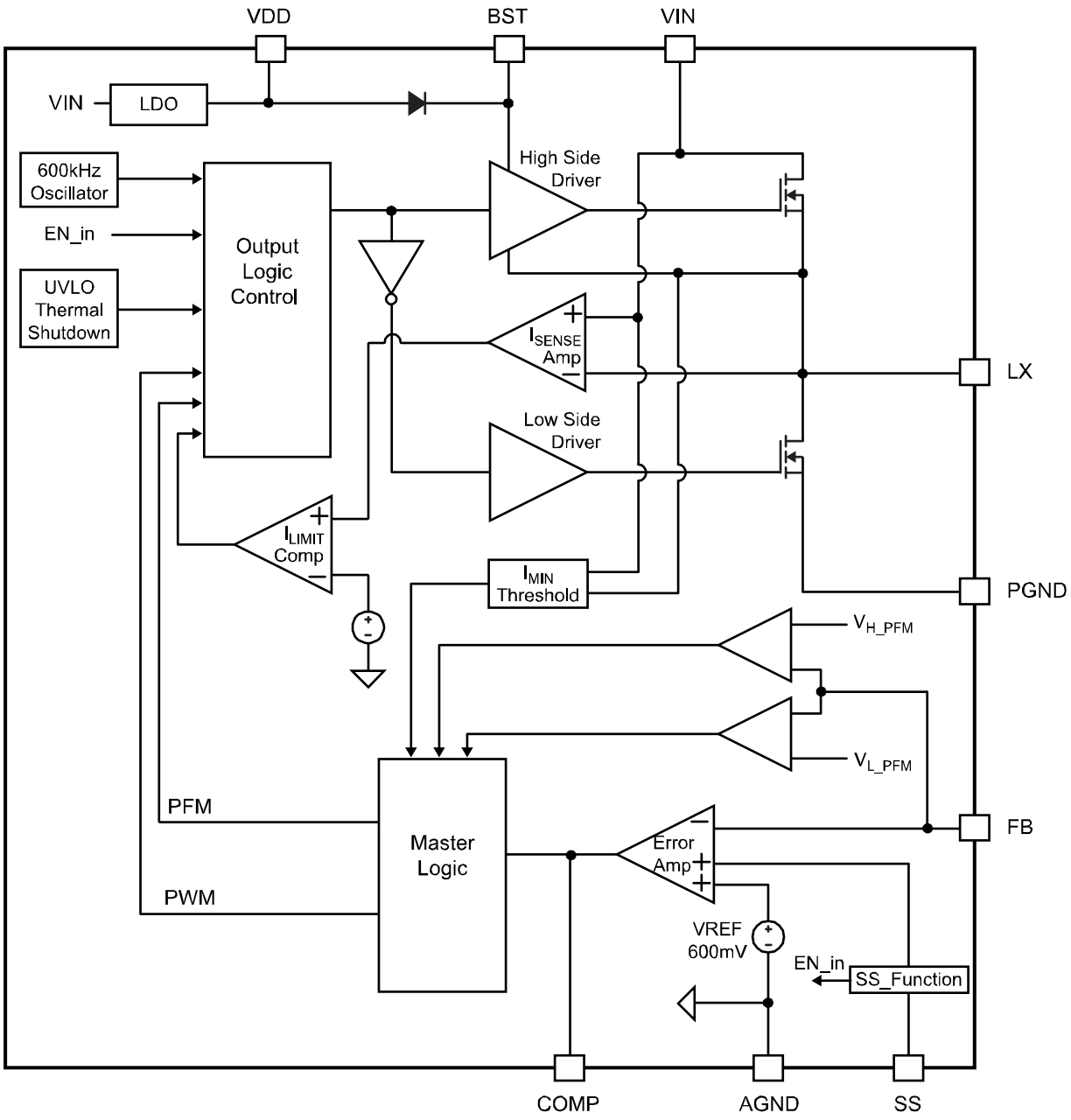


EPAD SO-8
(Top View)

Pin Description

Part Number	Pin Name	Pin Function
1	PGND	Power Ground connection.
2	VIN	Input Voltage Supply Pin. When VIN rises above the UVLO threshold the device starts up. **Note**: Connect close decoupling capacitor from VIN to PGND to minimize input switching loop.
3	BST	Bootstrap Connection for High-side NFET Gate Drive Input. Connect 10nF capacitor from BST to LX.
4	SS	Soft Start Input. Connect a capacitor between SS to GND for soft start time control.
5	COMP	External Loop Compensation Input.
6	AGND	Signal Ground Input.
7	FB	The Feedback Voltage Input. It is used to determine the output voltage via a resistor divider between the output and AGND.
8	VDD	Internal LDO Voltage Output. Connect a 1µF capacitor close to VDD to AGND.
Exposed Pad	LX	Output Connection to Inductor. Thermal connection for output stage.

Functional Block



Absolute Maximum Ratings

Exceeding the Absolute Maximum Ratings may damage the device.

Parameter	Rating
Supply Voltage (V_{IN})	30V
LX to GND	-0.7V to VIN+0.3V
SS to GND	-0.3V to +6V
BST to LX	-0.3V to +6V
FB to GND	-0.3V to +6V
COMP to GND	-0.3V to +6V
Junction Temperature (T_J)	+150°C
Storage Temperature (T_S)	-65°C to +150°C
ESD Rating(1)	2kV

Note:

1. Devices are inherently ESD sensitive, handling precautions are required. Human body model rating: 1.5kΩ in series with 100pF.

Recommended Operating Ratings

This device is not guaranteed to operate beyond the Recommended Operating Ratings.

Parameter	Rating
Supply Voltage (V_{IN})	4.5V to 26V
Output Voltage (V_{OUT})	0.6V to VIN
Ambient Temperature (T_A)	-40°C to +85°C
Package Thermal Resistance	
EPAD SO-8 (Θ_{JA})	50°C/W

Electrical Characteristics

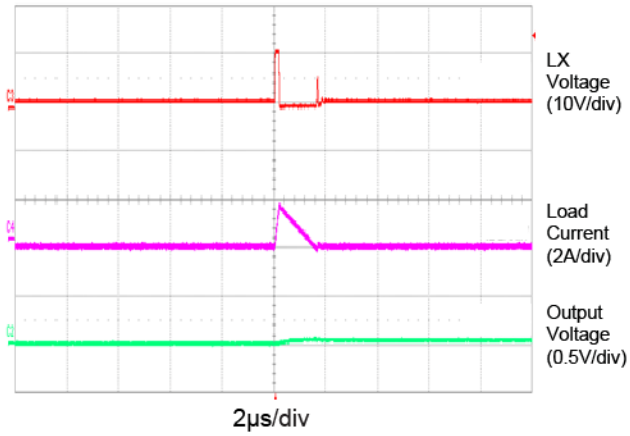
T_A = 25°C, V_{VIN} = 12V, V_{SS} = 2.5V, V_{OUT} = 3.3V unless otherwise specified. Specifications in **BOLD** indicate an ambient temperature range of -40°C to +85°C.

Symbol	Parameter	Conditions	Min.	Typ.	Max	Units
V_{VIN}	Supply Voltage		**4.5**		**26**	V
V_{UVLO}	Input Under-Voltage Lockout Threshold	V_{VIN} rising V_{VIN} falling	3.3		4.1	V
I_{VIN}	Supply Current (Quiescent)	I_{OUT} = 0, VFB = 0.8V		0.9	1.5	mA
I_{OFF}	Shutdown Supply Current	V_{SS} = 0V			**20**	µA
V_{VDD}	LDO Voltage	V_{VIN} > 6V		5.2		V
V_{FB}	Feedback Voltage		591	600	609	mV
V_{FB_LOAD}	Load Regulation	0.8A < I_{OUT} < 3.2A		0.5		%
V_{FB_LINE}	Line Regulation	6V < V_{VIN} < 26V, Load = 1A		0.05		%/V
I_{FB}	Feedback Input Current	V_{FB} = 0.6V			100	nA
V_{SS_OFF}	Enable Threshold	Off *threshold*			**0.4**	V
I_{SS}	SS Source Current	V_{SS} = 2.0V	-30	2.5	30	µA
Modulator						
F_s	Frequency		500	620	740	kHz
D_{MAX}	Maximum Duty Cycle			87		%
T_{ON_MIN}	Minimum On Time			80		ns
GM_{SYS}	System Loop Transconductance	I_{OUT}/V_{COMP}		5		A/V
GM_{EA}	Error Amplifier Transconductance			1		mA/V
Protection						
I_{LIM}	Current Limit		4	4.5		A
T_{OTP_RISE}	Over-Temperature Shutdown Limit	Temperature rising		155		°C
T_{OTP_FALL}		Temperature falling		115		°C
Outputs						
R_{DSON_HS}	High-Side Switch ON Resistance			115	170	mΩ
R_{DSON_HS}	Low-Side Switch ON Resistance			30	60	mΩ

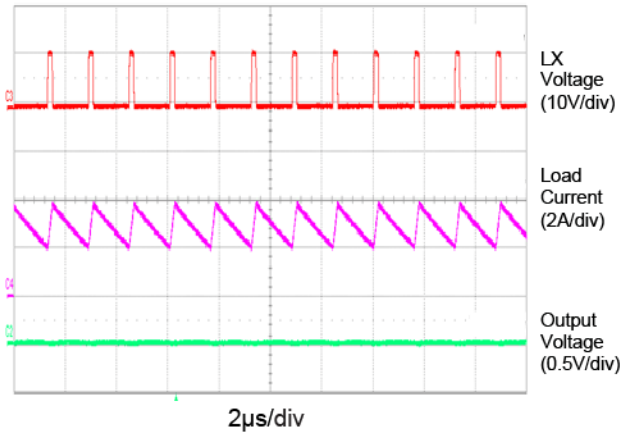
Typical Performance Characteristics

T_A = 25°C, V_{IN} = 12V, V_{OUT} = 1.1V unless otherwise specified.

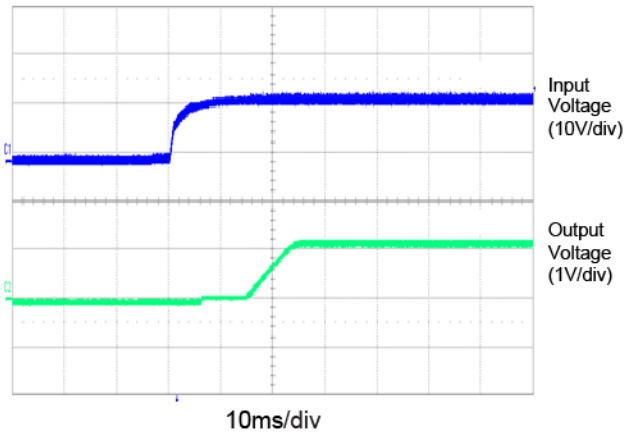
Light Load Operation



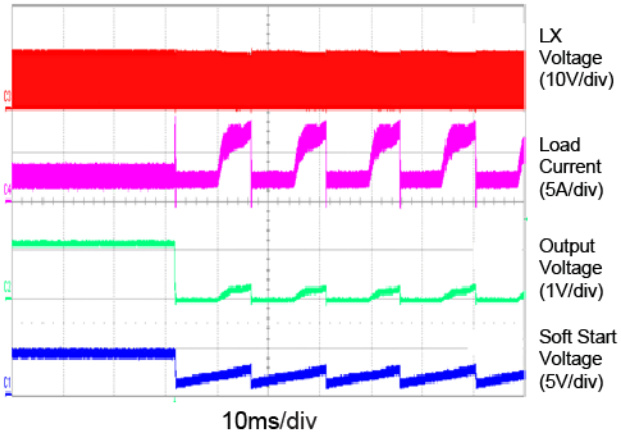
Full Load Operation



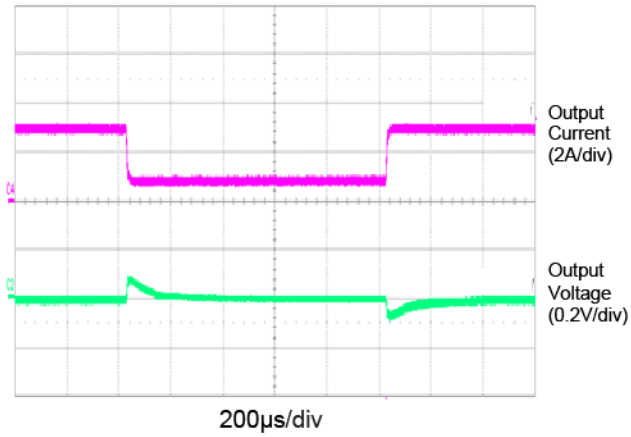
Start-Up to Full Load



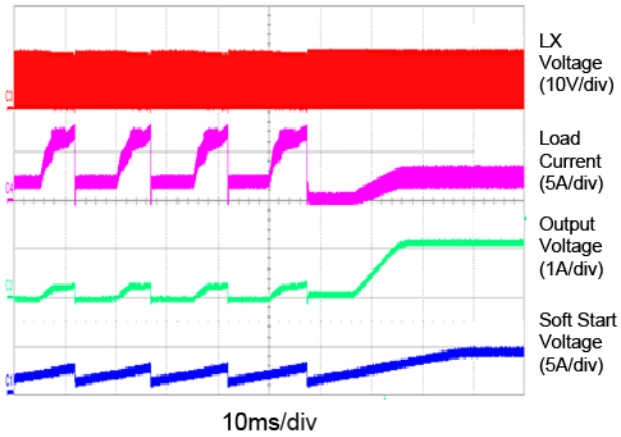
Short Circuit Protection

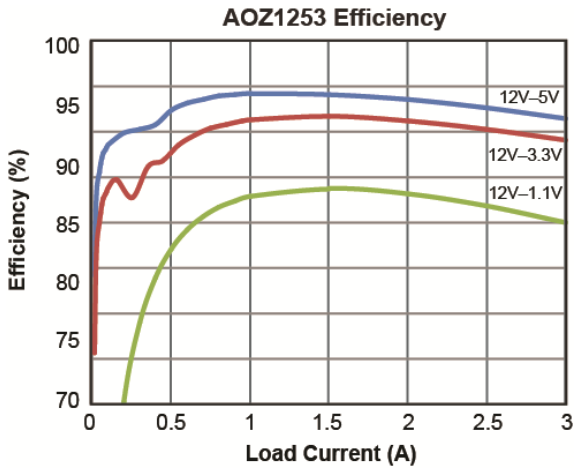


Load Transient



Short Circuit Recovery





Detailed Description

The AOZ1253 is a high efficiency current-mode buck regulator with integrated both high-side and low-side NMOS switches. It has a wide operating input voltage range of 4.5V to 26V and can supply up to 3A of output load current. AOZ1253's key protection features include input under voltage lockout, output over voltage protection, cycle by cycle current limit, fault short protection and thermal shut down. The AOZ1253 is available in the exposed pad SO-8 package.

Soft Start

AOZ1253 starts a soft start that can be adjusted by an external capacitor. The internal 2.5μA current source starts to charge the external capacitor through the soft-start pin. When soft-start voltage is higher than internal enable threshold voltage, the IC starts to switch with minimum on-time. With the soft-start voltage further increasing, the IC starts to switch with wider on-time, which drives the output (FB) following the soft-start voltage until output reaches the pre-set value. The output soft-start time can be calculated by:

$$T_{SS} = 0.6 \times \frac{C_{SS}}{I_{SS}}$$

Light Load and PWM Operation

Under low output current settings, AOZ1253 will operate in light load mode to obtain high efficiency. The two modes of operation, PFM and PWM are determined by the peak inductor current level and the output feedback voltage. For very low output current and consequently low peak inductor current, AOZ1253 will operate under critical inductor current mode if FB voltage is lower than threshold of V_{H_PFM}. V_{H_PFM} is 10mV higher than normal voltage reference. If output is higher than that value, IC will turn-off to keep high light load efficiency. As the output current increases, the IC will leave PFM mode and will enter PWM mode operating in fixed frequency continuous conduction mode (CCM). In CCM mode, AOZ1253 operates with the low side MOSFET switching in synchronous rectification to obtain high efficiency performance.

Error Amplifier

AOZ1253 uses an error amplifier that has a transconductance of 1000μA/V. Closed loop stability is realized through the frequency compensation network connected between COMP to AGND. (Refer to Loop Compensation)

Slope Compensation

A slope compensation ramp is also added in the control loop design to prevent sub harmonic oscillations. There is sufficient inductor current information to obtain stabile current mode operation. The output voltage is divided by the resistive voltage divider at the FB pin. The internal transconductance error amplifier then amplifies the difference between the voltages at FB with the reference voltage. The error signal voltage is an input to the COMP and is compared against the current signal which consists of both the inductor current and slope comp ramp at the PWM comparator input. If this current signal is less than the error voltage the high side switch will turn on.

Switching Frequency

The AOZ1253 has a fixed switching frequency under PWM mode of operation through an internal oscillator. Its nominal switching frequency is set to 600kHz.

Output Voltage Setting

The output voltage is set by a resistor divider network of R_1 and R_2, by feeding back the output to the FB pin. The output setting is defined by:

$$V_O = 0.6 \times \left(1 + \frac{R_1}{R_2}\right)$$

Below Table 1 lists popular regulated outputs and the corresponding values of R_1, R_2.

V_O (V)	R_1 (kΩ)	R_2 (kΩ)
0.6		Open
1.0	6.67	10
1.5	15	10
1.8	20	10
2.5	31.7	10
3.3	45	10
5.0	73.3	10

Table 1.Output Voltage Setting with Resistor Divider

The combination of R_1 and R_2 should be large enough to avoid drawing excessive current from the output that contributes to power loss. Since the switch duty cycle can be as high as 100%, the maximum output voltage can be set as high as the input voltage minus the voltage drop of the high side NMOS and inductor .

Over Current Protection (OCP)

The primary signal used in over current protection is the peak inductor. By employing peak current mode control, the COMP voltage is proportional to the peak inductor current. This voltage falls between the range of 0.4V and 2.5V, increasing with output load current. AOZ1253 utilizes cycle by cycle current limit and limits the peak inductor current. A preset current limit voltage is used as a reference trip point. When the output current exceeds the current limit range, the high side switch will stop switching.

Under fault conditions where the output maybe shorted to ground, V_{OUT} will drop rapidly and AOZ1253's protection circuit will force the inductor current to decay once the OCP level is reached within several switching cycles. This feature helps to prevent catastrophic failure and recovery of the IC once the short is removed. AOZ1253 will initiate a soft start once the over-current condition is removed.

Thermal Protection

An internal temperature sensor monitors the junction temperature of the controller. The internal control circuit shuts down the high-side NMOS once the junction temperature exceeds 150ºC. The regulator has a 50° hysteresis and will automatically restart when the junction temperature decreases to 100ºC.

Input capacitor

The input bypass capacitor must be connected very closely to the V_{IN} and PGND pins of AOZ1253. This mainly to ensure that proper filtering is maintained to filter out the pulsing input current inherent to buck regulator switching. The voltage rating of input capacitor is selected to be higher than maximum input voltage plus the input ripple voltage.

The input ripple voltage can be approximated by equation below:

$$\Delta V_{IN} = \frac{I_O}{f \times C_{IN}} \times \left(1 - \frac{V_O}{V_{IN}}\right) \times \frac{V_O}{V_{IN}}$$

Since the input current is discontinuous in a buck converter, the current stress on the input capacitor is one key concern when selecting the capacitor. For a buck regulator, the RMS value of input capacitor current can be calculated by:

$$I_{CIN\_RMS} = I_O \times \sqrt{\frac{V_O}{V_{IN}}\left(1 - \frac{V_O}{V_{IN}}\right)}$$

m equals the conversion ratio:

$$\frac{V_O}{V_{IN}} = m$$

The relationship between the input capacitor RMS current and voltage conversion ratio is calculated and shown in Figure 1 below. It can be seen that when V_O is half of V_{IN}, C_{IN} is under the worst current stress. The worst current stress on C_{IN} is $0.5 \cdot I_O$.

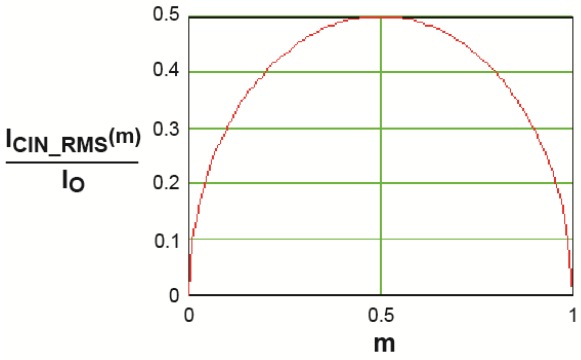


Figure 1. I_{CIN} vs. Voltage Conversion Ratio

To ensure reliable operation, the input capacitors must be selected to have a current rating higher than $I_{CIN-RMS}$ at the worst operating conditions. Ceramic capacitors are preferred for input capacitors because of their low ESR and high current rating. Depending on the application circuits, other low ESR tantalum capacitor may also be used. When selecting ceramic capacitors, X5R or X7R type dielectric ceramic capacitors should be used for their better temperature and voltage characteristics. Note that the ripple current rating from capacitor manufactures is based on certain amount of life time. Further de-rating may be necessary in practical design.

Inductor

The inductor is used to supply constant current to output when it is driven by a switching voltage. For given input and output voltage, inductance and switching frequency together decide the inductor ripple current, which is:

$$\Delta I_L = \frac{V_O}{f \times L} \times \left(1 - \frac{V_O}{V_{IN}}\right)$$

The peak inductor current is:

$$I_{Lpeak} = I_O + \frac{\Delta I_L}{2}$$

High inductance gives low inductor ripple current but requires larger size inductor to avoid saturation. Low ripple current reduces inductor core losses. It also reduces RMS current through inductor and switches, which results in less conduction loss. Usually, peak to peak ripple current on inductor is designed to be 20% to 30% of output current.

When selecting the inductor, make sure it is able to handle the peak current without saturation even at the highest operating temperature.

The inductor takes the highest current in a buck circuit. The conduction loss on inductor needs to be checked for thermal and efficiency requirements.

Surface mount inductors in different shape and styles are available from Coilcraft, Elytone and Murata. Shielded inductors are small and radiate less EMI noise. But they cost more than unshielded inductors. The choice depends on EMI requirement, price and size.

Output Capacitor

The output capacitor is selected based on the DC output voltage rating, output ripple voltage specification and ripple current rating. The selected output capacitor must have a higher rated voltage specification than the maximum desired output voltage including ripple. De-rating needs to be considered for long term reliability. Output ripple voltage specification is another important factor for selecting the output capacitor. In a buck converter circuit, output ripple voltage is determined by inductor value, switching frequency, output capacitor value and ESR. It can be calculated by the equation below:

$$\Delta V_O = \Delta I_L \times \left(ESR_{CO} + \frac{1}{8 \times f \times C_O}\right)$$

where,

C_O is output capacitor value and

ESR_{CO} is the Equivalent Series Resistor of output capacitor.

When low ESR ceramic capacitor is used as output capacitor, the impedance of the capacitor at the switching frequency dominates. Output ripple is mainly caused by capacitor value and inductor ripple current. The output ripple voltage calculation can be simplified to:

$$\Delta V_O = \Delta I_L \times \frac{1}{8 \times f \times C_O}$$

If the impedance of ESR at switching frequency dominates, the output ripple voltage is mainly decided by capacitor ESR and inductor ripple current. The output ripple voltage calculation can be further simplified to:

$$\Delta V_O = \Delta I_L \times ESR_{CO}$$

For lower output ripple voltage across the entire operating temperature range, X5R or X7R dielectric type of ceramic, or other low ESR tantalum are recommended to be used as output capacitors.

In a buck converter, output capacitor current is continuous. The RMS current of output capacitor is decided by the peak to peak inductor ripple current. It can be calculated by:

$$I_{CO\_RMS} = \frac{\Delta I_L}{\sqrt{12}}$$

Usually, the ripple current rating of the output capacitor is a smaller issue because of the low current stress. When the buck inductor is selected to be very small and inductor ripple current is high, output capacitor could be overstressed.

Loop Compensation

The AOZ1253 employs peak current mode control for ease-of-use and fast transient response. Peak current mode control eliminates the double pole effect of the output L&C filter. It greatly simplifies the compensation loop design.

With peak current mode control, the buck power stage can be simplified to be a one-pole and one-zero system in frequency domain. The pole is dominant pole can be calculated by:

$$f_{p1} = \frac{1}{2\pi \times C_O \times R_L}$$

The zero is an ESR zero due to output capacitor and it's ESR. It is can be calculated by:

$$f_{Z1} = \frac{1}{2\pi \times C_O \times ESR_{CO}}$$

where,

C_O is the output filter capacitor;

R_L is load resistor value; and

ESR_{CO} is the equivalent series resistance of output capacitor.

The compensation design is actually to shape the converter control loop transfer function to get desired gain and phase. Several different types of compensation network can be used for the AOZ1253. For most cases, a series capacitor and resistor network connected to the COMP pin sets the pole-zero and is adequate for a stable high-bandwidth control loop.

In the AOZ1253, FB pin and COMP pin are the inverting input and the output of internal error amplifier. A series R and C compensation network connected to COMP provides one pole and one zero. The pole is:

$$f_{p2} = \frac{G_{EA}}{2\pi \times C_C \times G_{VEA}}$$

where,

G_{EA} is the error amplifier transconductance, which is $1000 \cdot 10^{-6}$ A/V;

G_{VEA} is the error amplifier voltage gain, which is 500 V/V; and

C_C is compensation capacitor in the Typical Application schematic on the first page.

The zero given by the external compensation network, capacitor C_C and resistor R_C is located at:

$$f_{Z2} = \frac{1}{2\pi \times C_C \times R_C}$$

To design the compensation circuit, a target crossover frequency f_C for close loop must be selected. The system crossover frequency is where control loop has unity gain. The crossover is the also called the converter bandwidth. Generally a higher bandwidth means faster response to load transient. However, the bandwidth should not be too high because of system stability concern. When designing the compensation loop, converter stability under all line and load condition must be considered.

Usually, it is recommended to set the bandwidth to be equal or less than 1/10 of switching frequency. It is recommended to choose a crossover frequency equal or less than 60kHz.

The strategy for choosing R_C and C_C is to set the cross over frequency with R_C and set the compensator zero with C_C. Using selected crossover frequency, f_C, to calculate R_C:

$$R_C = f_C \times \frac{V_O}{V_{FB}} \times \frac{2\pi \times C_O}{G_{EA} \times G_{CS}}$$

where,

f_C is desired crossover frequency. For best performance, f_C is set to be about 1/10 of switching frequency;

V_{FB} is 0.6V;

G_{EA} is the error amplifier transconductance, which is $1000 \cdot 10^{-6}$ A/V; and

G_{CS} is the current sense circuit transconductance, which is 4 A/V.

The compensation capacitor C_C and resistor R_C together make a zero. This zero is put somewhere close to the dominate pole f_{p1} but lower than 1/5 of selected crossover frequency. C_C can is selected by:

$$C_C = \frac{1.5}{2\pi \times R_C \times F_{p1}}$$

Equation above can also be simplified to:

$$C_C = \frac{C_O \times R_L}{R_C}$$

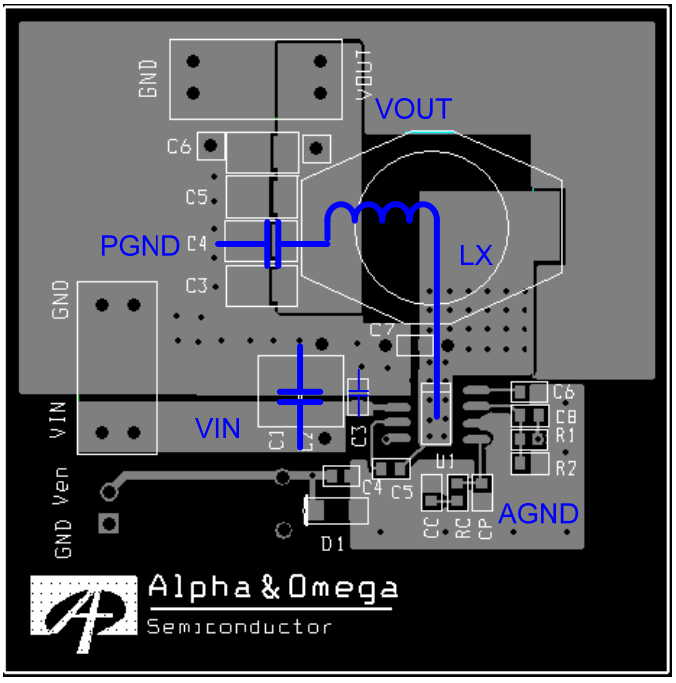
PCB Layout Consideration

As with all high current switching buck regulators, circuit board layout is the key in preventing inductive overshoots and undershoots transient spikes. There are essentially two high pulsing current loops in a synchronous buck converter. The first switching loop is formed when the high-side MOSFET is switched on. The circulating current flows from the input capacitors, to the filter inductor, to the output capacitors (load), then returns to the input capacitor through power ground. It is imperative that a low inductive ceramic capacitor be placed directly across VIN (PIN2) and PGND (PIN1) to reduce the switching loop during the high side turn on transition.

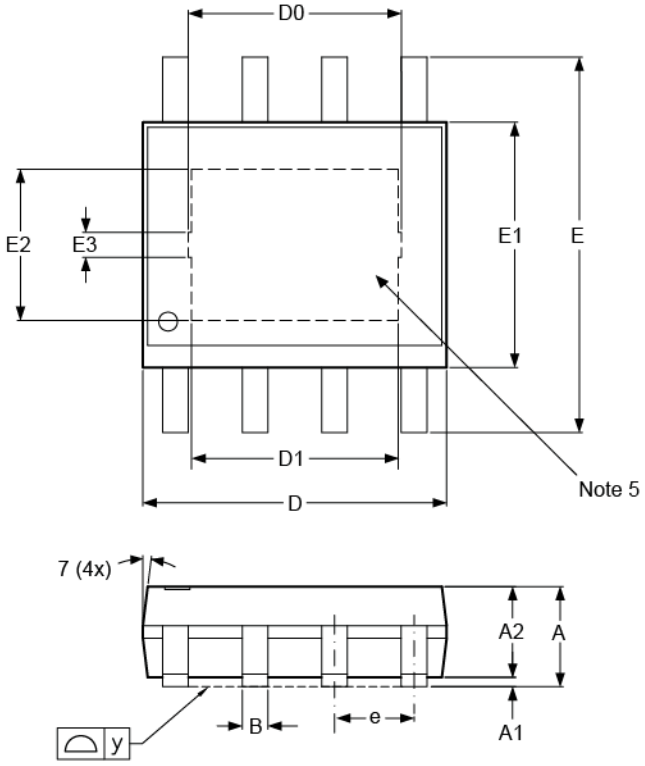
The second loop is formed when the low-side MOSFET is switched on during synchronous operation. This loop is formed from the inductor, to the output capacitors (load), then returns through the low-side MOSFET. The PCB layout for the AOZ1253 is shown below. It can be seen that the input bypassing capacitors are placed in close proximity to VIN and PGND. Analog ground and power grounds are separated to filter out noise from the main power switching loops. The sensitive nodes that require connection through analog ground (AGND) are COMP, FB, and VSS.

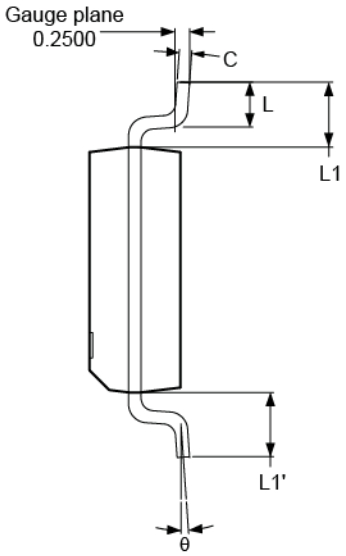
PCB guideline that can be helpful:

1. The exposed (LX) node serves as the interconnect of both high-side and low-side MOSFETs. It is suggested that a large copper plane added underneath the IC to improve thermal dissipation.
2. To improve high-side thermal dissipation, maximize the copper area connected to the VIN pin.
3. The input capacitor should be connected in close proximity to the VIN pin and the PGND pins.
4. A ground plane is strongly recommended. Separate PGND from AGND and connect them at a single point to avoid noise coupling.
5. Form a short wide trace from LX to the output inductor and capacitors.
6. The LX switching node is the noisiest of all pins; therefore, all sensitive nodes must be far away from this pin.

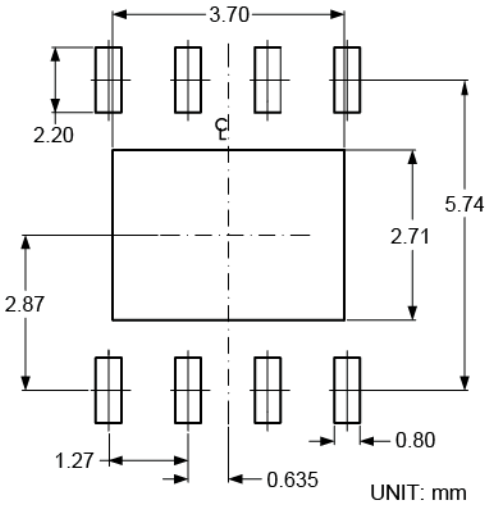


Package Dimensions, Exposed Pad SO-8





RECOMMENDED LAND PATTERN



Dimensions in millimeters

Symbols	Min.	Nom.	Max.
A	1.40	1.55	1.70
A1	0.00	0.05	0.10
A2	1.40	1.50	1.60
B	0.31	0.406	0.51
C	0.17	—	0.25
D	4.80	4.96	5.00
D0	3.20	3.40	3.60
D1	3.10	3.30	3.50
E	5.80	6.00	6.20
e	—	1.27	—
E1	3.80	3.90	4.00
E2	2.21	2.41	2.61
E3	0.40 REF		
L	0.40	0.95	1.27
y	—	—	0.10
θ	0°	3°	8°
| L1–L1' |	—	0.04	0.12
L1	1.04 REF		

Dimensions in inches

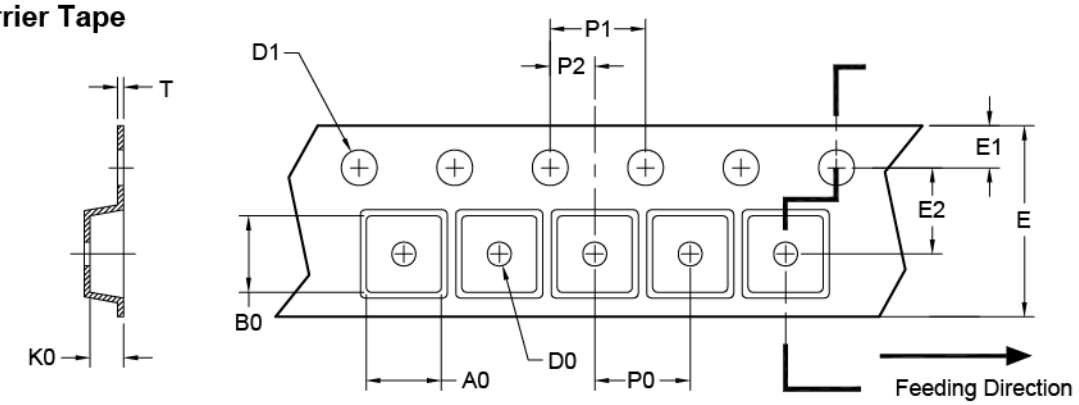
Symbols	Min.	Nom.	Max.
A	0.055	0.061	0.067
A1	0.000	0.002	0.004
A2	0.055	0.059	0.063
B	0.012	0.016	0.020
C	0.007	—	0.010
D	0.189	0.195	0.197
D0	0.126	0.134	0.142
D1	0.122	0.130	0.138
E	0.228	0.236	0.244
e	—	0.050	—
E1	0.150	0.153	0.157
E2	0.087	0.095	0.103
E3	0.016 REF		
L	0.016	0.037	0.050
y	—	—	0.004
θ	0°	3°	8°
| L1–L1' |	—	0.002	0.005
L1	0.041 REF		

Notes:

1. Package body sizes exclude mold flash and gate burrs.
2. Dimension L is measured in gauge plane.
3. Tolerance 0.10mm unless otherwise specified.
4. Controlling dimension is millimeter, converted inch dimensions are not necessarily exact.
5. Die pad exposure size is according to lead frame design.
6. Followed from JEDEC MS-012

Tape and Reel Dimensions, Exposed Pad SO-8

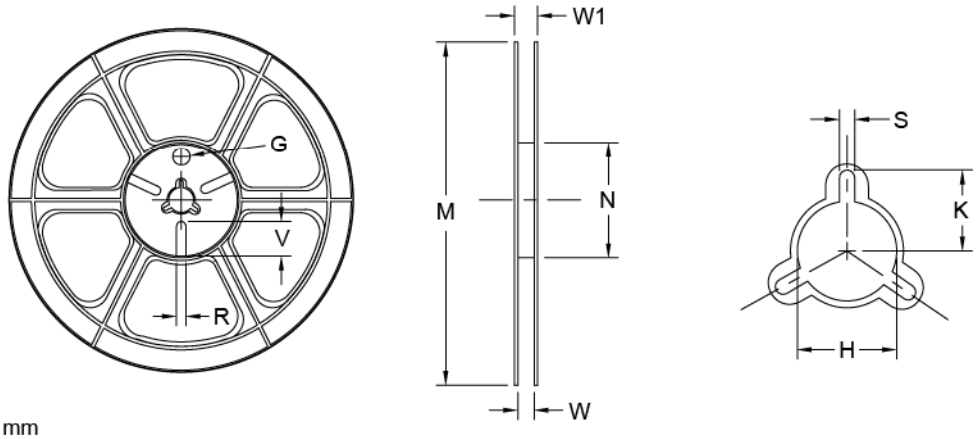
Carrier Tape



UNIT: mm

Package	A0	B0	K0	D0	D1	E	E1	E2	P0	P1	P2	T
SO-8 (12mm)	6.40 ±0.10	5.20 ±0.10	2.10 ±0.10	1.60 ±0.10	1.50 ±0.10	12.00 ±0.10	1.75 ±0.10	5.50 ±0.10	8.00 ±0.10	4.00 ±0.10	2.00 ±0.10	0.25 ±0.10

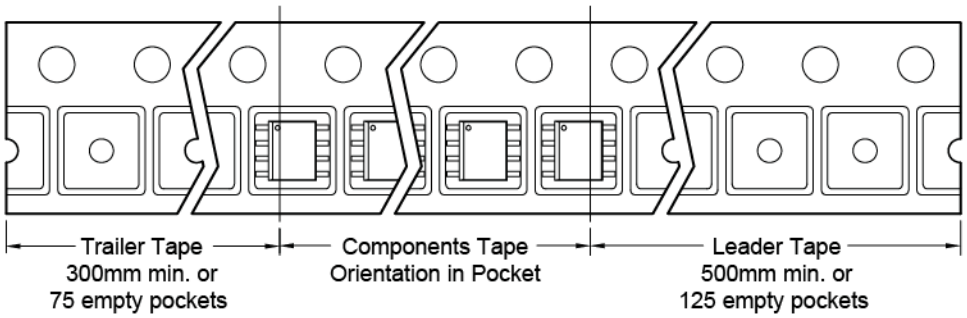
Reel



UNIT: mm

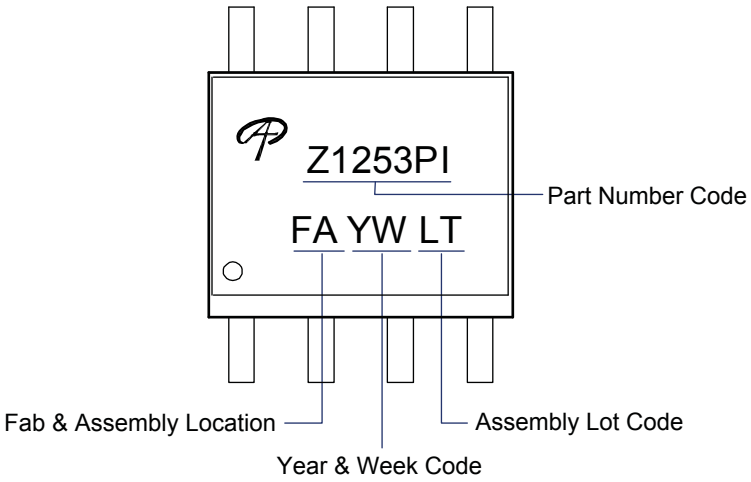
Tape Size	Reel Size	M	N	W	W1	H	K	S	G	R	V
12mm	ø330	ø330.00 ±0.50	ø97.00 ±0.10	13.00 ±0.30	17.40 ±1.00	ø13.00 +0.50/-0.20	10.60	2.00 ±0.50	—	—	—

Leader/Trailer and Orientation



Part Marking

AOZ1253PI
(EPAD SO-8)



This datasheet contains preliminary data; supplementary data may be published at a later date.
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As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.

2. A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.