

NTMS4177P

Power MOSFET

-30 V, -11.4 A, P-Channel, SOIC-8

Features

- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Capacitance to Minimize Driver Losses
- Optimized Gate Charge to Minimize Switching Losses
- SOIC-8 Surface Mount Package Saves Board Space
- This is a Pb-Free Device

Applications

- Load Switches
- Notebook PC's
- Desktop PC's

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise stated)

Rating	Symbol	Value	Unit	
Drain-to-Source Voltage	V_{DSS}	-30	V	
Gate-to-Source Voltage	V_{GS}	± 20	V	
Continuous Drain Current $R_{\theta JA}$ (Note 1)	I_D	$T_A = 25^\circ\text{C}$	-8.9	A
		$T_A = 70^\circ\text{C}$	-7.1	
Power Dissipation $R_{\theta JA}$ (Note 1)	P_D	1.52	W	
Continuous Drain Current $R_{\theta JA}$ (Note 2)	I_D	$T_A = 25^\circ\text{C}$	-6.6	A
		$T_A = 70^\circ\text{C}$	-5.3	
Power Dissipation $R_{\theta JA}$ (Note 2)	P_D	0.84	W	
Continuous Drain Current $R_{\theta JA} t < 10$ s (Note 1)	I_D	$T_A = 25^\circ\text{C}$	-11.4	A
		$T_A = 70^\circ\text{C}$	-9.3	
Power Dissipation $R_{\theta JA} t < 10$ s (Note 1)	P_D	2.5	W	
Pulsed Drain Current	I_{DM}	-46	A	
Operating Junction and Storage Temperature	T_J, T_{STG}	-55 to +150	$^\circ\text{C}$	
Source Current (Body Diode)	I_S	-2.1	A	
Single Pulse Drain-to-Source Avalanche Energy $T_J = 25^\circ\text{C}$, $V_{DD} = 30$ V, $V_{GS} = 10$ V, $I_L = 20$ A _{pk} , $L = 1.0$ mH, $R_G = 25 \Omega$	EAS	200	mJ	
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)	T_L	260	$^\circ\text{C}$	

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Surface-mounted on FR4 board using 1 inch sq pad size, 1 oz Cu.
2. Surface-mounted on FR4 board using the minimum recommended pad size.

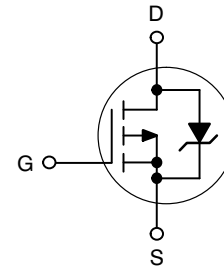


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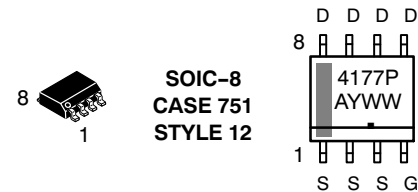
<http://onsemi.com>

$V_{(BR)DSS}$	$R_{DS(on)}$ Max	I_D Max
-30 V	12 m Ω @ -10 V	-11.4 A
	19 m Ω @ -4.5 V	

P-Channel



MARKING DIAGRAM & PIN ASSIGNMENT



4177P = Device Code
 A = Assembly Location
 Y = Year
 WW = Work Week
 ■ = Pb-Free Package

ORDERING INFORMATION

Device	Package	Shipping†
NTMS4177PR2G	SOIC-8 (Pb-Free)	2500/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

NTMS4177P

THERMAL RESISTANCE RATINGS

Rating	Symbol	Max	Unit
Junction-to-Ambient – Steady State (Note 3)	$R_{\theta JA}$	82	°C/W
Junction-to-Ambient – $t \leq 10$ s (Note 3)	$R_{\theta JA}$	50	
Junction-to-FOOT (Drain)	$R_{\theta JF}$	20	
Junction-to-Ambient – Steady State (Note 4)	$R_{\theta JA}$	148	

3. Surface-mounted on FR4 board using 1 inch sq pad size, 1 oz Cu.

4. Surface-mounted on FR4 board using the minimum recommended pad size.

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted)jk

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = -250\ \mu\text{A}$	-30			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$			29		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	$V_{GS} = 0\text{ V}, V_{DS} = -24\text{ V}$			-1.0	μA
					-5.0	
Gate-to-Source Leakage Current	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			± 100	nA

ON CHARACTERISTICS (Note 5)

Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = -250\ \mu\text{A}$	-1.5		-2.5	V
Negative Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$			6.0		mV/°C
Drain-to-Source On Resistance	$R_{DS(on)}$	$V_{GS} = -10\text{ V}, I_D = -11.4\text{ A}$ $V_{GS} = -4.5\text{ V}, I_D = -9.1\text{ A}$		10	12	m Ω
				15	19	
Forward Transconductance	g_{FS}	$V_{DS} = -1.5\text{ V}, I_D = -11.4\text{ A}$		30		S

CHARGES, CAPACITANCES AND GATE RESISTANCE

Input Capacitance	C_{ISS}	$V_{GS} = 0\text{ V}, f = 1.0\text{ MHz}, V_{DS} = -24\text{ V}$		3100		pF
Output Capacitance	C_{OSS}			550		
Reverse Transfer Capacitance	C_{RSS}			370		
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = -4.5\text{ V}, V_{DS} = -15\text{ V}, I_D = -11.4\text{ A}$		29		nC
Threshold Gate Charge	$Q_{G(TH)}$			3.3		
Gate-to-Source Charge	Q_{GS}			10		
Gate-to-Drain Charge	Q_{GD}			13		
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = -10\text{ V}, V_{DS} = -15\text{ V}, I_D = -11.4\text{ A}$		55		nC
Gate Resistance	R_G			2.0	4.0	Ω

SWITCHING CHARACTERISTICS (Note 6)

Turn-On Delay Time	$t_{d(ON)}$	$V_{GS} = -10\text{ V}, V_{DD} = -15\text{ V}, I_D = -1.0\text{ A}, R_G = 6.0\ \Omega$		18		ns
Rise Time	t_r			13		
Turn-Off Delay Time	$t_{d(OFF)}$			64		
Fall Time	t_f			36		

DRAIN-TO-SOURCE CHARACTERISTICS

Forward Diode Voltage	V_{SD}	$V_{GS} = 0\text{ V}, I_D = -2.1\text{ A}$	$T_J = 25^\circ\text{C}$		-0.73	-1.0	V
			$T_J = 125^\circ\text{C}$		0.54		ns
Reverse Recovery Time	t_{RR}	$V_{GS} = 0\text{ V}, d_{IS}/d_t = 100\text{ A}/\mu\text{s}, I_S = -2.1\text{ A}$			34		
Charge Time	T_a				18		
Discharge Time	T_b				16		
Reverse Recovery Time	Q_{RR}				30		

5. Pulse Test: pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$.

6. Switching characteristics are independent of operating junction temperatures.

TYPICAL PERFORMANCE CURVES

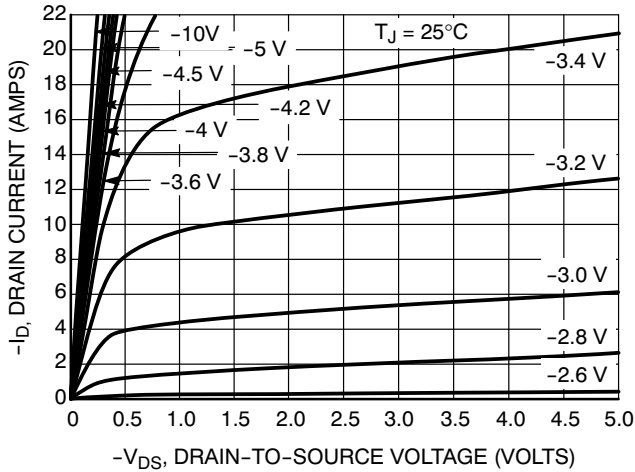


Figure 1. On-Region Characteristics

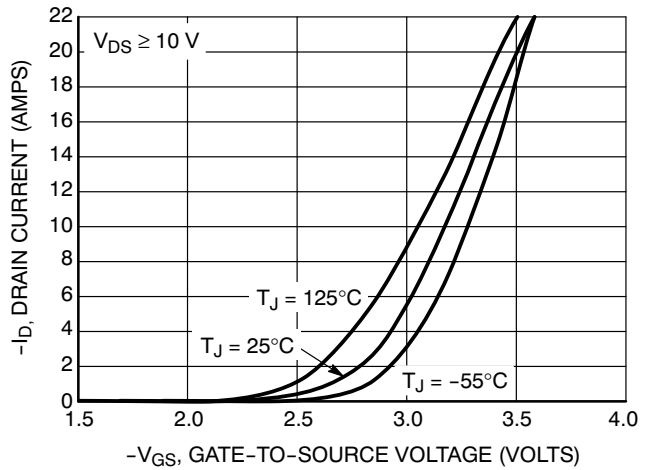


Figure 2. Transfer Characteristics

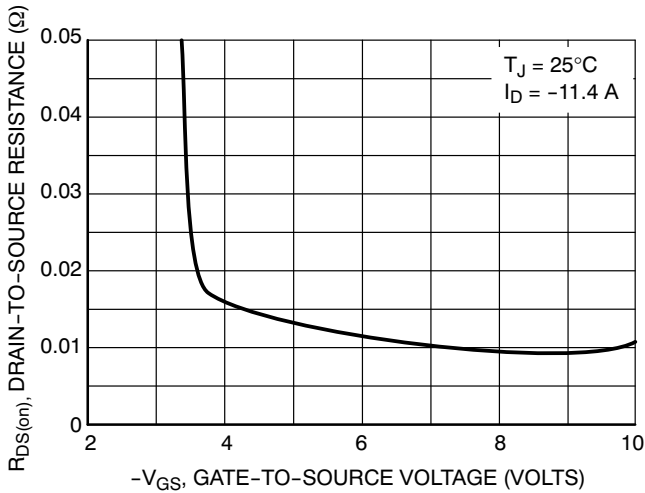


Figure 3. On-Resistance vs. Gate-to-Source Voltage

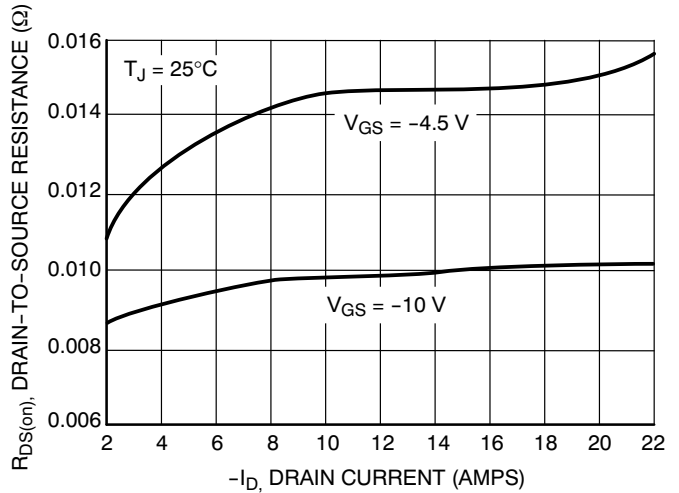


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

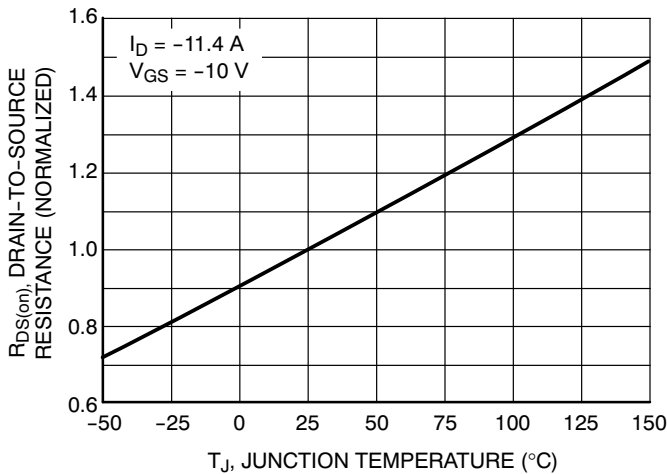


Figure 5. On-Resistance Variation with Temperature

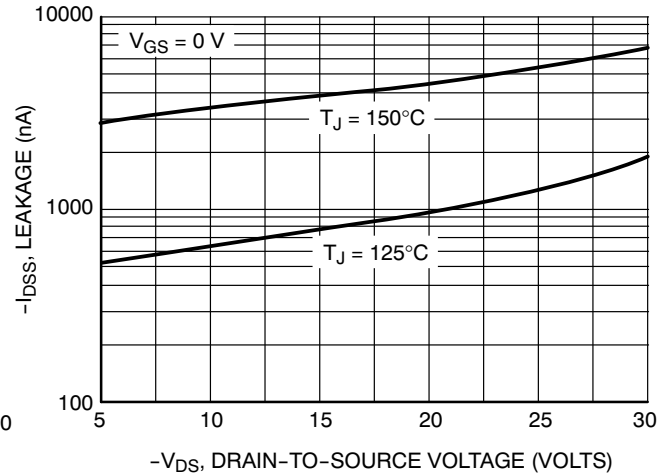


Figure 6. Drain-to-Source Leakage Current vs. Voltage

TYPICAL PERFORMANCE CURVES

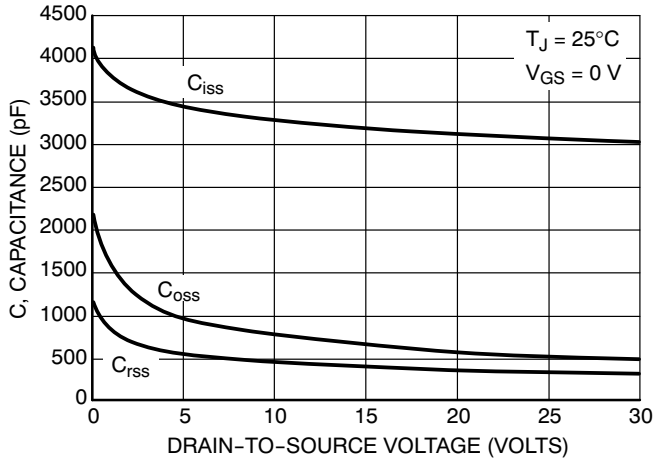


Figure 7. Capacitance Variation

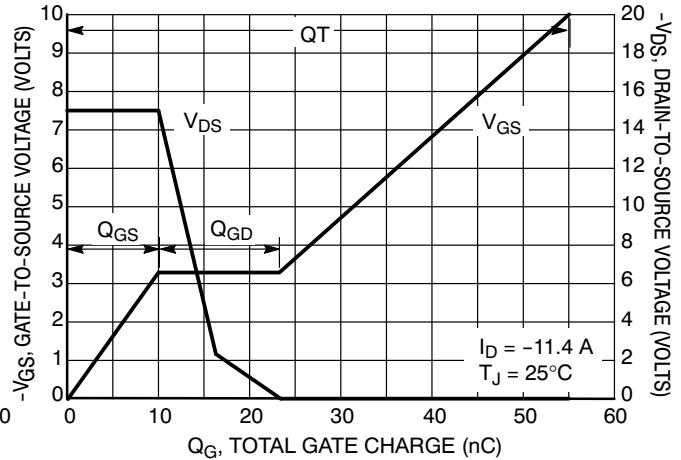


Figure 8. Gate-To-Source and Drain-To-Source Voltage vs. Total Charge

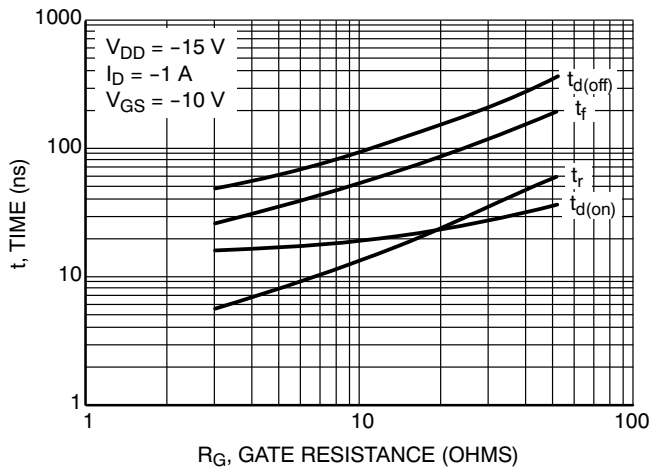


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

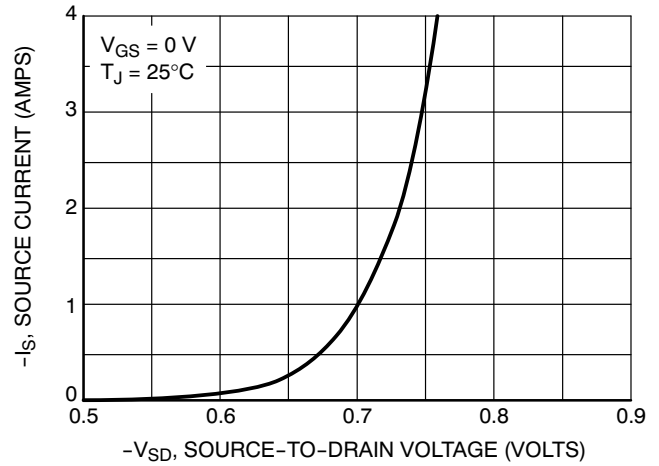


Figure 10. Diode Forward Voltage vs. Current

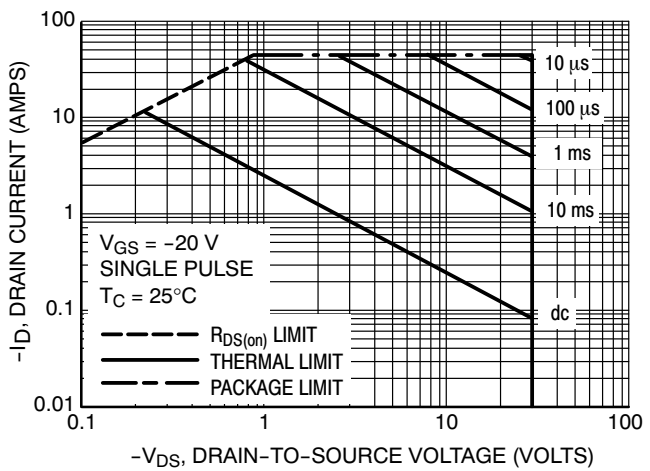


Figure 11. Maximum Rated Forward Biased Safe Operating Area

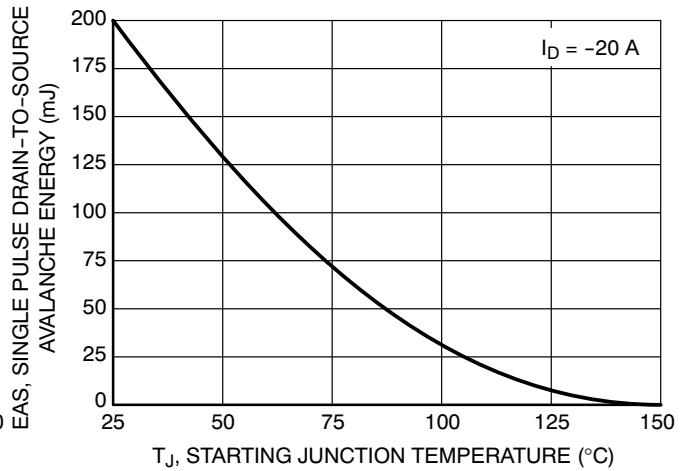
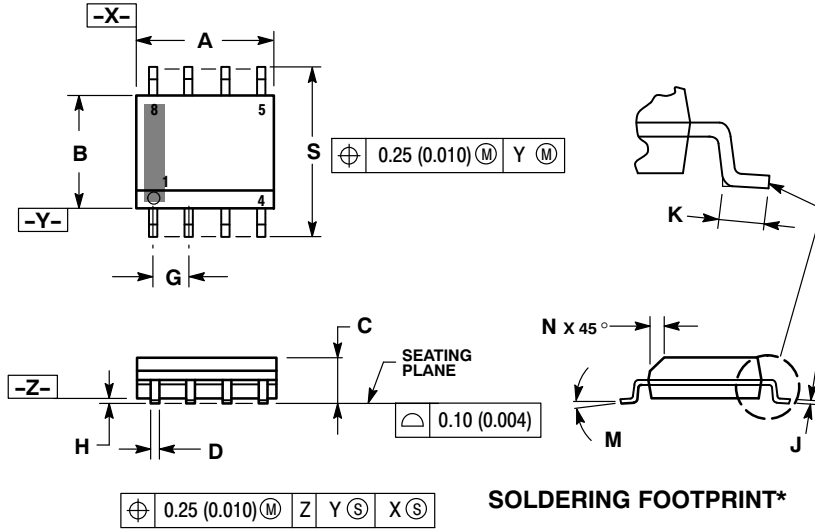


Figure 12. Maximum Avalanche Energy vs. Starting Junction Temperature

NTMS4177P

PACKAGE DIMENSIONS

SOIC-8 NB
CASE 751-07
ISSUE AJ

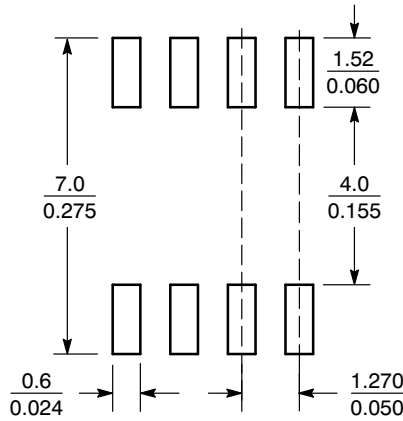


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°		8°	
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

SOLDERING FOOTPRINT*



SCALE 6:1 $\left(\frac{\text{mm}}{\text{inches}}\right)$

STYLE 12:

- PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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