



EMIF10-1K010F1

IPAD™

10 LINES EMI FILTER AND ESD PROTECTION

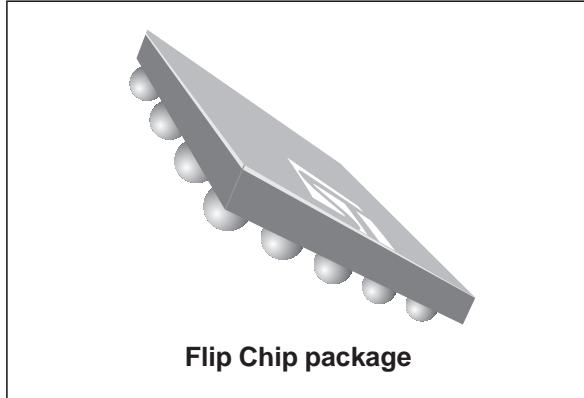
MAIN PRODUCT CHARACTERISTICS:

Where EMI filtering in ESD sensitive equipment is required :

- Mobile phones and communication systems
- Computers, printers and MCU Boards

DESCRIPTION

The EMIF10-1K010F1 is a highly integrated devices designed to suppress EMI/RFI noise in all systems subjected to electromagnetic interferences. The EMIF10 flip chip packaging means the package size is equal to the die size. This filter includes an ESD protection circuitry which prevents the device from destruction when subjected to ESD surges up 15kV.



Flip Chip package

BENEFITS

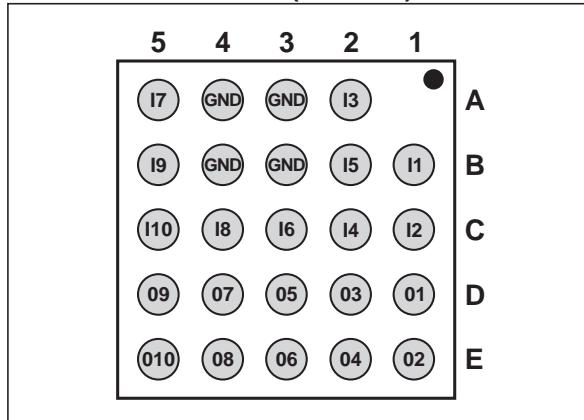
- EMI symmetrical (I/O) low-pass filter
- High efficiency in EMI filtering
- Very low PCB space consuming:
2.57mm x 2.57mm
- Very thin package: 0.65 mm
- High efficiency in ESD suppression
- High reliability offered by monolithic integration
- High reducing of parasitic elements through integration & wafer level packaging.

COMPLIES WITH THE FOLLOWING STANDARDS:

IEC61000-4-2

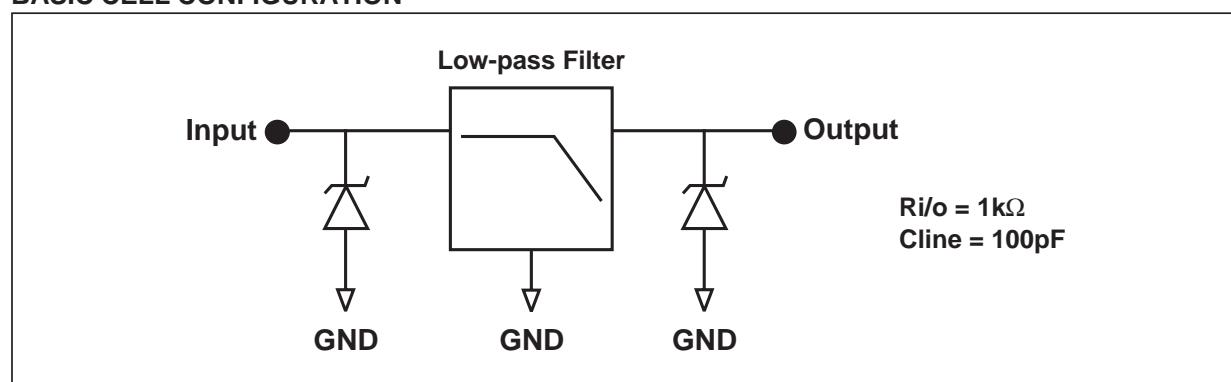
Level 4 15kV (air discharge)
 8 kV (contact discharge)

PIN CONFIGURATION (ball side)



MIL STD 883E - Method 3015-6 Class 3

BASIC CELL CONFIGURATION



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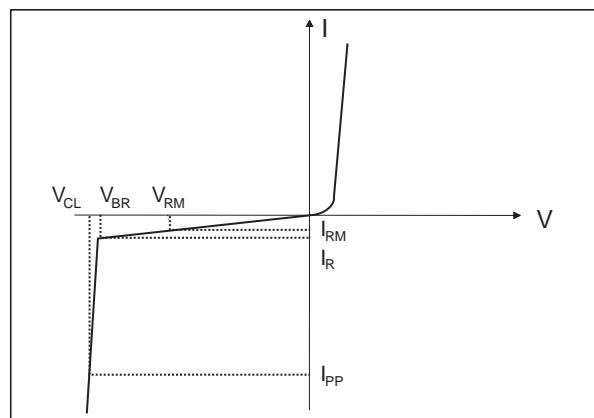
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ABSOLUTE MAXIMUM RATINGS ($T_{amb} = 25^{\circ}\text{C}$)

Symbol	Parameter and test conditions	Value	Unit
T_j	Junction temperature	125	$^{\circ}\text{C}$
T_{op}	Operating temperature range	-40 to +85	$^{\circ}\text{C}$
T_{stg}	Storage temperature range	-55 to +150	$^{\circ}\text{C}$

ELECTRICAL CHARACTERISTICS ($T_{amb} = 25^{\circ}\text{C}$)

Symbol	Parameters
V_{BR}	Breakdown voltage
I_{RM}	Leakage current @ V_{RM}
V_{RM}	Stand-off voltage
V_{CL}	Clamping voltage
R_d	Dynamic impedance
I_{PP}	Peak pulse current
$R_{I/O}$	Series resistance between Input & Output
C_{in}	Input capacitance per line



Symbol	Test conditions	Min	Typ	Max	Unit
V_{BR}	$I_R = 1\text{mA}$	6	8	10	V
I_{RM}	$V_{RM} = 3\text{V}$ per line			500	nA
$R_{I/O}$		900	1000	1100	Ω
C_{line}	At 0V bias	80	100	120	pF

Fig. 1: S21(dB) attenuation measurement and Aplac simulation.

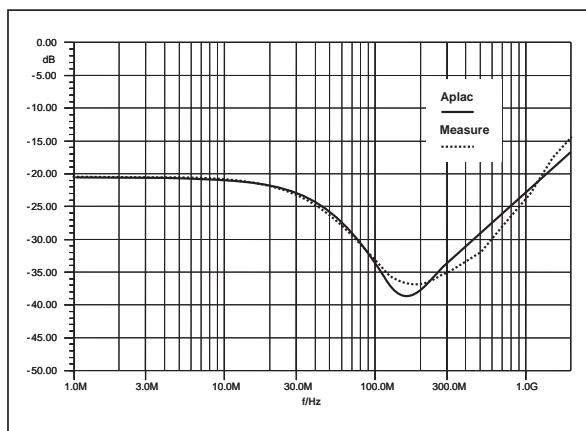


Fig. 2: Analog crosstalk measurements.

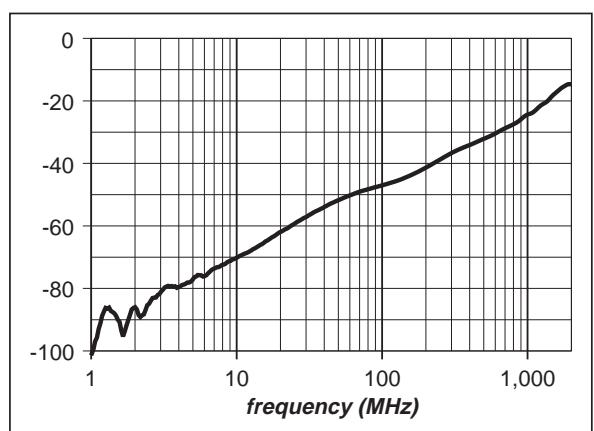


Fig. 3: Digital crosstalk measurement.

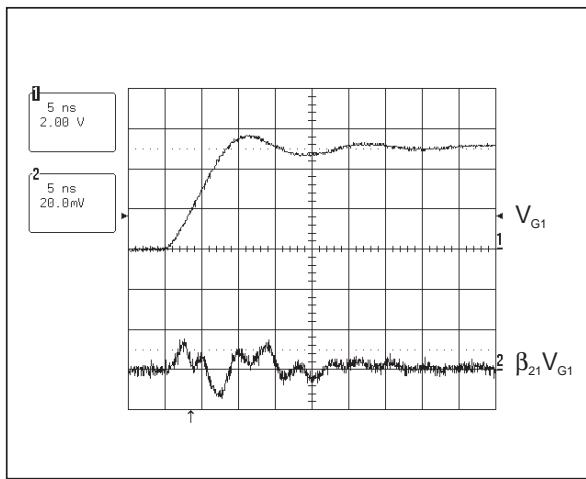


Fig. 4: ESD response to IEC61000-4-2 (+15kV air discharge) on one input V(in) and on one output (Vout).

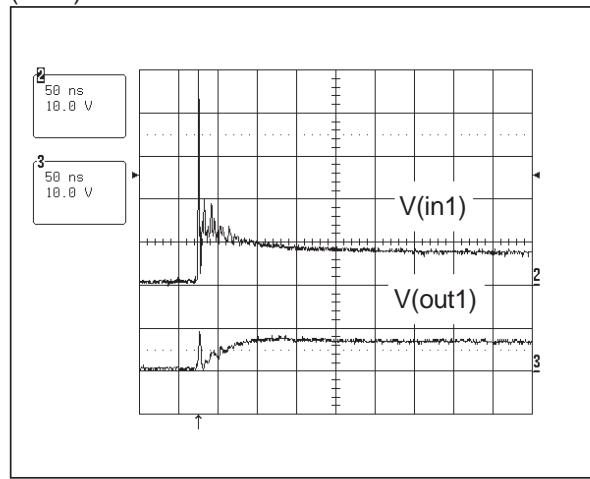


Fig. 5: ESD response to IEC61000-4-2 (+15kV air discharge) on one input V(in) and on one output (Vout).

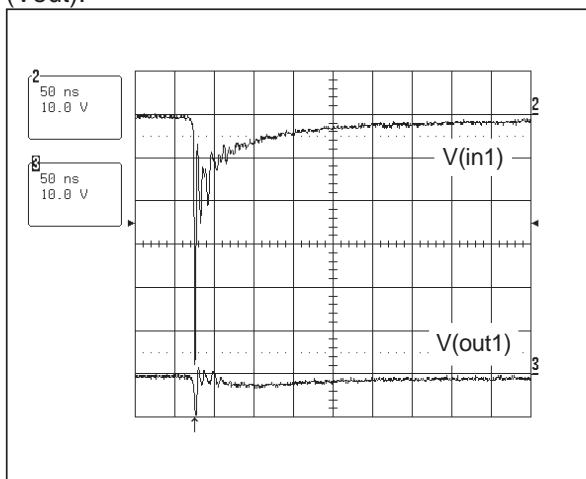
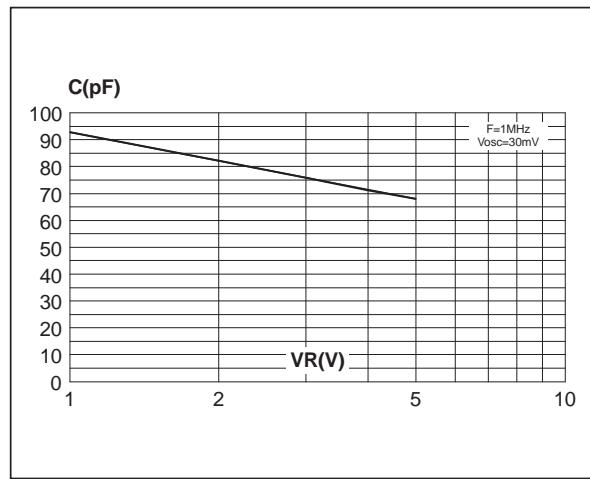


Fig. 6: Line capacitance versus applied voltage.



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Fig. 7: Aplac model single line structure.

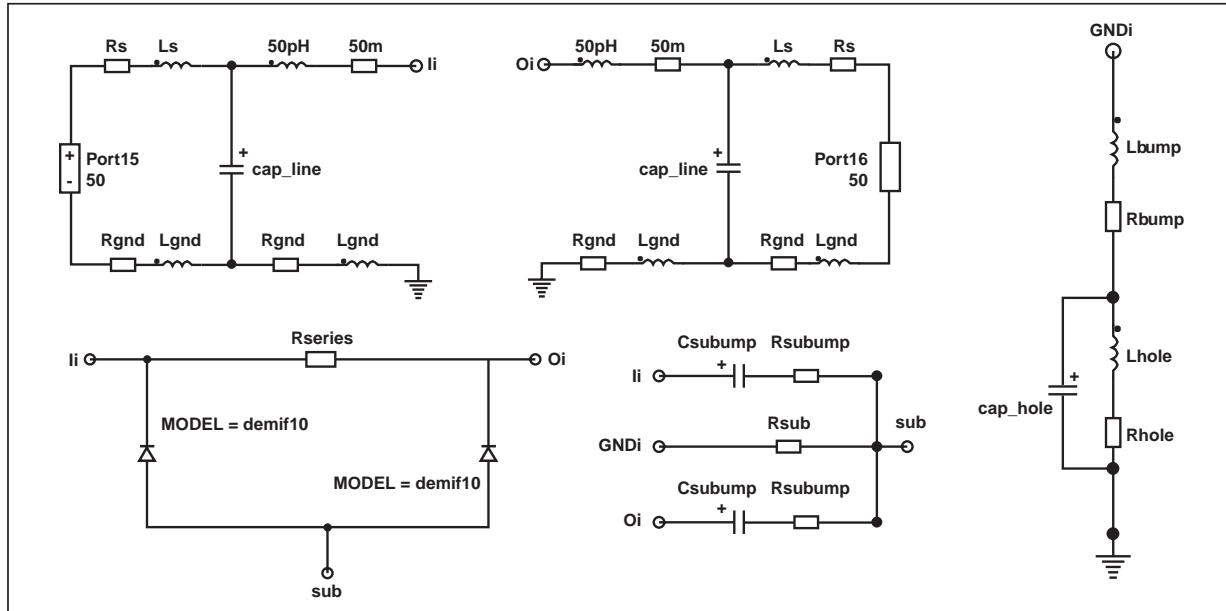
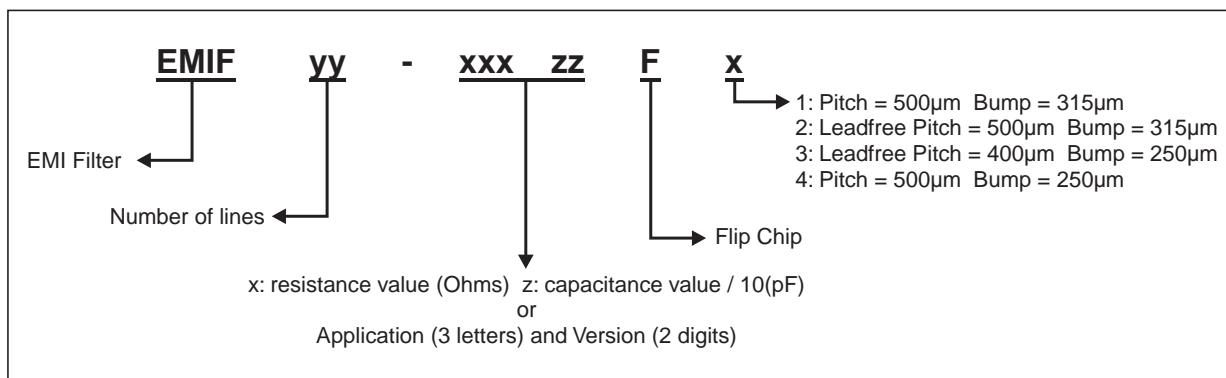


Fig. 8: Aplac model parameters.

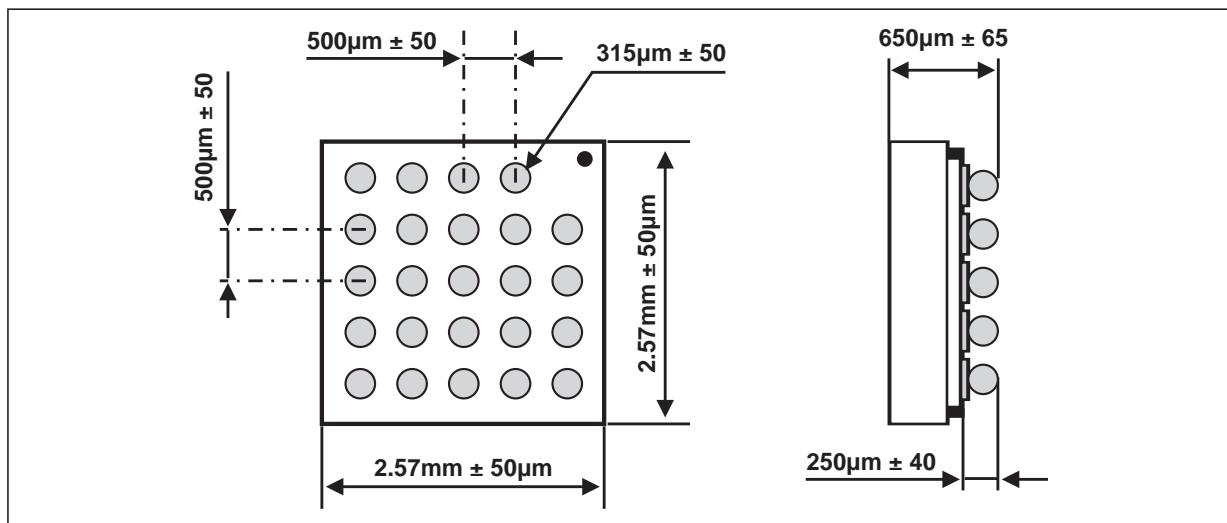
aplacvar	C_z	57pF	Model demif10
aplacvar	R_{series}	960	$BV = 7$
aplacvar	cap_line	0.8pF	$IBV = 1\text{m}$
aplacvar	L_s	0.6nH	$C_{JO} = C_z$
aplacvar	R_{bump}	50m	$M = 0.3333$
aplacvar	L_{bump}	50pH	$R_s = 1$
aplacvar	R_s	0.15	$V_J = 0.6$
aplacvar	C_{subump}	15pF	$TT = 100\text{n}$
aplacvar	R_{subump}	0.15	
aplacvar	R_{sub}	0.1	
aplacvar	I_{hole}	1.2nH opt	
aplacvar	R_{hole}	0.15	
aplacvar	cap_hole	0.15pF	
aplacvar	R_{gnd}	0.25	
aplacvar	I_{gnd}	0.4nH	

ORDER CODE

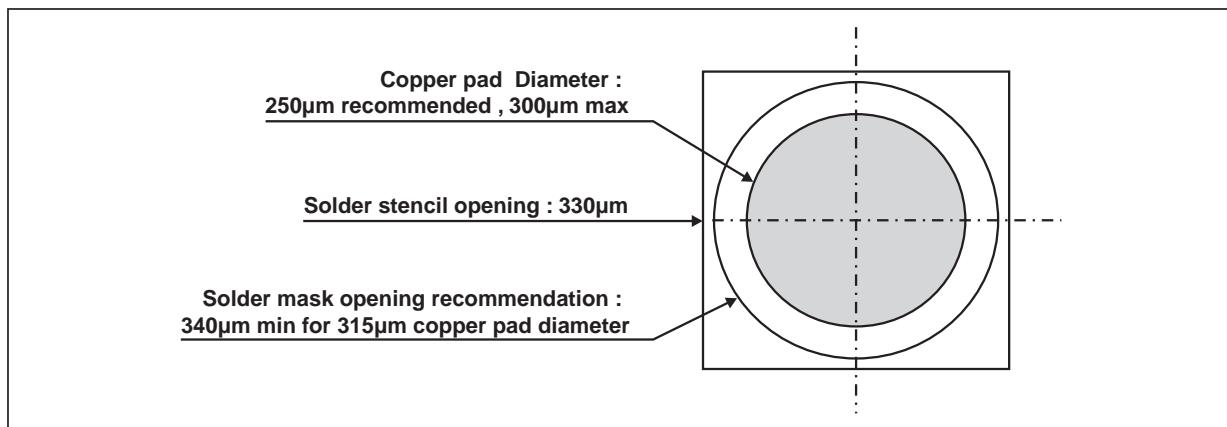


PACKAGE MECHANICAL DATA

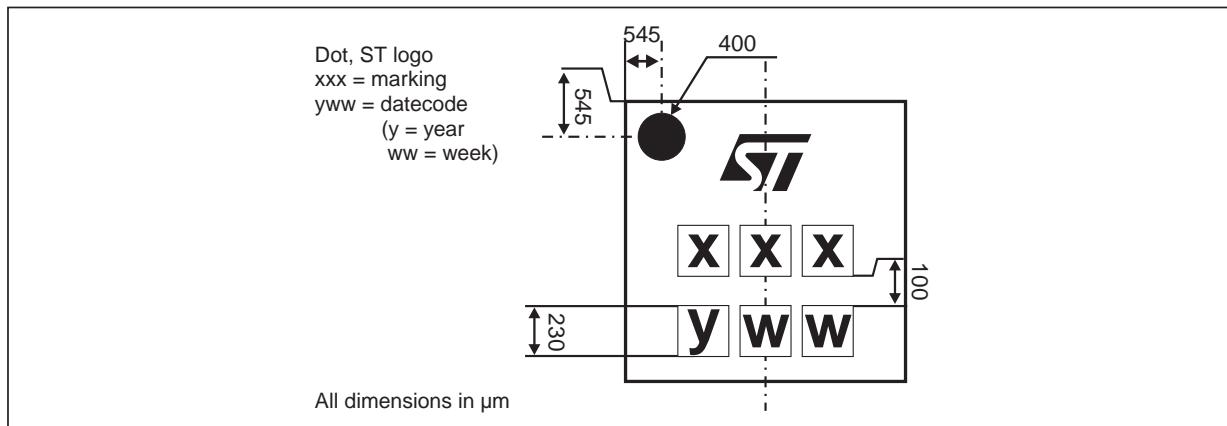
FLIP CHIP



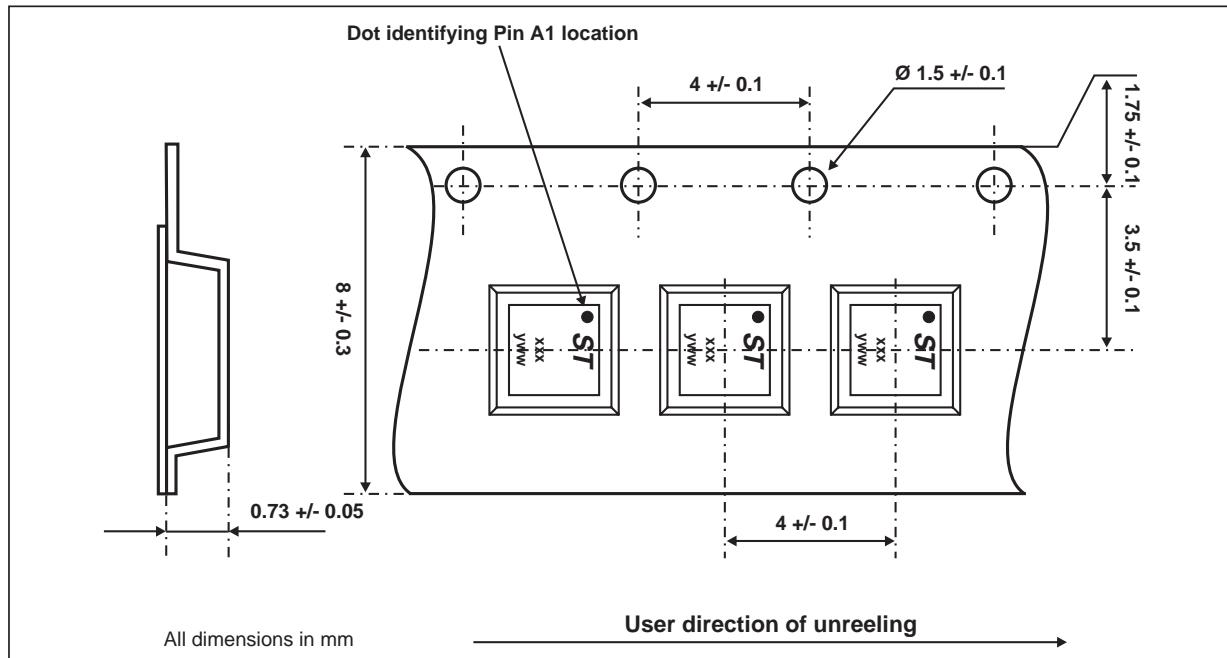
FOOT PRINT RECOMMENDATIONS



MARKING



PACKING



OTHER INFORMATION

Ordering code	Marking	Package	Weight	Base qty	Delivery mode
EMIF10-1K010F1	FDT	Flip Chip	9.2 mg	5000	Tape & reel (7")

Note: More information are available in the application notes:

- AN1235: "Flip-Chip: Package description and recommandations for use"
- AN1751: "EMI Filters: Recommendations and measurements"

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