Data Sheet January 2002

# 19A, 100V, 0.200 Ohm, P-Channel Power MOSFET

This is an advanced power MOSFET designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. It is a P-Channel enhancement mode silicon gate power field effect transistor designed for applications such as switching regulators, switching convertors, motor drivers, relay drivers, and drivers for high power bipolar switching transistors requiring high speed and low gate drive power. These types can be operated directly from integrated circuits.

Formerly developmental type TA17521.

## Ordering Information

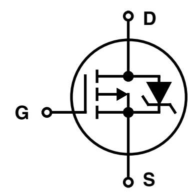
| PART NUMBER | PACKAGE | BRAND |
|---|---|---|
| IRFP9140 | TO-247 | IRFP9140 |

NOTE: When ordering, use the entire part number.

## Features

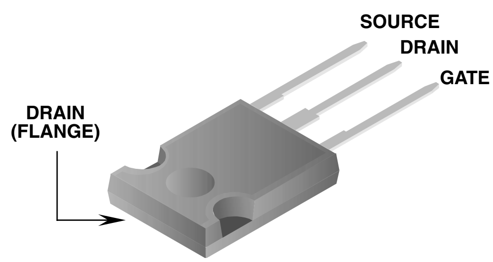
- 19A, 100V
- $r_{DS(ON)} = 0.200\Omega$
- Single Pulse Avalanche Energy Rated
- SOA is Power Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

## Symbol




## Packaging

JEDEC STYLE T0-247



## Absolute Maximum Ratings $T_C = 25^oC$, Unless Otherwise Specified

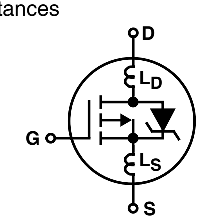
| | | IRFP9140 | UNITS |
|---|---|---|---|
| Drain to Source Voltage (Note 1) | $V_{DS}$ | -100 | V |
| Drain to Gate Voltage ($R_{GS}$ = 20kΩ) (Note 1) | $V_{DGR}$ | -100 | V |
| Continuous Drain Current | $I_D$ | -19 | A |
| $T_C$ =100°C | $I_{DM}$ | -12 | A |
| Pulsed Drain (Note 3) | $I_{DM}$ | -76 | A |
| Gate to Source Voltage | $V_{GS}$ | ±20 | V |
| Maximum Power Dissipation | $P_D$ | 150 | W |
| Linear Derating Factor | | 1.2 | W/°C |
| Single Pulse Avalanche Energy Rating | $E_{as}$ | 960 | mJ |
| Operating and Storage Temperature | $T_J$, $T_{STG}$ | -55 to 150 | °C |
| Maximum Temperature for Soldering | | | |
| Leads at 0.063in (1.6mm) from Case for 10s | $T_L$ | 300 | °C |
| Package Body for 10s, See Techbrief 334 | $T_{pkg}$ | 260 | °C |

*CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

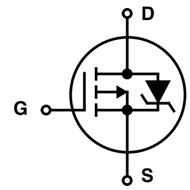
NOTE:

1. $T_J = 25^oC$ to $125^oC$.

## Electrical Specifications $T_C = 25^oC$, Unless Otherwise Specified

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Drain to Source Breakdown Voltage | $BV_{DSS}$ | $V_{GS}$ = 0V, $I_D$ = -250µA, (Figure 10) | -100 | - | - | V |
| Gate Threshold Voltage | $V_{GS(TH)}$ | $V_{DS} = V_{GS}$, $I_D$ = -250µA | -2.0 | - | -4.0 | V |
| Zero Gate Voltage Drain Current | $I_{DSS}$ | $V_{DS}$ = Rated $BV_{DSS}$, $V_{GS}$ = 0V | - | - | 25 | µA |
| | | $V_{DS}$ = 0.8 x Rated $BV_{DSS}$, $V_{GS}$ = 0V, $T_J = 125^oC$ | - | - | 250 | µA |
| On-State Drain Current (Note 2) | $I_{D(ON)}$ | $V_{DS} > I_{D(ON)} \times r_{DS(ON)\,MAX}$, $V_{GS}$ = -10V | -19 | - | - | A |
| Gate to Source Leakage Current | $I_{GSS}$ | $V_{GS}$ = ±20V | - | - | ±100 | nA |
| Drain to Source On Resistance (Note 2) | $r_{DS(ON)}$ | $V_{GS}$ = -10V, $I_D$ = -10A, (Figures 8, 9) | - | 0.14 | 0.20 | Ω |
| Forward Transconductance (Note 2) | $g_{fs}$ | $V_{DS} \le$ -50V, $I_D$ = -10A, (Figure 12) | 5.3 | 7.9 | - | S |
| Turn-On Delay Time | $t_{d(ON)}$ | $V_{DD}$ = -50V, $I_D \approx$ -19A, $R_G$ = 9.1Ω, $R_L$ = 2.5Ω, $V_{GS}$ = -10V, (Figures 17, 18) MOSFET Switching Times Are Essentially Independent of Operating Temperature | - | 16 | 20 | ns |
| Rise Time | $t_r$ | | - | 65 | 100 | ns |
| Turn-Off Delay Time | $t_{d(OFF)}$ | | - | 47 | 70 | ns |
| Fall Time | $t_f$ | | - | 28 | 70 | ns |
| Total Gate Charge (Gate to Source + Gate to Drain) | $Q_{g(TOT)}$ | $V_{GS}$ = -10V, $I_D$ = -19A, $V_{DS}$ = 0.8 x Rated $BV_{DSS}$, $I_{G(REF)}$ = -1.5mA (Figures 14, 19, 20) Gate Charge is Essentially Independent of Operating Temperature | - | 37 | 55 | nC |
| Gate to Source Charge | $Q_{gs}$ | | - | 8.7 | - | nC |
| Gate to Drain "Miller" Charge | $Q_{gd}$ | | - | 22 | - | nC |
| Input Capacitance | $C_{ISS}$ | $V_{GS}$ = 0V, $V_{DS}$ = -25V, f = 1.0MHz, (Figure 11) | - | 1200 | - | pF |
| Output Capacitance | $C_{OSS}$ | | - | 570 | - | pF |
| Reverse Transfer Capacitance | $C_{RSS}$ | | - | 160 | - | pF |
| Internal Drain Inductance | $L_D$ | Measured Between Contact Screw on Header That Is Closer to Source and Gate Pins and Center of Die; Modified MOSFET Symbol Showing the Internal Device Inductances   | - | 5.0 | - | nH |
| Internal Source Inductance | $L_S$ | Measured From the Source Pin, 6mm (0.25in) From Header and Source Bonding Pad | - | 13 | - | nH |
| Junction to Case | $R_{\theta JC}$ | | - | - | 0.83 | °C/W |
| Junction to Ambient | $R_{\theta JA}$ | Free Air Operation | - | - | 30 | °C/W |

## Source to Drain Diode Specifications

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Continuous Source to Drain Current | $I_{SD}$ | Modified MOSFET Symbol Showing the Integral Reverse P-N Junction Diode   | - | - | -19 | A |
| Pulse Source to Drain Current (Note 3) | $I_{SDM}$ | | - | - | -76 | A |
| Source to Drain Diode Voltage (Note 2) | $V_{SD}$ | $T_J = 25^oC$, $I_{SD}$ = -19A, $V_{GS}$ = 0V, (Figure 13) | - | - | -1.5 | V |
| Reverse Recovery Time | $t_{rr}$ | $T_J = 25^oC$, $I_{SD}$ = -18A, $dI_{SD}/dt$ = 100A/μs | - | 210 | - | ns |
| Reverse Recovery Charge | $Q_{RR}$ | $T_J = 25^oC$, $I_{SD}$ = -18A, $dI_{SD}/dt$ = 100A/μs | - | 2.0 | - | μC |

NOTES:

2. Pulse test: pulse width ≤ 80μs, duty cycle ≤ 2%.
3. Repetitive rating: pulse width limited by Maximum junction temperature. See Transient Thermal Impedance curve (Figure 3).
4. $V_{DD}$ = 50V, start $T_J = 25^oC$, L = 4.2mH, $R_G = 25\Omega$, peak $I_{AS}$ = 19A. See Figures 15, 16.

## *Typical Performance Curves* Unless Otherwise Specified

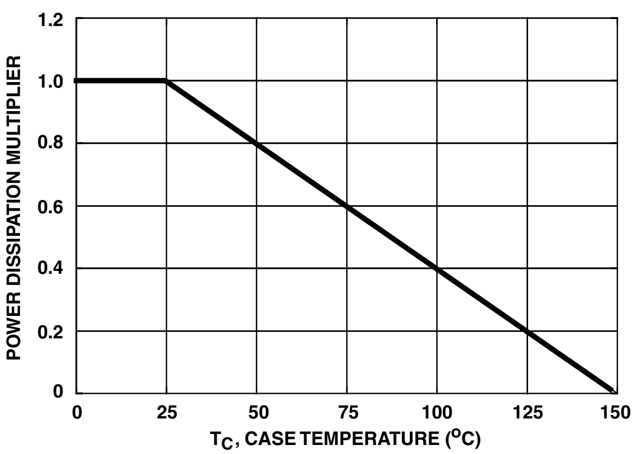



FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE

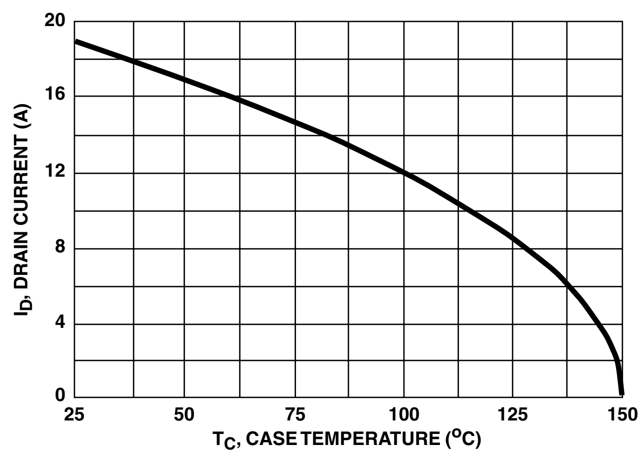



FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE

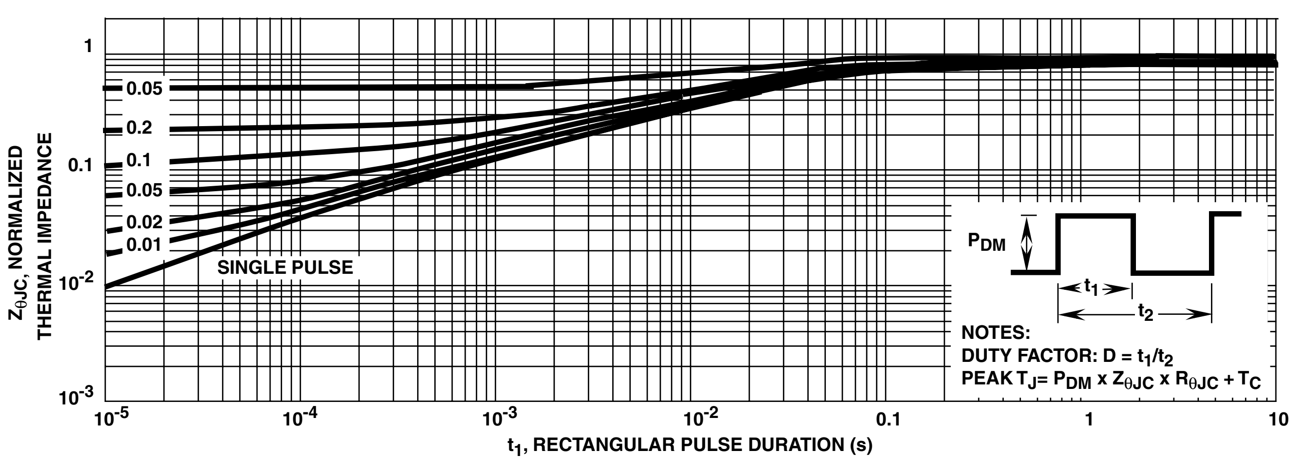



FIGURE 3. NORMALIZED TRANSIENT THERMAL IMPEDANCE

## *Typical Performance Curves* Unless Otherwise Specified **(Continued)**

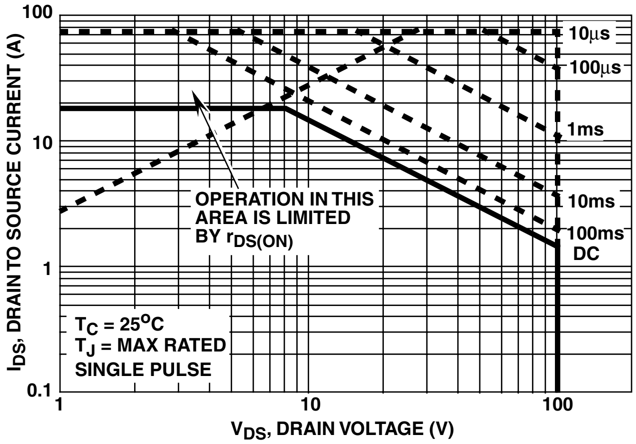



**FIGURE 4. FORWARD BIAS SAFE OPERATING AREA**

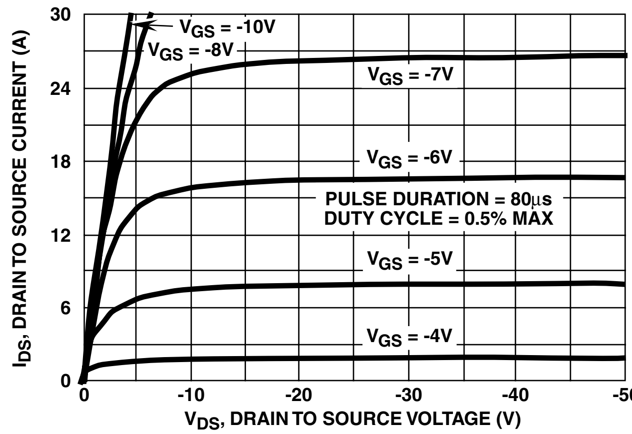



**FIGURE 5. OUTPUT CHARACTERISTICS**

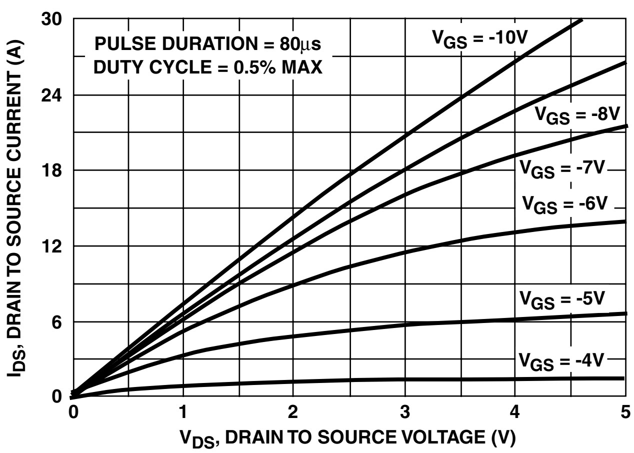



**FIGURE 6. SATURATION CHARACTERISTICS**

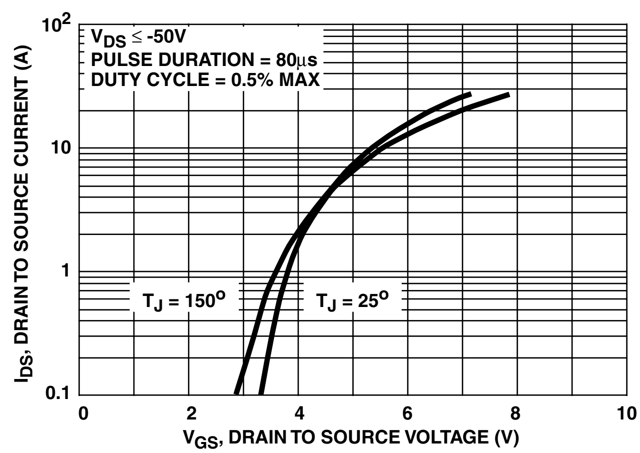



**FIGURE 7. TRANSFER CHARACTERISTICS**

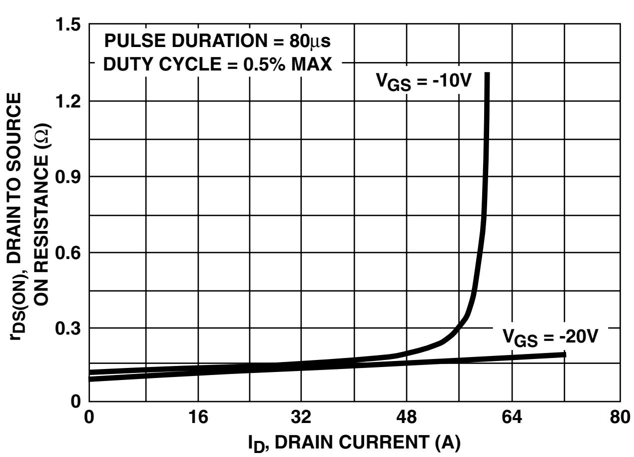



**FIGURE 8. DRAIN TO SOURCE ON RESISTANCE vs GATE VOLTAGE AND DRAIN CURRENT**

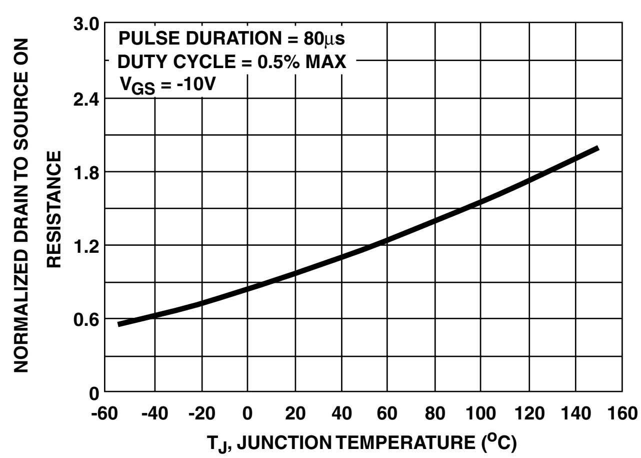



**FIGURE 9. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE**

## *Typical Performance Curves* Unless Otherwise Specified **(Continued)**

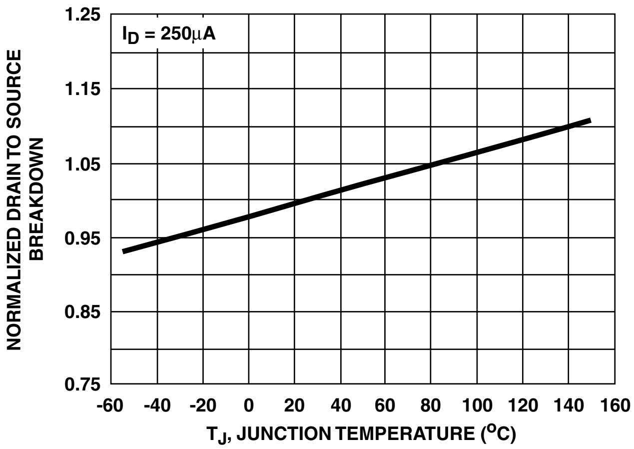



**FIGURE 10. NORMALIZED DRAIN TO SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE**

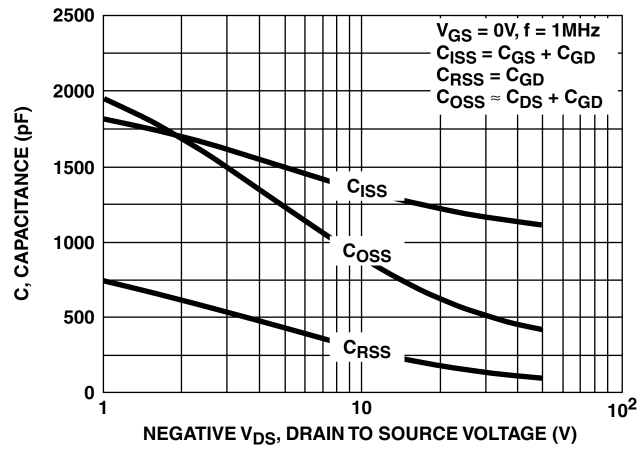



**FIGURE 11. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE**

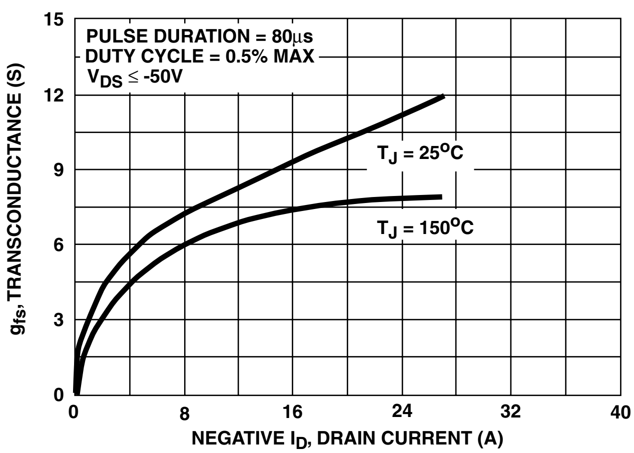



**FIGURE 12. TRANSCONDUCTANCE vs DRAIN CURRENT**

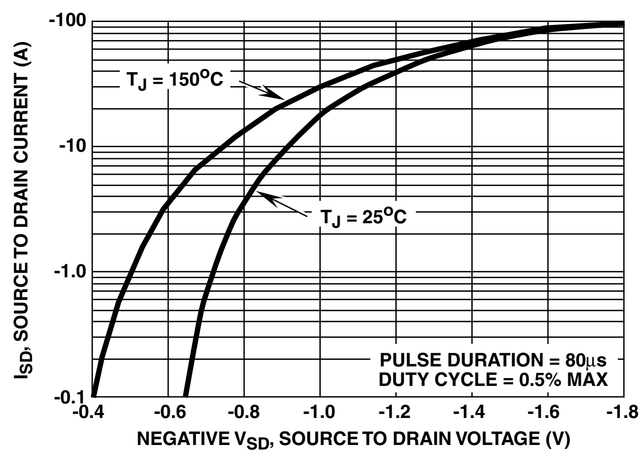



**FIGURE 13. SOURCE TO DRAIN DIODE VOLTAGE**

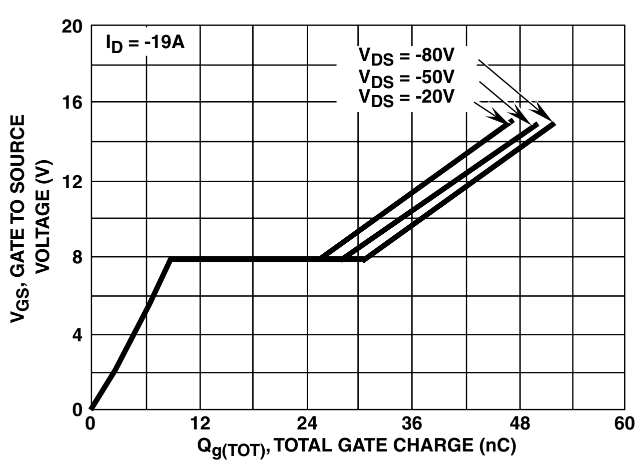



**FIGURE 14. GATE TO SOURCE VOLTAGE vs GATE CHARGE**

## *Test Circuits and Waveforms*

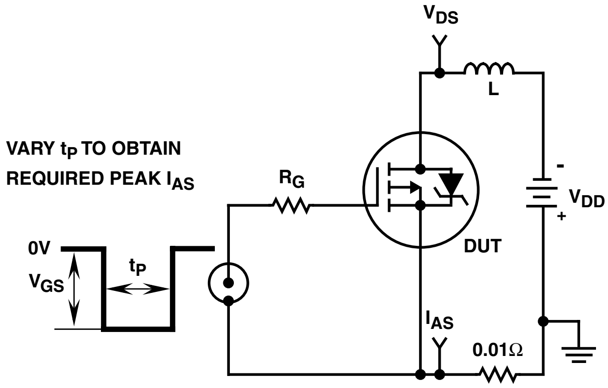



**FIGURE 15. UNCLAMPED ENERGY TEST CIRCUIT**

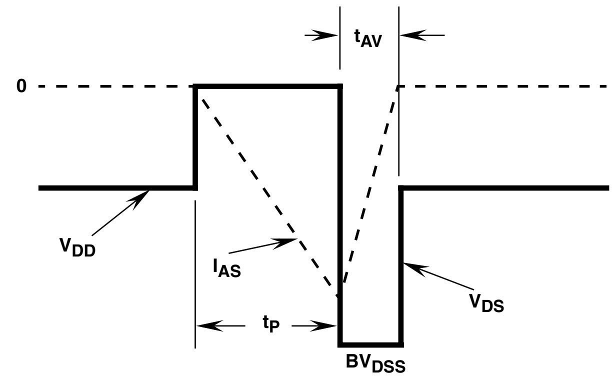



**FIGURE 16. UNCLAMPED ENERGY WAVEFORMS**

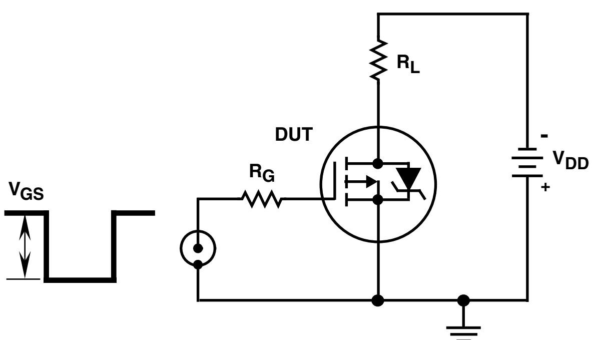



**FIGURE 17. SWITCHING TIME TEST CIRCUIT**

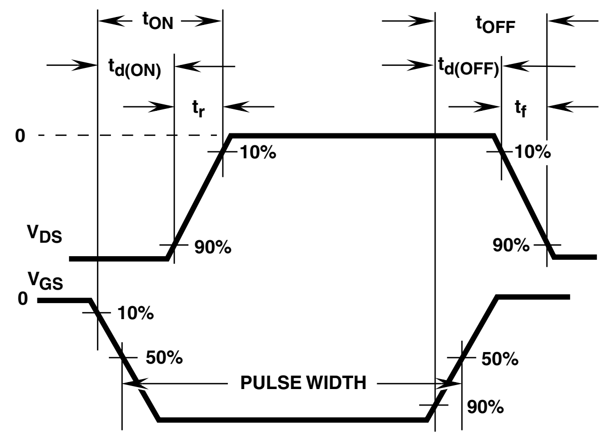



**FIGURE 18. RESISTIVE SWITCHING WAVEFORMS**

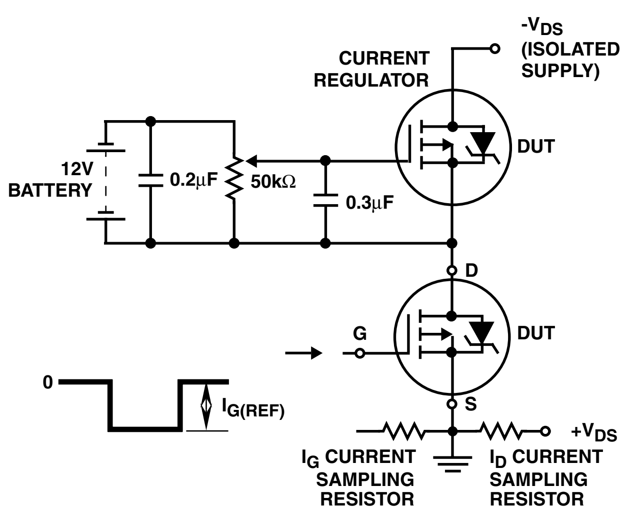



**FIGURE 19. GATE CHARGE TEST CIRCUIT**

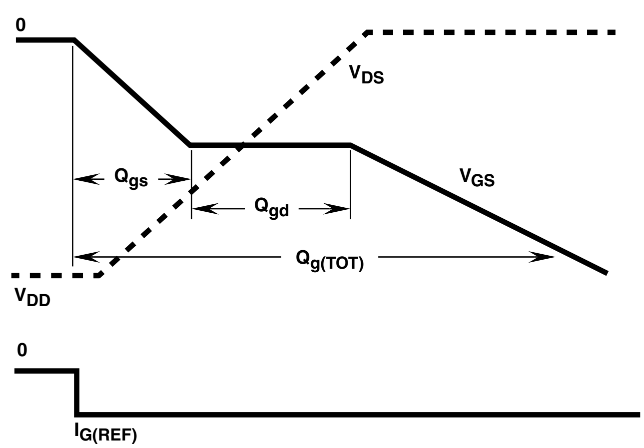



**FIGURE 20. GATE CHARGE WAVEFORMS**

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