Recent Additions
## CD54AC652/3A
CD54ACT652/3A

T-52-31

Octal-Bus Transceiver/Register, 3-State
Non-Inverting

The RCA CD54AC652 and CD54ACT652 are 3-state-octal-bus transceivers/registers that utilize the new RCA ADVANCED CMOS LOGIC technology. The CD54AC652 and CD54ACT652 have non-inverting outputs. These devices consist of bus transceiver circuits, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers. Output Enables OE$_{AB}$ and $\overline{OE}_{BA}$ are provided to control the transceiver functions. SAB and SBA control pins are provided to select whether real-time or stored data is transferred. The circuitry used for select control will eliminate the typical decoding glitch that occurs in a multiplexer during the transition between stored and real-time data. A LOW input level selects real-time data, and a HIGH selects stored data. The following examples demonstrate the four fundamental bus-management functions that can be performed with the octal-bus transceivers and registers.
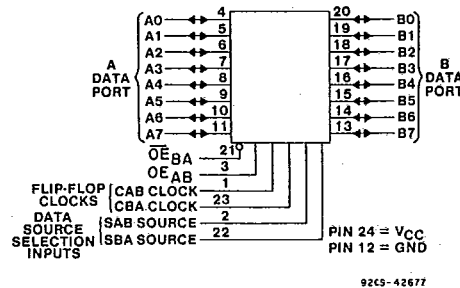
Data on the A or B data bus, or both, can be stored in the internal D flip-flops by low-to-high transitions at the appropriate clock pins (CAB or CBA) regardless of the select or enable control pins. When SAB and SBA are in the real-time transfer mode, it is also possible to store data without using the internal D-type flip-flops by simultaneously enabling OE$_{AB}$ and $\overline{OE}_{BA}$. In this configuration, each output reinforces its input. Thus, when all other data sources to the two sets of bus lines are at high impedance, each set of bus lines will remain at its last state.

The CD54AC652 and CD54ACT652 are supplied in 24-lead dual-in-line ceramic packages (F suffix).

92CS-42677

FUNCTIONAL DIAGRAM

Package Specifications
(See Section 11, Fig. 13)

Static Electrical Characteristics (Limits with black dots (•) are tested 100%.)

CHARACTERISTICS	TEST CONDITIONS		V$_{CC}$ (V)	AMBIENT TEMPERATURE (T$_A$) - °C				UNITS
				+25		–55 to +125		
	V$_I$ (V)	I$_O$ (mA)		MIN.	MAX.	MIN.	MAX.	
Quiescent Supply Current (MSI) I$_{CC}$	V$_{CC}$ or GND	0	5.5	—	8•	—	160•	μA

The complete static electrical test specification consists of the above by-type static tests combined with the standard static tests in the beginning of this section.

ACT INPUT LOADING TABLE

INPUT	UNIT LOAD*
CAB, CBA	1.25
SAB, SBA	1.2
OE$_{AB}$	0.67
$\overline{OE}_{BA}$	1.17
An, Bn	0.4

*Unit load is ΔI$_{CC}$ limit specified in Static Characteristics Chart, e.g., 2.4 mA max. @ 25°C.

HARRIS SEMICOND SECTOR   37E D ■■ 4302271 0026200 0 ■■HAS

High-Reliability Advanced CMOS Logic ICs

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SWITCHING CHARACTERISTICS: AC Series; t_r, t_f = 3 ns, C_L = 50 pF (Worst Case)

CHARACTERISTICS	SYMBOL	V_{CC} (V)	-55 to +125°C		UNITS
			MIN.	MAX.	
Propagation Delays: Store A Data to B Bus Store B Data to A Bus	t_{PLH} t_{PHL}	1.5 3.3* 5†	— 4 2.7	194 21.7 15.5•	ns
A Data to B Bus B Data to A Bus	t_{PLH} t_{PHL}	1.5 3.3 5	— 3.7 2.4	178 19.9 14.2•	ns
Select to Data	t_{PLH} t_{PHL}	1.5 3.3 5	— 4 2.7	194 21.7 15.5•	ns
3-State Enabling/Disabling Time Bus to Output or Register to Output	t_{PZL} t_{PZH} t_{PLZ} t_{PHZ}	1.5 3.3 5	— 4 2.7	194 23.3 15.5•	ns
Power Dissipation Capacitance	C_{PD}§	—			pF
Min. (Valley) V_{OH} During Switching of Other Outputs (Output Under Test Not Switching)	V_{OHV}	5	4 Typ. @ 25°C		V
Max. (Peak) V_{OL} During Switching of Other Outputs (Output Under Test Not Switching)	V_{OLP}	5	4 Typ. @ 25°C		V
Input Capacitance	C_I	—	—	10	pF
3-State Output Capacitance	C_O	—	—	15	pF

SWITCHING CHARACTERISTICS: ACT Series; t_r, t_f = 3 ns, C_L = 50 pF (Worst Case)

CHARACTERISTICS	SYMBOL	V_{CC} (V)	-55 to +125°C		UNITS
			MIN.	MAX.	
Propagation Delays: Store A Data to B Bus Store B Data to A Bus	t_{PLH} t_{PHL}	5†	2.7	15.5•	ns
A Data to B Bus B Data to A Bus	t_{PLH} t_{PHL}	5	2.4	14.2•	ns
Select to Data	t_{PLH} t_{PHL}	5	2.7	15.5•	ns
3-State Enabling/Disabling Time Bus to Output or Register to Output	t_{PZL} t_{PZH} t_{PLZ} t_{PHZ}	5	2.7	15.5•	ns
Power Dissipation Capacitance	C_{PD}§	—			pF
Min. (Valley) V_{OH} During Switching of Outher Outputs (Output Under Test Not Switching)	V_{OHV}	5	4 Typ. @ 25°C		V
Max. (Peak) V_{OL} During Switching of Other Outputs (Output Under Test Not Switching)	V_{OLP}	5	1 Typ. @ 25°C		V
Input Capacitance	C_I	—	—	10	pF
3-State Output Capacitance	C_O	—	—	15	pF

*3.3 V: min. is @ 3.6 V
      max. is @ 3 V

†5 V: min. is @ 5.5 V
      max. is @ 4.5 V

(Limits with black dots (•) are tested 100%.)

§C_{PD} is used to determine the dynamic power consumption, per package.
For AC, $P_D = C_{PD}V_{CC}^2 f_i + \Sigma (C_L V_{CC}^2 f_o)$
For ACT, $P_D = V_{CC}^2 C_{PD} f_i + \Sigma V_{CC}^2 C_L f_o + V_{CC} \Delta I_{CC}$ where f_i = input frequency
f_o = output frequency
C_L = output load capacitance
V_{CC} = supply voltage

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