SONY

CXP921F064A

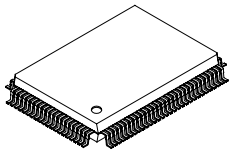
CMOS 16-bit Single Chip Microcomputer

Description

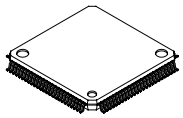
The CXP921F064A is a CMOS 16-bit microcomputer integrating on a single chip an A/D converter, serial interface, I^2C bus interface, timer, clock prescaler, remote control receive circuit, and as well as basic configurations like a 16-bit CPU, ROM, RAM, and I/O port.

This LSI also provides the sleep/stop functions that enable lower power consumption.

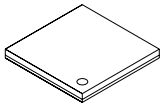
100 pin QFP (Plastic)



100 pin LQFP (Plastic)



104 pin LFLGA (Plastic)



Features

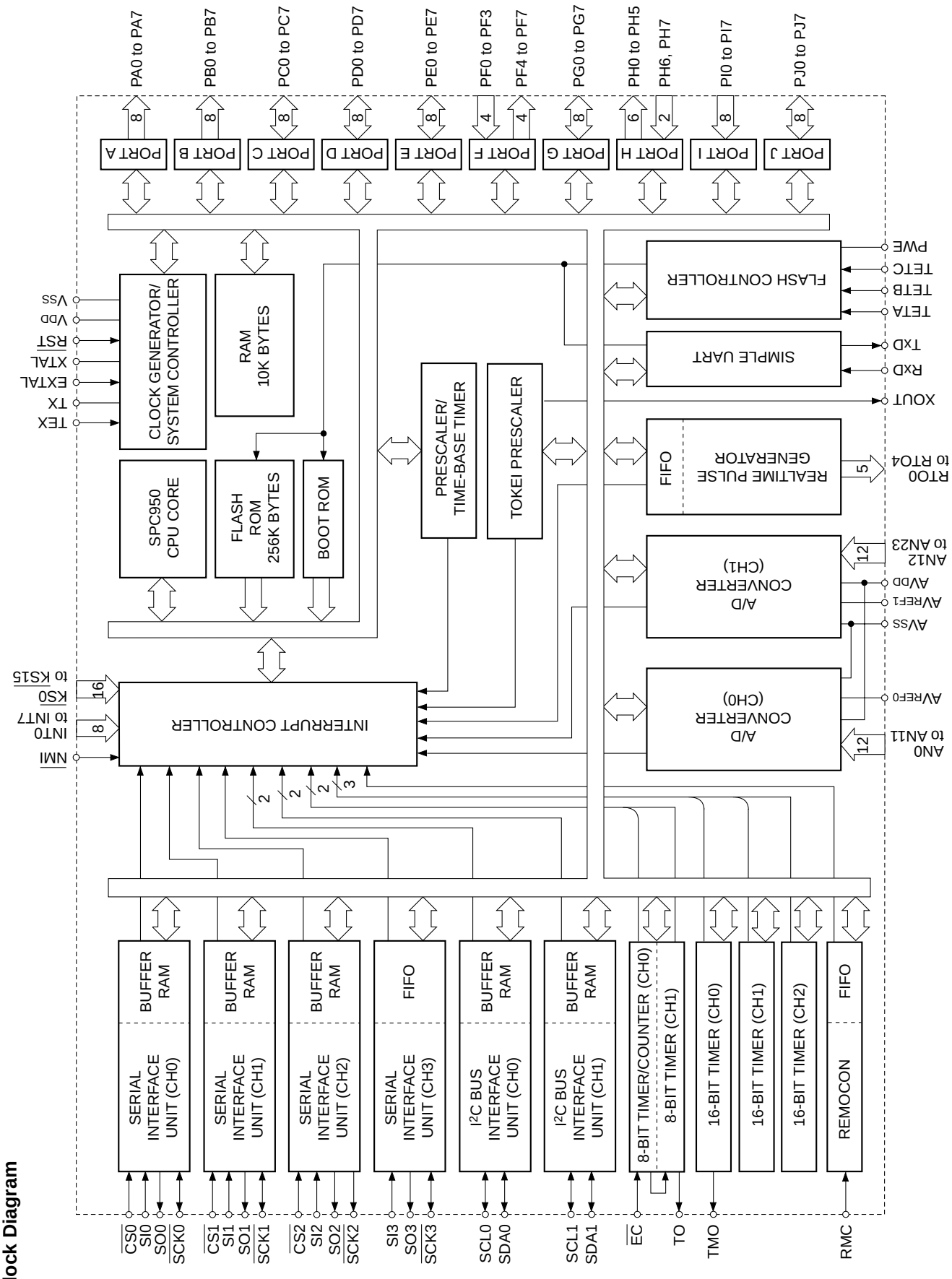
- An efficient instruction set as a controller
  - — Direct addressing, numerous abbreviated forms, multiplication and division instructions
- Instruction sets for C language and RTOS
  - — Highly quadratic instruction system, general-purpose register of 16-bit × 8-pin × 16-bank configuration
- Minimum instruction cycle 100ns at 20MHz operation (2.7 to 3.3V)
  61µs at 32kHz operation (2.2 to 3.3V)
- Incorporated Flash ROM capacity 256K bytes
- Incorporated RAM capacity 10K bytes
- Peripheral functions
  - — A/D converter 8-bit 12 analog input, 2 channels, successive approximation system, automatic scanning function, (Conversion time: 3.4µs at 20MHz)
  - — Serial interface 128-byte buffer RAM, 3 channels
    8-stage FIFO, 1 channel (supports special mode master/slave)
  - — I^2C bus interface 64-byte buffer RAM , 2 channels
    (supports master/slave and automatic transfer mode)
  - — Timers 8-bit timer/counter, 2 channels (with timing output)
    16-bit timer, 3 channels
  - — Real-time pulse generator 5-bit output, 1 channel (2-stage FIFO)
  - — Clock prescaler
  - — Remote control receive circuit 8-bit pulse measurement counter, 8-stage FIFO
- Interruption 30 factors, 30 vectors, multi-interruption and priority selection possible
- Standby mode Sleep/stop
- Package 100-pin plastic QFP/LQFP
  104-pin plastic LFLGA
- Mask ROM CXP921064A
- Piggy/evaluation chip CXP921000A

Structure

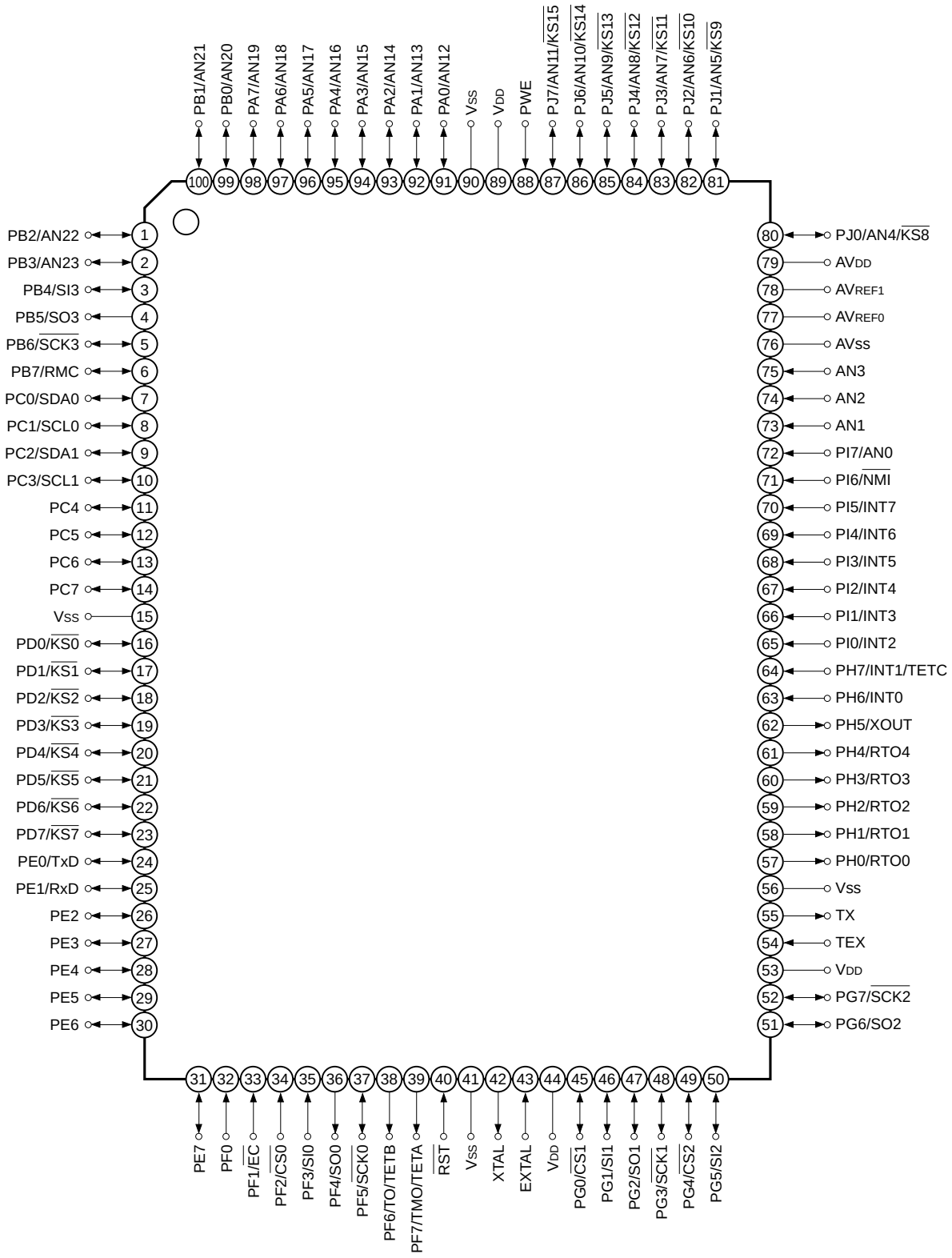
Silicon gate CMOS IC

E00250A18-PS

Block Diagram

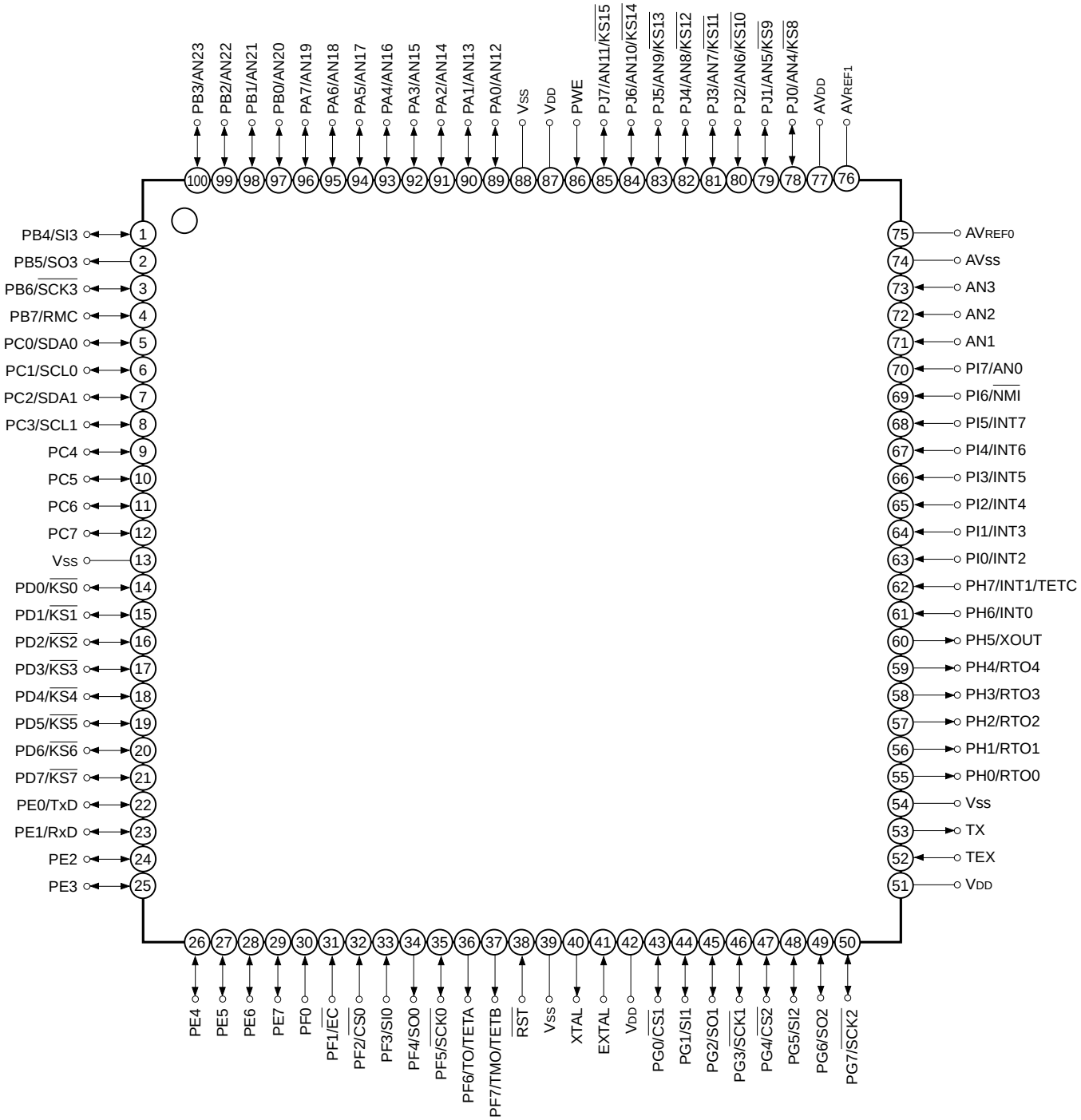


Pin Assignment 1 (Top View) 100-pin QFP package



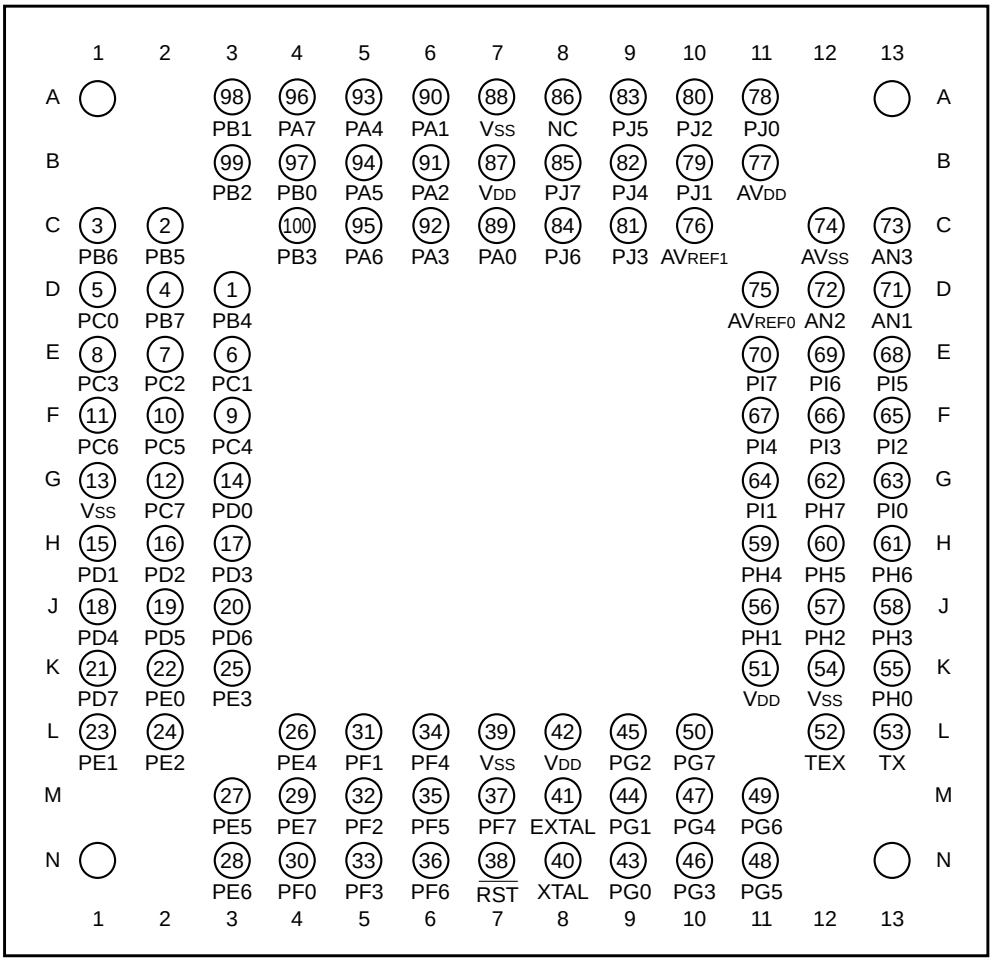
Note) 1. Vss (Pins 15, 41, 56 and 90) must be connected to GND.
2. VDD (Pins 44, 53 and 89) must be connected to VDD.

Pin Assignment 2 (Top View) 100-pin LQFP package



Note) 1. Vss (Pins 13, 39, 54 and 88) must be connected to GND.
2. VDD (Pins 42, 51 and 87) must be connected to VDD.

Pin Assignment 3 (Top View) 104-pin LFLGA package



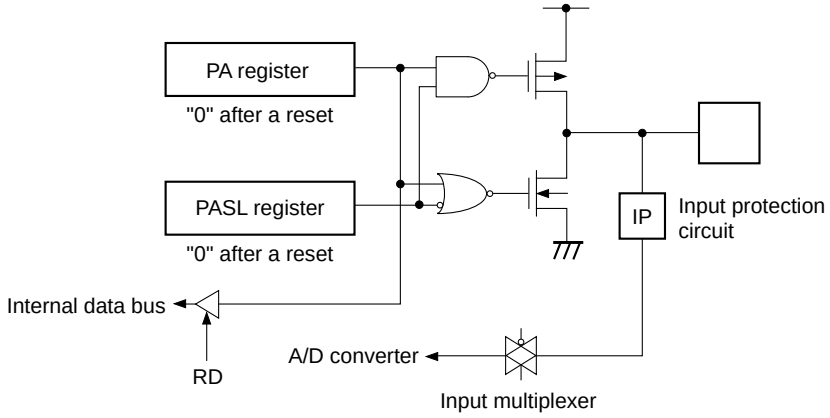
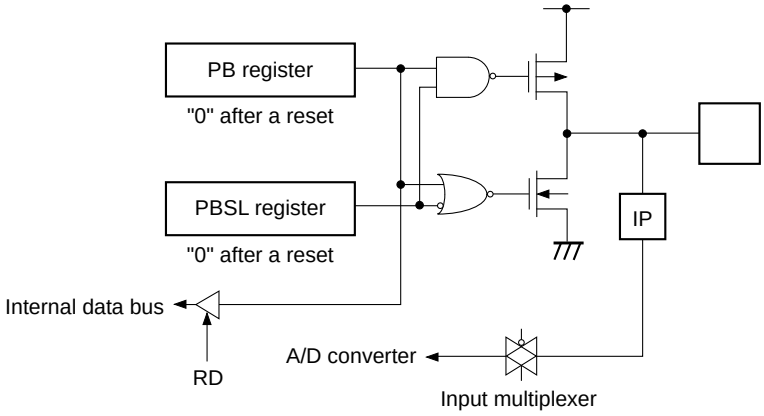
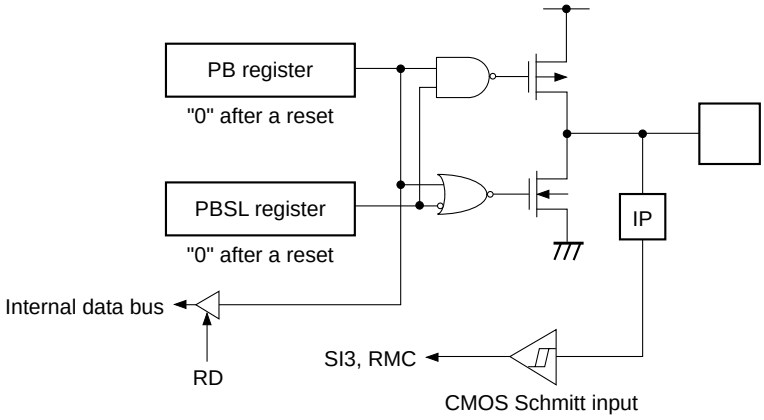
Note) 1. Vss (Pins 13, 39, 54 and 88) must be connected to GND.
2. V_{DD} (Pins 42, 51 and 87) must be connected to V_{DD}.
3. Pin Nos. 1 to 100 are the same Pin Nos. of LQFP. For details, see page 4.

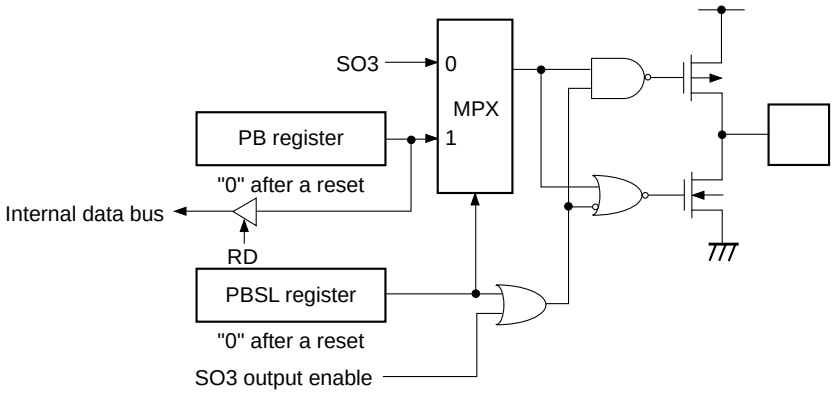
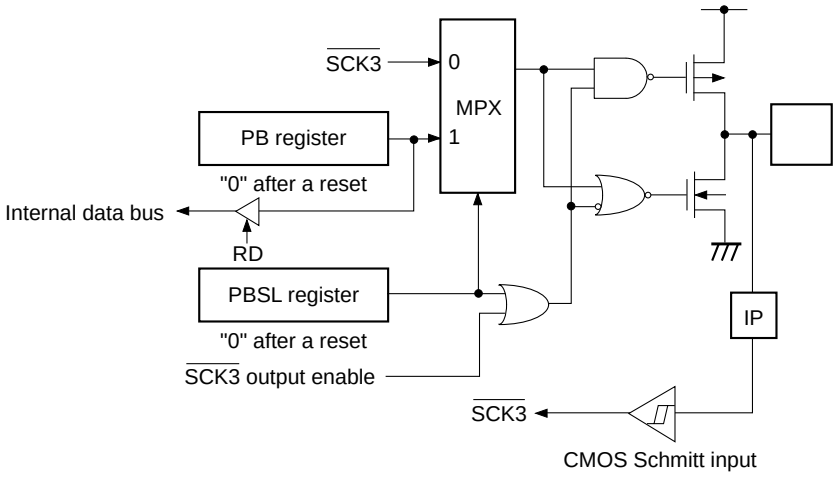
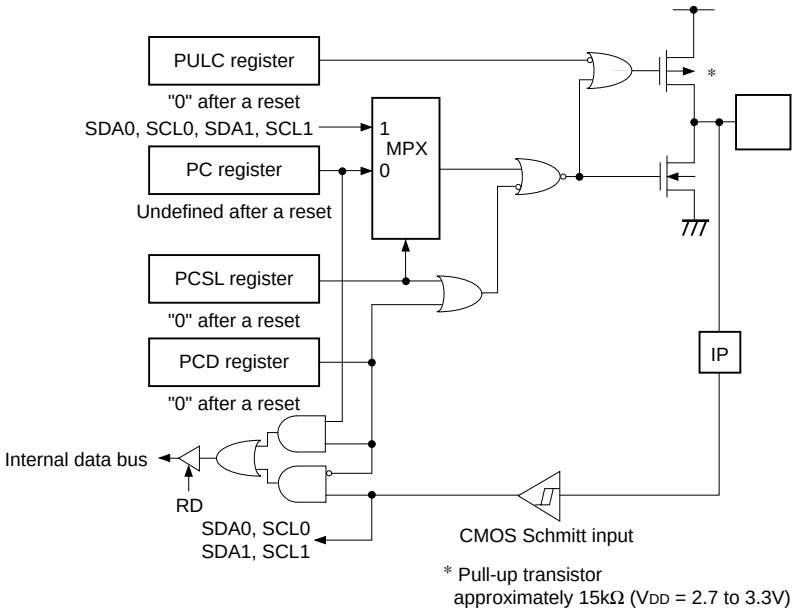
Pin Functions

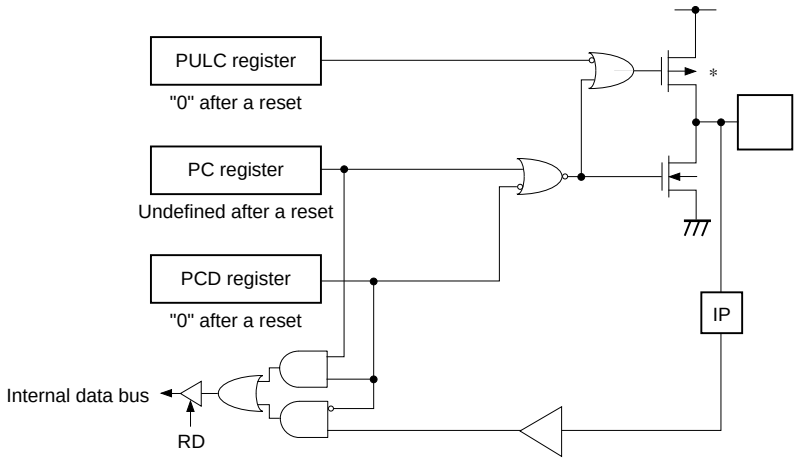
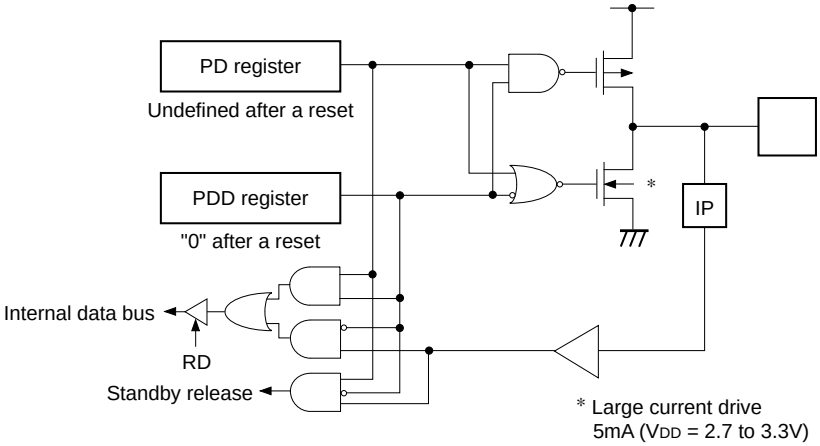
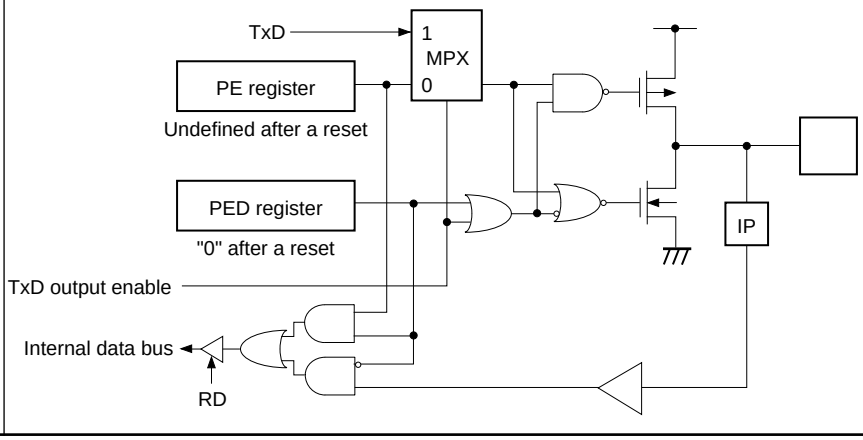
Symbol	I/O	Functions		
PA0/AN12 to PA7/AN19	Output / Input	(Port A) 8-bit output port. (8 pins)		Analog input for A/D converter. (12 pins)
PB0/AN20 to PB3/AN23	Output / Input	(Port B) 8-bit output port. (8 pins)		
PB4/SI3	Output / Input			Serial data (CH3) input.
PB5/SO3	Output / Output			Serial data (CH3) output.
PB6/$\overline{\text{SCK3}}$	Output / I/O			Serial clock (CH3) I/O.
PB7/RMC	Output / Input			Remote control receive circuit input.
PC0/SDA0	I/O / I/O	(Port C) 8-bit I/O port. I/O can be specified in 1-bit units. Pull-up resistor is present or not through program in 1-bit units. (8 pins)		Data I/O of I^2C bus interface (CH0).
PC1/SCL0	I/O / I/O			Clock I/O of I^2C bus interface (CH0).
PC2/SDA1	I/O / I/O			Data I/O of I^2C bus interface (CH1).
PC3/SCL1	I/O / I/O			Clock I/O of I^2C bus interface (CH1).
PC4 to PC7	I/O			
PD0/$\overline{\text{KS0}}$ to PD7/$\overline{\text{KS7}}$	I/O / Input	(Port D) 8-bit I/O port. I/O can be specified in 1-bit units. Can drive 5mA sink current (V_{DD} = 2.7 to 3.3V). (8 pins)		Standby release input function can be specified in 1-bit units. (8 pins)
PE0/TxD	I/O / Output	(Port E) 8-bit I/O port. I/O can be specified in 1-bit units. (8 pins)		Serial (asynchronous communication) during flash on-board write.
PE1/RxD	I/O / Input			
PE2 to PE7	I/O			
PF0	Input	(Port F) 8-bit port. Lower 4 bits are for input; upper 4 bits are for output. (8 pins)		
PF1/$\overline{\text{EC}}$	Input / Input			External event input for 8-bit timer/counter.
PF2/$\overline{\text{CS0}}$	Input / Input			Serial chip select (CH0) input.
PF3/SI0	Input / Input			Serial data (CH0) input.
PF4/SO0	Output / Output			Serial data (CH0) output.
PF5/$\overline{\text{SCK0}}$	Output / I/O			Serial clock (CH0) I/O.
PF6/TO/TETB	Output / Output		Flash mode setting pins	8-bit timer/counter output.
PF7/TMO/TETA	Output / Output			16-bit timer (CH0) output.

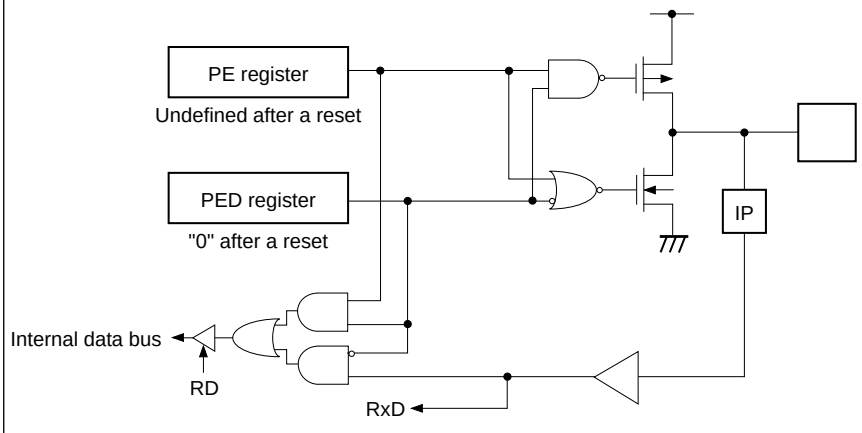
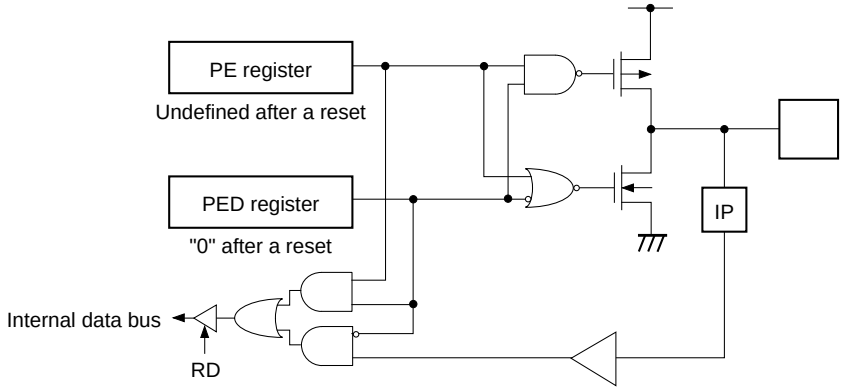
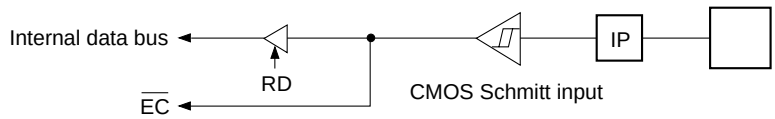
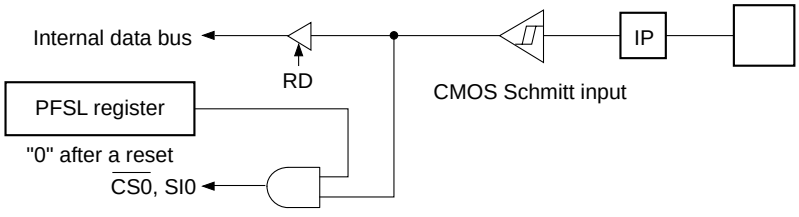
Symbol	I/O	Functions	
PG0/$\overline{CS1}$	I/O / Input	(Port G) 8-bit I/O port. I/O can be specified in 1-bit units. (8 pins)	Serial chip select (CH1) input.
PG1/SI1	I/O / Input		Serial data (CH1) input.
PG2/SO1	I/O / Output		Serial data (CH1) output.
PG3/$\overline{SCK1}$	I/O / I/O		Serial clock (CH1) I/O.
PG4/$\overline{CS2}$	I/O / Input		Serial chip select (CH2) input.
PG5/SI2	I/O / Input		Serial data (CH2) input.
PG6/SO2	I/O / Output		Serial data (CH2) output.
PG7/$\overline{SCK2}$	I/O / Output		Serial clock (CH2) output.
PH0/RTO0 to PH4/RTO4	Output / Output	(Port H) 8-bit port. Lower 6 bits are for output; upper 2 bits are for input. (8 pins)	Real-time pulse generator output. (5 pins)
PH5/XOUT	Output / Output		Clock output for clock prescaler buzzer.
PH6/INT0	Input / Input		External interrupt input. (8 pins)
PH7/INT1/ TETC	Input / Input / Input	Flash mode setting pins	
PI0/INT2 to PI5/INT7	Input / Input	(Port I) 8-bit input port. (8 pins)	
PI6/$\overline{NMI}$	Input / Input		Non-maskable external interrupt input.
PI7/AN0	Input / Input		
AN1 to AN3	Input	Analog input for A/D converter. (12 pins)	
PJ0/AN4/ $\overline{KS8}$ to PJ7/AN11/ $\overline{KS15}$	I/O / Input / Input	(Port J) 8-bit I/O port. I/O can be specified in 1-bit units. (8 pins)	Standby release input function can be specified in 1-bit units. (8 pins)
EXTAL	Input	Connects a crystal for main clock oscillation. (When the clock is supplied externally, input it to EXTAL and input an opposite phase clock to XTAL.)	
XTAL			
TEX	Input	Connects a crystal for sub clock oscillation. (When the clock is supplied externally, input it to TEX and input an opposite phase clock to TX.)	
TX			
$\overline{RST}$	Input	System reset. Active at "L" level.	
AV_{DD}		Positive power supply for A/D converter.	
AV_{REF0}	Input	Reference voltage input for A/D converter (CH0).	
AV_{REF1}	Input	Reference voltage input for A/D converter (CH1).	
AV_{SS}		GND for A/D converter.	
V_{DD}		Positive power supply. (Connect all three V_{DD} pins to positive power supply.)	
V_{SS}		GND (Connect all four Vss pins to GND.)	
PWE	Input	Permits erasure and write of incorporated Flash EEPROM.	

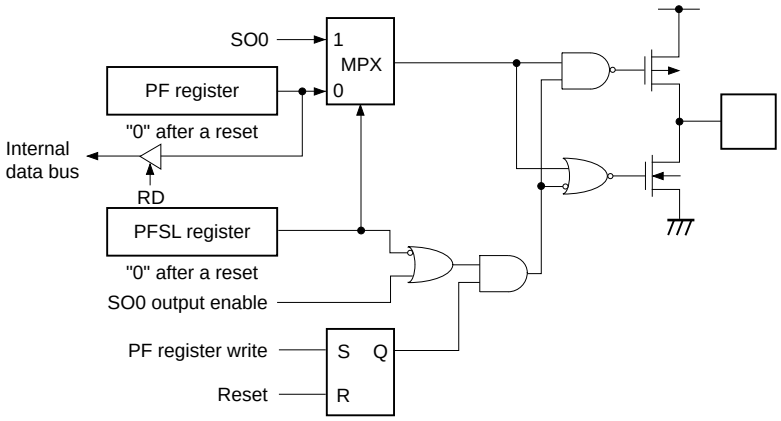
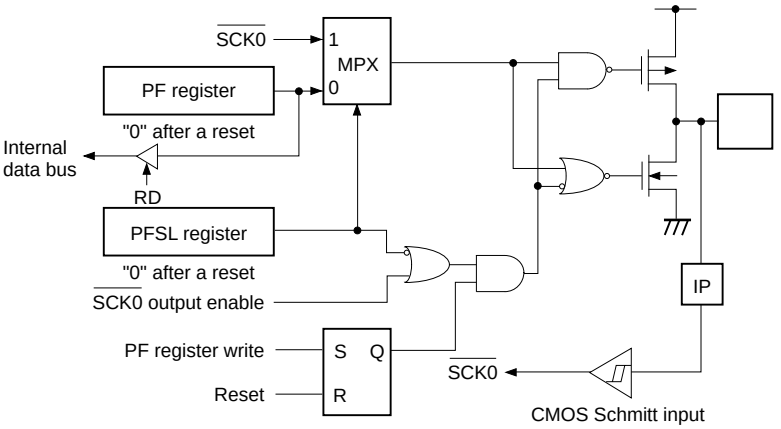
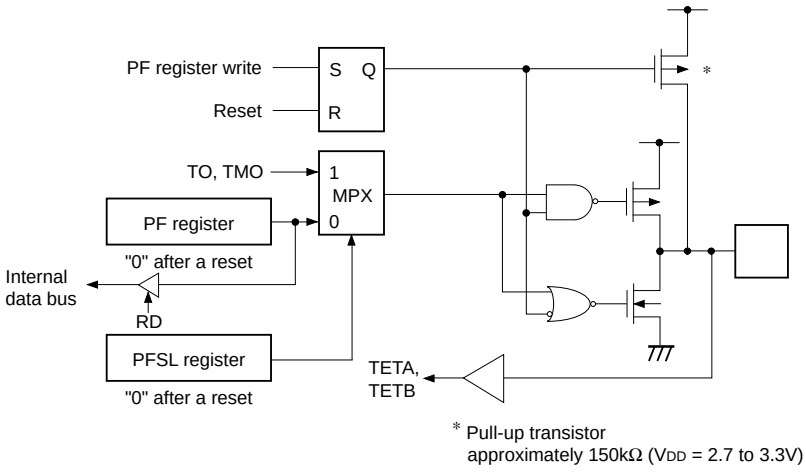
I/O Circuit Format for Pins

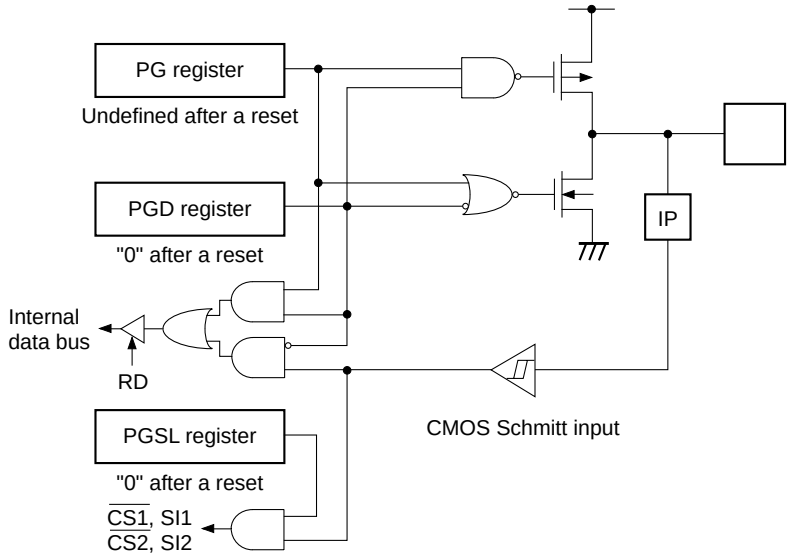
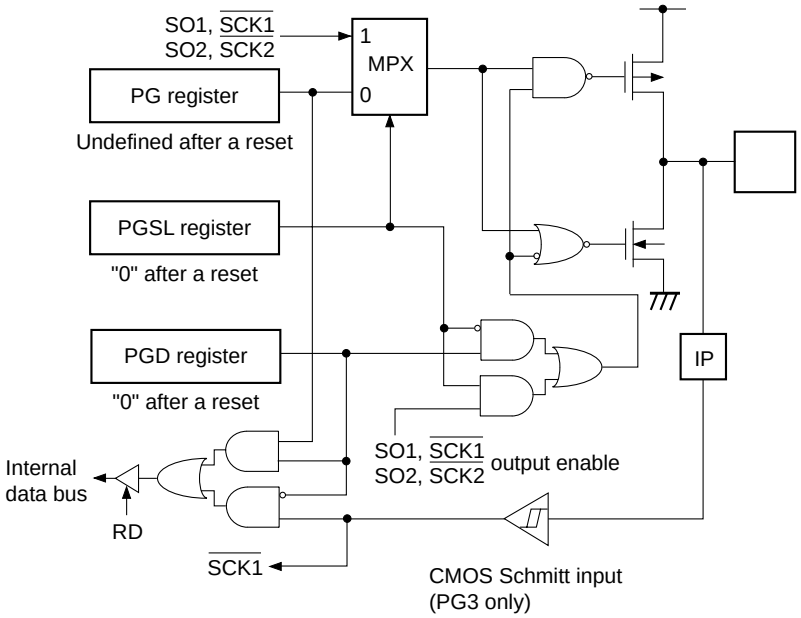
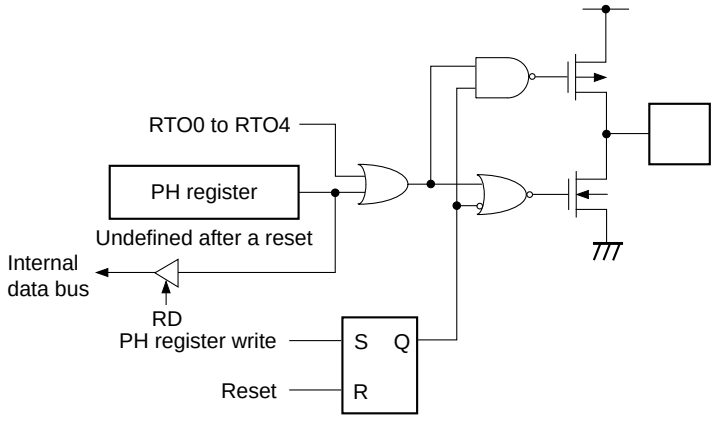
Pin	Circuit format	After a reset
PA0/AN12 to PA7/AN19		Hi-Z
PB0/AN20 to PB3/AN23		Hi-Z
PB4/SI3 PB7/RMC		Hi-Z

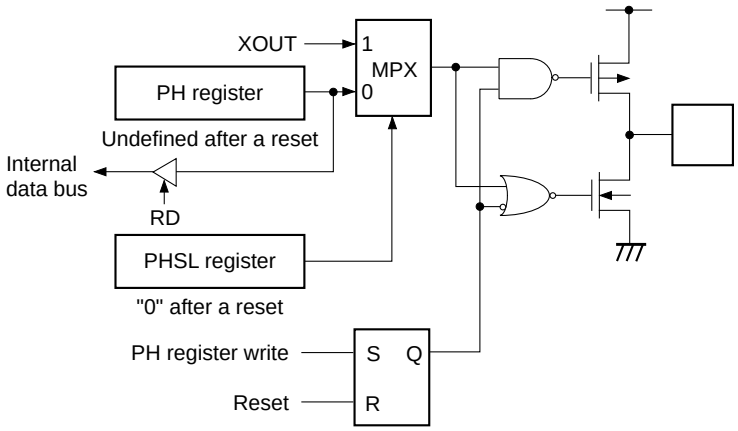
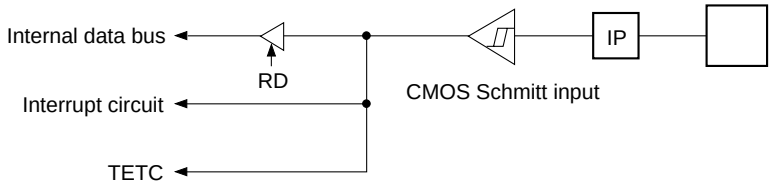
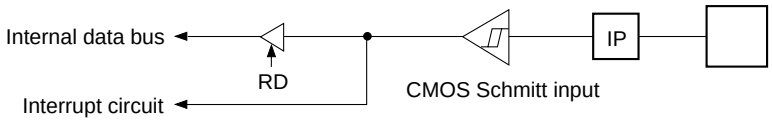
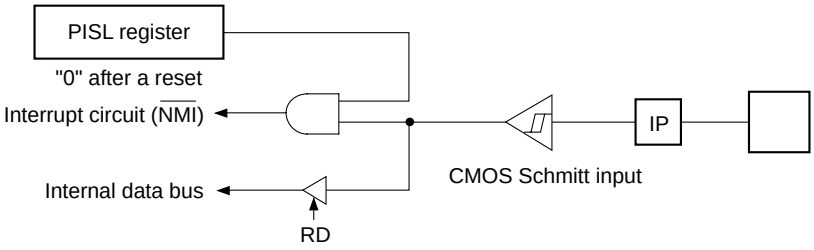
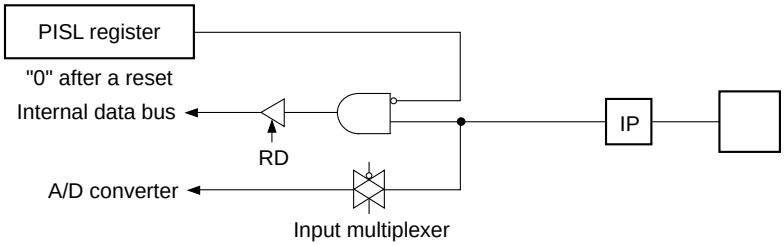
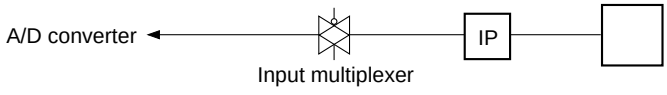
Pin	Circuit format	After a reset
PB5/SO3		Hi-Z
PB6/$\overline{\text{SCK3}}$		Hi-Z
PC0/SDA0 PC1/SCL0 PC2/SDA1 PC3/SCL1		Hi-Z

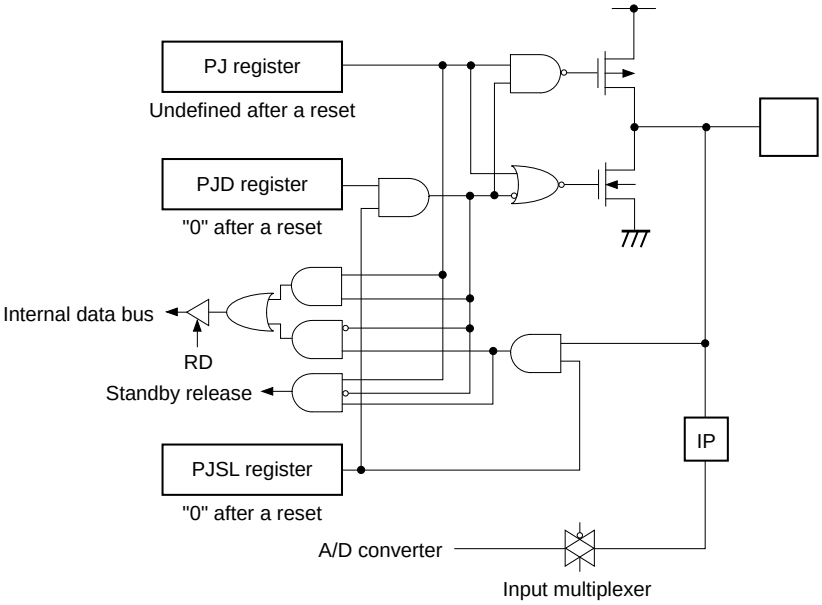
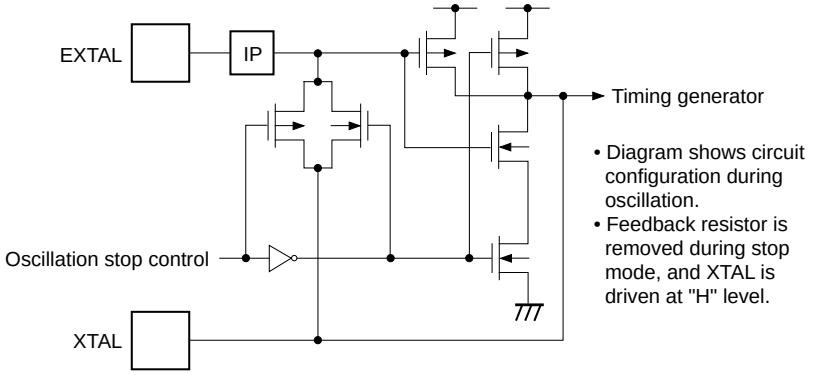
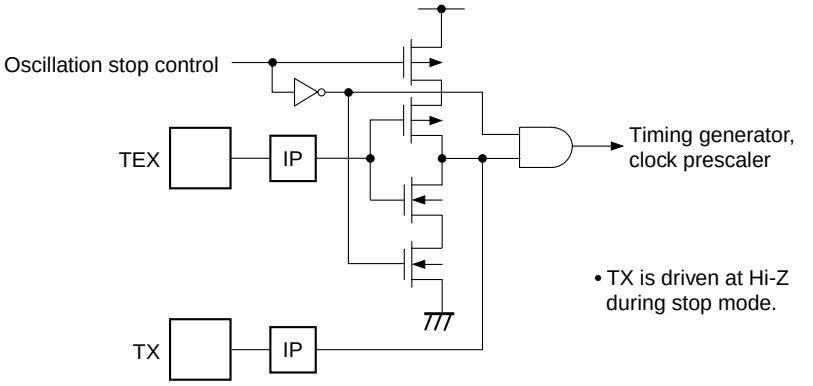
Pin	Circuit format	After a reset
PC4 to PC7		Hi-Z
PD0/$\overline{KS0}$ to PD7/$\overline{KS7}$		Hi-Z
PE0/TxD		Hi-Z

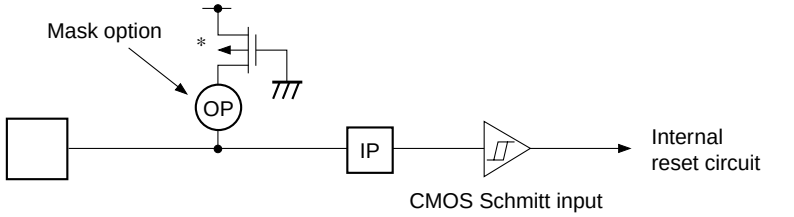
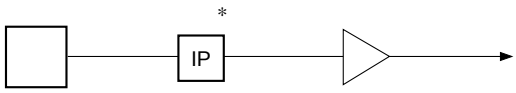
Pin	Circuit format	After a reset
PE1/RxD		Hi-Z
PE2 to PE7		Hi-Z
PF0		Hi-Z
PF1/$\overline{EC}$		Hi-Z
PF2/$\overline{CS0}$ PF3/SI0		Hi-Z

Pin	Circuit format	After a reset
PF4/SO0		Hi-Z
PF5/$\overline{\text{SCK0}}$		Hi-Z
PF6/TO/ TETB PF7/TMO/ TETA		"H" level ("H" level at ON resistance of pull-up transistor during a reset.)

Pin	Circuit format	After a reset
PG0/$\overline{CS1}$ PG1/$\overline{SI1}$ PG4/$\overline{CS2}$ PG5/SI2		Hi-Z
PG2/$\overline{SO1}$ PG3/$\overline{SCK1}$ PG6/$\overline{SO2}$ PG7/$\overline{SCK2}$		Hi-Z
PH0/RTO0 to PH4/RTO4		Hi-Z

Pin	Circuit format	After a reset
PH5/XOUT		Hi-Z
PH6/INT0 to PH7/INT1/ TETC		Hi-Z
PI0/INT2 to PI5/INT7		Hi-Z
PI6/$\overline{\text{NMI}}$		Hi-Z
PI7/AN0		Hi-Z
AN1 to AN3		Hi-Z

Pin	Circuit format	After a reset
PJ0/AN4/ $\overline{KS8}$ to PJ7/AN11/ $\overline{KS15}$		Hi-Z
EXTAL XTAL		Oscillation
TEX TX		Oscillation

Pin	Circuit format	After a reset
$\overline{\text{RST}}$	 * Pull-up transistor approximately 30kΩ (V_{DD} = 2.7 to 3.3V)	"L" level (during a reset)
PWE	 * Input protection only to negative voltage	Hi-Z

Absolute Maximum Ratings (V_{SS} = 0V reference)

Item	Symbol	Rating	Unit	Remarks
Supply voltage	V_{DD}	–0.3 to +4.6	V	
	AV_{DD}	AV_{SS} to +4.6*1	V	
	AV_{REF}	AV_{SS} to +4.6*1	V	
	AV_{SS}	–0.3 to +0.3	V	
Input voltage	V_{IN}	–0.3 to +4.6*2	V	
Output voltage	V_{OUT}	–0.3 to +4.6*2	V	
High level output current	I_{OH}	–5	mA	Output (value per pin)
High level total output current	$\sum I_{OH}$	–50	mA	Total for all output pins
Low level output current	I_{OL}	15	mA	All pins excluding large current output pins (value per pin)
	I_{OLC}	20	mA	Large current output pins*3 (value per pin)
Low level total output current	$\sum I_{OL}$	130	mA	Total for all output pins
Operating temperature	Topr	–20 to +75*4	°C	
Storage temperature	Tstg	–55 to +150	°C	
Allowable power dissipation	P_D	600	mW	QFP-100P-L01
		380	mW	LQFP-100P-L01
		500	mW	LFLGA-104P-02

*1 AV_{DD} and AV_{REF} must be the same voltage with V_{DD}.

*2 V_{IN} and V_{OUT} must not exceed V_{DD} + 0.3V.

*3 The large current drive transistor is N-ch transistor of PD.

*4 Operating temperature range during write/erasure of flash memory is Ta = 0 to 50°C.

Note) Usage exceeding absolute maximum ratings may permanently impair the LSI. Normal operation should be conducted under the recommended operating conditions. Exceeding these conditions may adversely affect the reliability of the LSI.

Recommended Operating Conditions (Vss = 0V reference)

Item	Symbol	Min.	Max.	Unit	Remarks
Supply voltage	V_{DD}	2.7	3.3	V	
		2.2	3.3	V	Guaranteed operation range with TEX clock
		2.2	3.3	V	Guaranteed operation range for clock mode
		2.0	3.3	V	Guaranteed data hold range during stop mode
	AV_{DD}	2.7	3.3	V	*1
	AV_{REF}	2.7	3.3	V	*1
High level input voltage	V_{IH}	$0.7V_{DD}$	V_{DD}	V	*2
	V_{IHS}	$0.8V_{DD}$	V_{DD}	V	CMOS Schmitt input*3
	V_{IHEX}	$0.7V_{DD}$	V_{DD} + 0.3	V	EXTAL, TEX
Low level input voltage	V_{IL}	0	$0.2V_{DD}$	V	*2
	V_{ILS}	0	$0.2V_{DD}$	V	CMOS Schmitt input*3
	V_{ILEX}	–0.3	$0.3V_{DD}$	V	EXTAL, TEX
Operating temperature	Topr	–20	+75	°C	

*1 AV_{DD} and AV_{REF} must be the same voltage with V_{DD}.

*2 PC4 to PC7, PD, PE, PF0, PG2, PG6, PI7, PJ for normal input port.

*3 PB4, PB6, PB7, PC0 to PC3, PF1 to PF3, PF5, PG0, PG1, PG3 to PG5, PH6, PH7, PI0 to PI6, $\overline{RST}$.

Electrical Characteristics

DC Characteristics (Topr = –20 to +75°C, Vss = 0V reference)

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
High level output voltage	V_{OH}	PA, PB, PD, PE, PF4 to PF7, PG, PH0 to PH5, PJ	V_{DD} = 2.7V, I_{OH} = –0.15mA	2.4			V
			V_{DD} = 2.7V, I_{OH} = –0.5mA	2.0			V
		PC	V_{DD} = 2.7V, I_{OH} = –0.05mA	1.3			V
Low level output voltage	V_{OL}	PA, PB , PC4 to PC7, PE , PF4 to PF7, PG, PH0 to PH5, PJ	V_{DD} = 2.7V, I_{OL} = 1.2mA			0.3	V
			V_{DD} = 2.7V, I_{OL} = 1.6mA			0.5	V
		PC0 to PC3 (SCL0, SCL1, SDA0, SDA1)	V_{DD} = 2.7V, I_{OL} = 2.0mA			0.3	V
			V_{DD} = 2.7V, I_{OL} = 3.0mA			0.5	V
		PD	V_{DD} = 2.7V, I_{OL} = 5.0mA			1.0	V
Input current	I_{IHE}	EXTAL	V_{DD} = 3.3V, V_{IH} = 3.3V	0.3		20	µA
	I_{ILE}		V_{DD} = 3.3V, V_{IL} = 0.3V	–0.3		–20	µA
	I_{ILR}	$\overline{RST}$*1	V_{DD} = 3.3V, V_{IL} = 0.3V	–0.9		–250	µA
	I_{IL}	PC*2				–250	µA
			V_{DD} = 2.7V, V_{IH} = 2.4V	–1.0			µA
I/O leakage current	I_{IZ}	PA, PB, PD to PG, PH6, PH7, PI, PJ, AN1 to AN3, TEX	V_{DD} = 3.3V, V_I = 0, 3.3V			±10	µA
Open drain output leakage current (N-ch Tr. off state)	I_{LOH}	PC*2	V_{DD} = 3.3V, V_{IH} = 3.3V			10	µA
Supply current*3	I_{DD1}*4	V_{DD}, V_{SS}	V_{DD} = 3.0 ± 0.3V, 20MHz crystal oscillation, A/D off state (C_1 = C_2 = 10pF)		20	26	mA
	I_{DD2}		V_{DD} = 3.0 ± 0.3V, 32kHz crystal oscillation, 20MHz oscillation stop, A/D off state (C_1 = C_2 = 47pF)		70	150	µA
	I_{DDS1}		V_{DD} = 3.0 ± 0.3V, 20MHz crystal oscillation, A/D off state (C_1 = C_2 = 10pF), sleep mode		7	12	mA
	I_{DDS2}		V_{DD} = 3.0 ± 0.3V, 32kHz crystal oscillation, 20MHz oscillation stop, A/D off state (C_1 = C_2 = 47pF), sleep mode		12	70	µA
	I_{DDS3}		V_{DD} = 3.0V, 32kHz crystal oscillation, 20MHz oscillation stop (C_1 = C_2 = 47pF), clock mode		7	50	µA
	I_{DDS4}		V_{DD} = 3.0V, stop mode			40	µA

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
Input capacitance	C_{IN}	PA, PB0 to PB4, PB6, PB7, PC to PE, PF0 to PF3, PF5, PG, PH6, PH7, PI, PJ, AN1 to AN3, EXTAL, TEX, $\overline{RST}$	Clock 1MHz 0V for all pins excluding measured pins		10	20	pF

*1 $\overline{RST}$ specifies the input current when pull-up resistor has been selected; the leakage current when no resistor has been selected.

*2 PC specifies the input current when pull-up resistor has been selected; the leakage current when no resistor has been selected.

*3 When all output pins are open.

*4 When the upper two bits (PCK1, PCK0) of the clock control register (CLC: 0002FEh) are set to "00" and the LSI is operated in high-speed mode (2 frequency dividing clock).

AC Characteristics

(1) Clock timing

(Topr = –20 to +75°C, V_{DD} = 2.7 to 3.3V, Vss = 0V reference)

Item	Symbol	Pins	Conditions		Min.	Typ.	Max.	Unit
Main clock base oscillation frequency	f_{EX}	EXTAL, XTAL	Fig.1	V_{DD} = 3.0 ± 0.3V	15	20	20.5	MHz
Main clock base oscillation input pulse width	t_{XH}	EXTAL	Fig.1, Fig.2 External clock drive	V_{DD} = 3.0 ± 0.3V	20			ns
	t_{XL}							
Main clock base oscillation input rise time, fall time	t_{XR}	EXTAL	Fig.1, Fig.2 External clock drive	V_{DD} = 3.0 ± 0.3V			14	ns
	t_{XF}							
Sub clock base oscillation frequency	f_{TEX}	TEX, TX	Fig.1	V_{DD} = 2.2 to 3.3V	32.735	32.768	33.096	kHz
Sub clock base oscillation input pulse width	t_{TH}	TEX	Fig.1, Fig.2 External clock drive	V_{DD} = 3.3V	15.3			µs
	t_{TL}			V_{DD} = 2.2V	15.3			µs
Sub clock base oscillation input rise time, fall time	t_{TR}	TEX	Fig.1, Fig.2 External clock drive	V_{DD} = 3.3V			200	ns
	t_{TF}			V_{DD} = 2.2V			200	ns

Note) tsys indicates the four values below according to the upper two bits (PCK1, PCK0) of the clock control register (CLC: 0002FEh) during main mode and tsys = $2/f_{TEX}$ = 61.04µs during sub mode.
tsys [ns] = $2/f_{EX}$ (PCK1, PCK0 = 00), $4/f_{EX}$ (PCK1, PCK0 = 01), $8/f_{EX}$ (PCK1, PCK0 = 10), $16/f_{EX}$ (PCK1, PCK0 = 11)

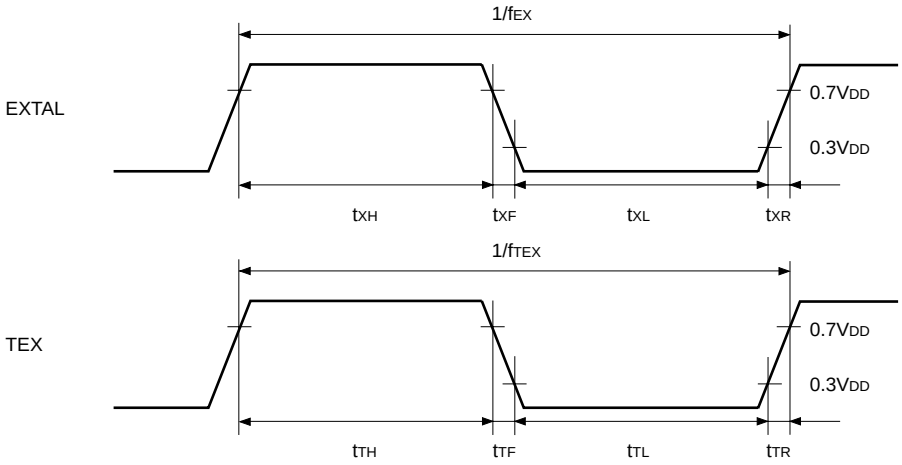


Fig.1. Clock timing

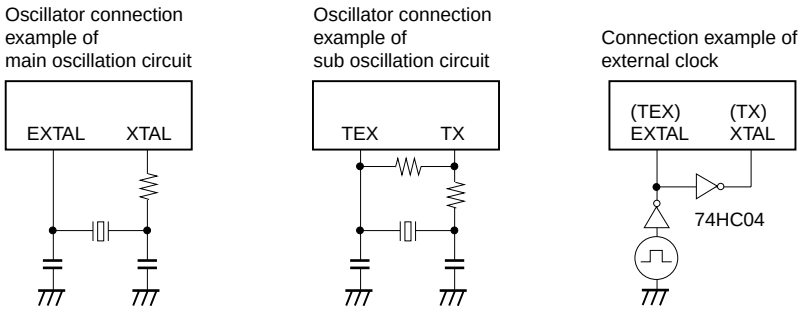


Fig.2. Oscillator connection and clock applied conditions

(2) Event count input (Topr = –20 to +75°C, V_{DD} = 2.7 to 3.3V, Vss = 0V reference)

Item	Symbol	Pins	Conditions	Min.	Max.	Unit
Event count input clock pulse width	t_{EH}, t_{EL}	$\overline{EC}$	Fig.3	tsys + 100		ns

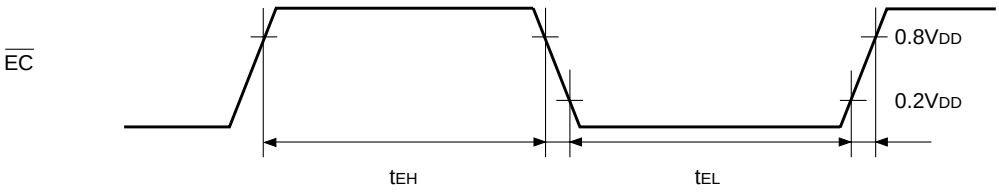


Fig.3. Event count input timing

(3) Interruption and reset input (Topr = –20 to +75°C, V_{DD} = 2.7 to 3.3V, Vss = 0V reference)

Item	Symbol	Pins	Conditions		Min.	Max.	Unit
External interruption high, low level width	t_{IH}, t_{IL}	$\overline{NMI}$ INT0 to INT7 $\overline{KS0}$ to $\overline{KS15}$	Main mode Sub mode Sleep mode		tsys + 100		ns
			Clock mode Stop mode		1		µs
		INT4 to INT7	Noise filter selected	ϕ	2tsys + 100		ns
				PS4	32/fEX + 100		
				PS6	128/fEX + 100		
Reset input low level width	t_{RST}	$\overline{RST}$	Fig.5		50/fEX		ns

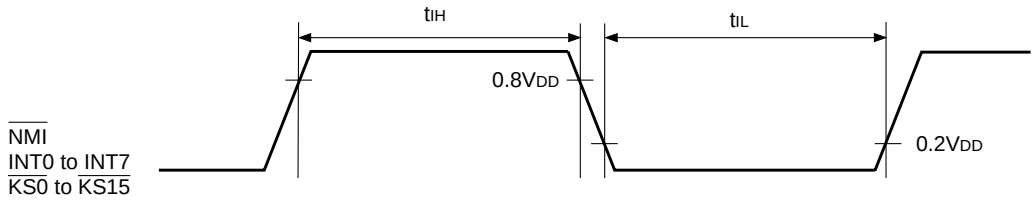


Fig.4. Interruption input timing

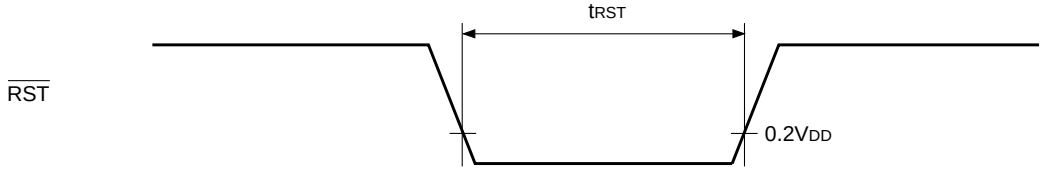


Fig.5. Reset input timing

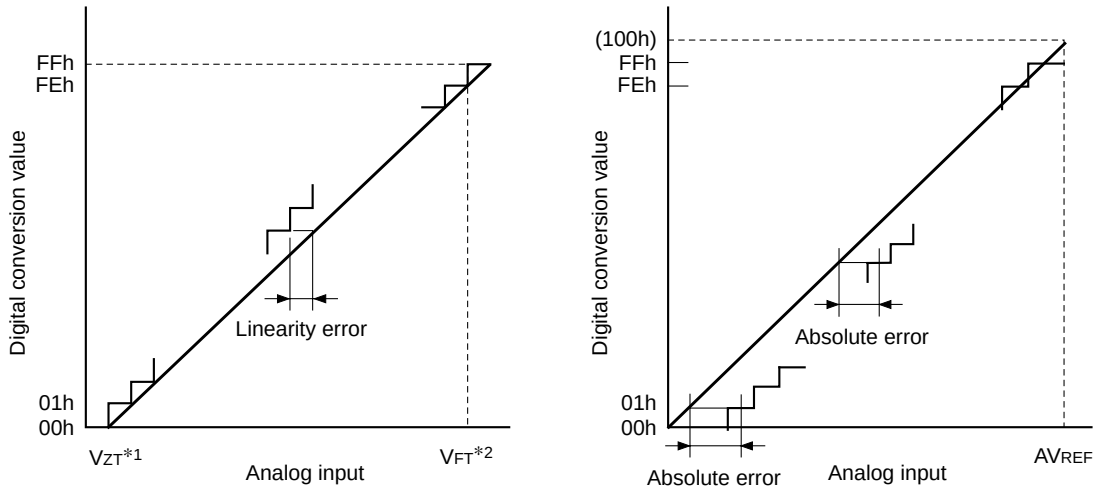
(4) A/D converter characteristics

(Topr = –20 to +75°C, V_{DD} = AV_{DD} = AV_{REF} = 2.7 to 3.3V, Vss = AVss = 0V reference)

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
Resolution						8	Bits
Linearity error			V_{DD} = AV_{DD} = AV_{REF} = 3.0V			±1	LSB
Absolute error						±3	LSB
Conversion time	t_{CONV}			34tsys			µs
Sampling time	t_{SAMP}			9tsys			µs
Reference input voltage	V_{REF}	AV_{REF}	V_{DD} = AV_{DD} = AV_{REF}	2.7		3.3	V
Analog input voltage	V_{IAN}	AN0 to AN23		0		AV_{REF}	V
AV_{REF} current	I_{REF}	AV_{REF0} AV_{REF1}	Main mode Sub mode		1.1	1.5	mA
	I_{REFS}		Clock mode Stop mode during ADC off state*			10	µA

* When Bit 14 (ADOFF) of A/D control status register (ADCS0: 00013Ch, ADCS1: 00014Ch) is specified to "1".

Note) AV_{DD} and AV_{REF} must be the same voltage with V_{DD}.



*1 V_{ZT}: Value at which the digital conversion value changes from 00h to 01h and vice versa.

*2 V_{FT}: Value at which the digital conversion value changes from FEh to FFh and vice versa

Fig.6. Definition of A/D converter terms

(5) Serial transfer (CH0, CH1, CH2) (Topr = –20 to +75°C, V_{DD} = 2.7 to 3.3V, Vss = 0V reference)

Item	Symbol	Pins	Conditions	Min.	Max.	Unit
$\overline{CS} \downarrow \rightarrow \overline{SCK}$ delay time	t_{DCSK}	$\overline{SCK0}$ $\overline{SCK1}$ $\overline{SCK2}$	External start transfer mode ($\overline{SCK}$ = output mode)		1.5tsys + 200	ns
$\overline{CS} \uparrow \rightarrow \overline{SCK}$ float delay time	t_{DCSKF}	$\overline{SCK0}$ $\overline{SCK1}$ $\overline{SCK2}$	External start transfer mode ($\overline{SCK}$ = output mode)		1.5tsys + 200	ns
$\overline{CS} \downarrow \rightarrow$ SO delay time	t_{DCSO}	SO0 SO1 SO2	External start transfer mode		1.5tsys + 200	ns
$\overline{CS} \uparrow \rightarrow$ SO float delay time	t_{DCSOF}	$\overline{CS0}$ $\overline{CS1}$ $\overline{CS2}$	External start transfer mode		1.5tsys + 200	ns
$\overline{CS}$ high level width	t_{WHCS}	$\overline{CS0}$ $\overline{CS1}$ $\overline{CS2}$	External start transfer mode	tsys + 100		ns
$\overline{SCK}$ cycle time	t_{KCY}	$\overline{SCK0}$ $\overline{SCK1}$ $\overline{SCK2}$	Input mode	2tsys + 200		ns
			Output mode	16/f_{EX}		ns
$\overline{SCK}$ high, low pulse width	t_{KH} t_{KL}	$\overline{SCK0}$ $\overline{SCK1}$ $\overline{SCK2}$	Input mode	tsys + 100		ns
			Output mode	8/f_{EX} – 100		ns
SI input data setup time (for $\overline{SCK} \uparrow$)	t_{SIK}	SI0 SI1 SI2	$\overline{SCK}$ input mode	100		ns
			$\overline{SCK}$ output mode	200 – tsys		ns
SI input data hold time (for $\overline{SCK} \uparrow$)	t_{KSI}	SI0 SI1 SI2	$\overline{SCK}$ input mode	tsys + 100		ns
			$\overline{SCK}$ output mode	tsys + 100		ns
$\overline{SCK} \downarrow \rightarrow$ SO delay time	t_{KSO}	SO0 SO1 SO2	$\overline{SCK}$ input mode		tsys + 150	ns
			$\overline{SCK}$ output mode		100	ns
Minimum interval time	t_{INT}	$\overline{SCK0}$ $\overline{SCK1}$ $\overline{SCK2}$	$\overline{SCK}$ input mode	3tsys + 100		ns
			$\overline{SCK}$ output mode	8/f_{EX} – 100		ns

Note) The load condition for the $\overline{SCK}$ output mode and SO output delay time is 100pF.

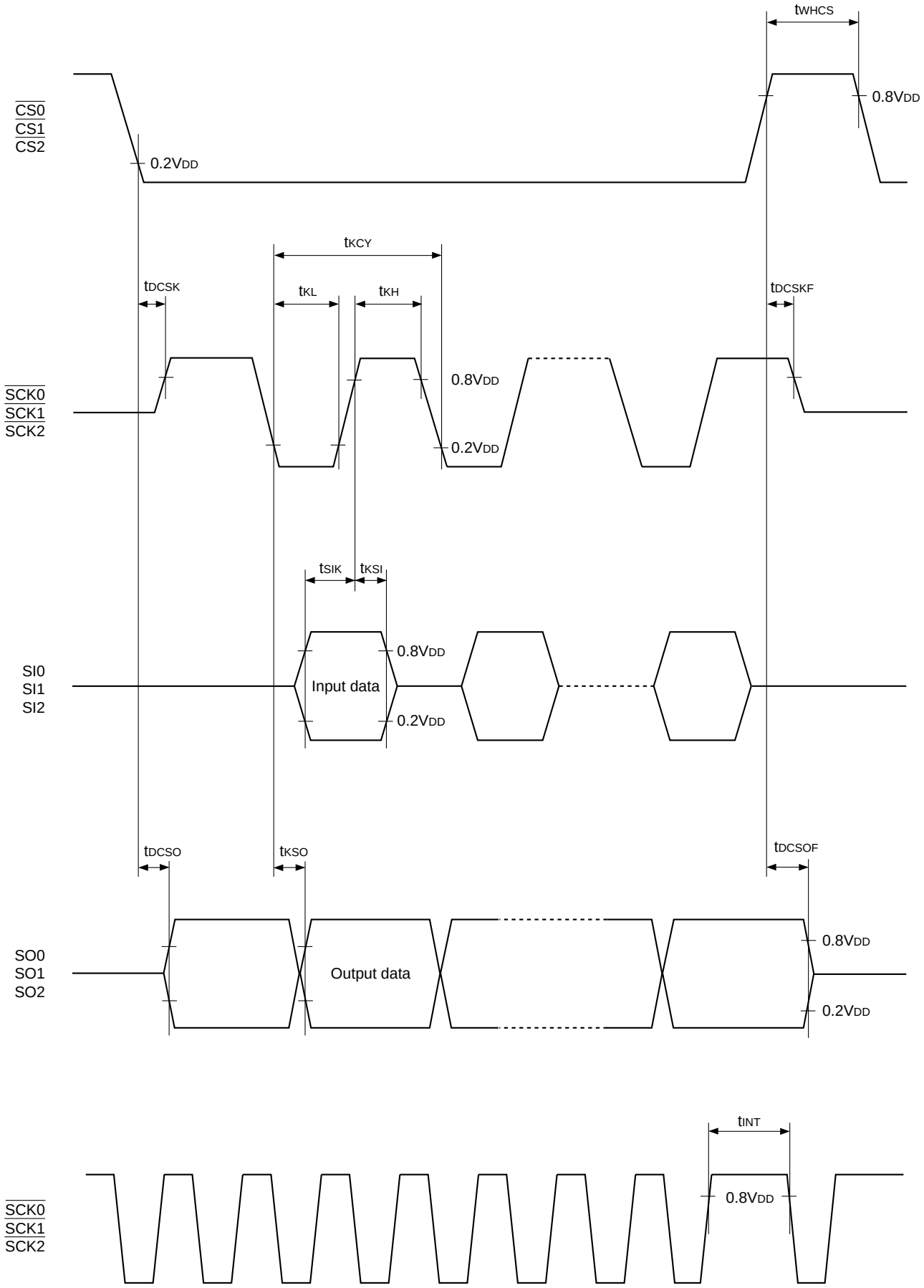


Fig.7. Serial transfer CH0, CH1, CH2 timing

(6) Serial transfer (CH3) [SIO mode] (Topr = –20 to +75°C, V_{DD} = 2.7 to 3.3V, Vss = 0V reference)

Item	Symbol	Pins	Conditions	Min.	Max.	Unit
$\overline{SCK}$ cycle time	t_{KCY}	$\overline{SCK3}$	Input mode	2tsys + 200		ns
			Output mode	$16/f_{EX}$		ns
$\overline{SCK}$ high, low pulse width	t_{KH} t_{KL}		Input mode	tsys + 100		ns
			Output mode	$8/f_{EX}$ – 100		ns
SI input data setup time (for $\overline{SCK}$ ↑)	t_{SIK}	SI3	$\overline{SCK}$ input mode	100		ns
			$\overline{SCK}$ output mode	200		ns
SI input data hold time (for $\overline{SCK}$ ↑)	t_{KSI}		$\overline{SCK}$ input mode	tsys + 100		ns
			$\overline{SCK}$ output mode	200		ns
$\overline{SCK}$ ↓ → SO delay time	t_{KSO}	SO3	$\overline{SCK}$ input mode		tsys + 150	ns
			$\overline{SCK}$ output mode		100	ns

Note) The load condition for the $\overline{SCK}$ output mode and SO output delay time is 100pF.

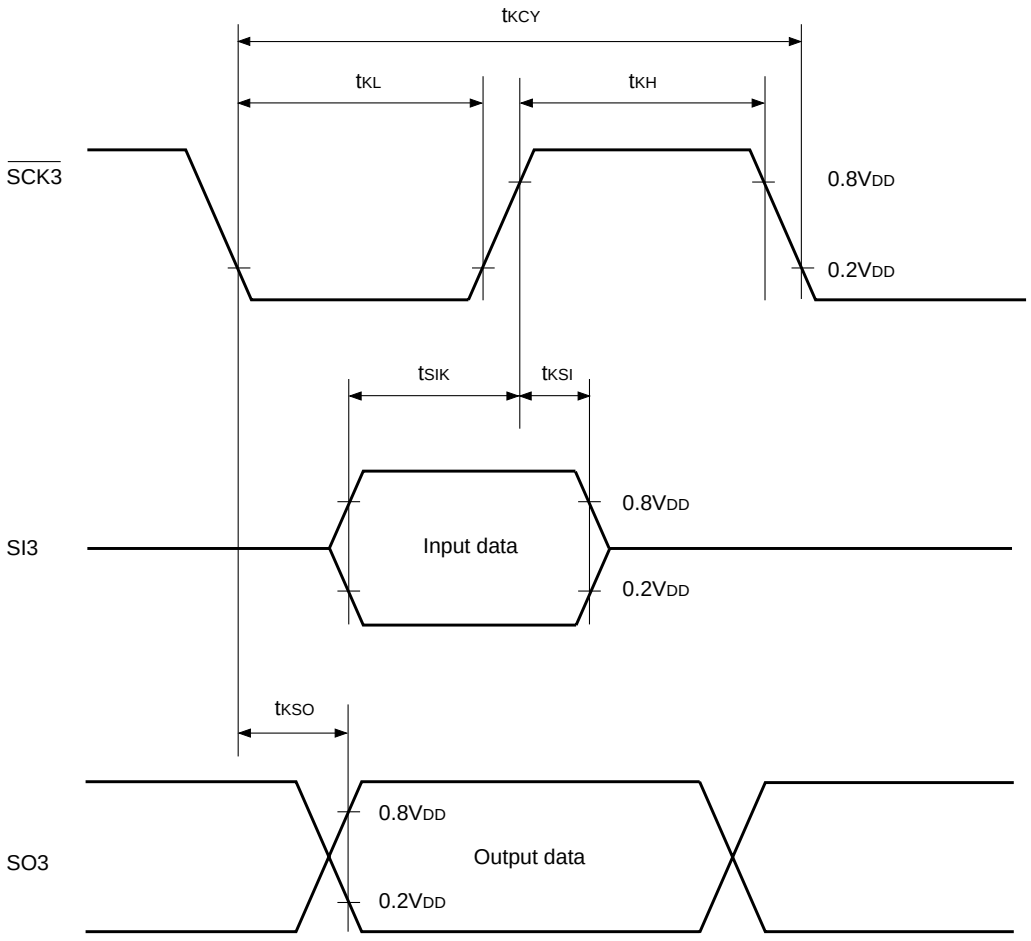


Fig.8. Serial transfer CH3 timing (SIO mode)

(7) Serial transfer (CH3) [Special mode] (Topr = –20 to +75°C, V_{DD} = 2.7 to 3.3V, Vss = 0V reference)

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
SO cycle time*	t_{LCY}	SO3 SI3	f_{EX} = 20MHz		104		µs
SI input setup time	t_{LSU}	SI3		2			
SI input hold time	t_{LHD}	SI3		2			
Input start bit high level width	t_{LSBH}	SI3	Communication slave mode	1			
SI → SO delay time	t_{LIO}	SO3				1	

* When lower 2 bits (SCK1, SCK0) of serial mode register (SIOM3: 0001A4h) is specified to "00".

Note) The load condition for the SO output delay time is 100pF.

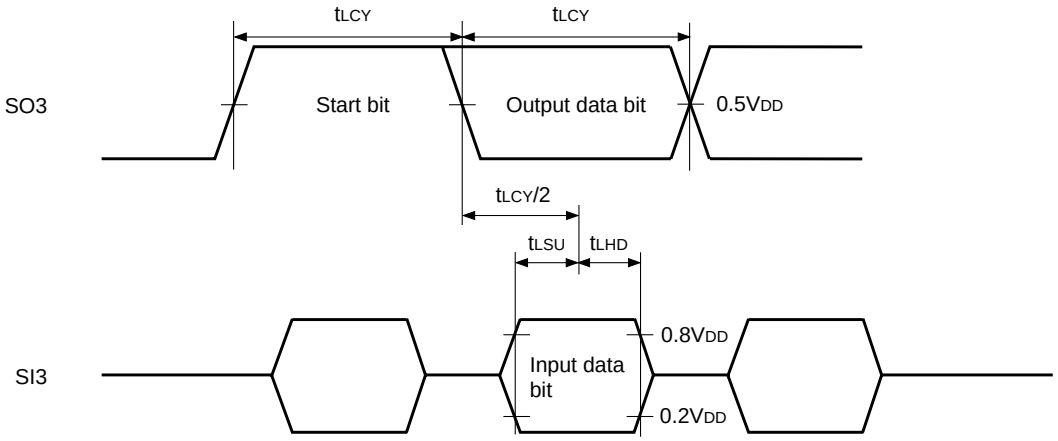


Fig.9. Serial transfer CH3 timing (Special mode)

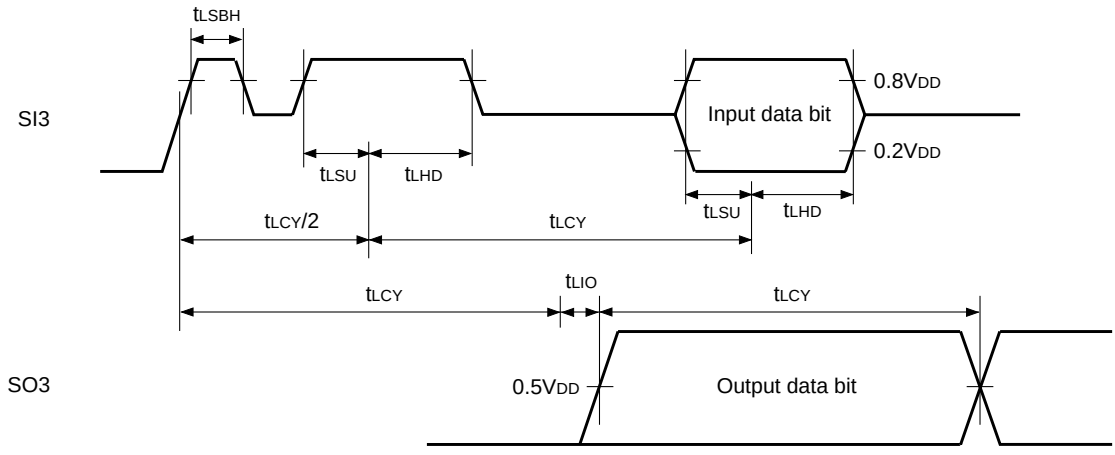


Fig.10. Serial transfer CH3 timing (Special mode)

(8) I²C bus (CH0, CH1) (Topr = –20 to +75°C, V_{DD} = 2.7 to 3.3V, Vss = 0V reference)

Item	Symbol	Pins	Standard mode		High-speed mode		Unit
			Min.	Max.	Min.	Max.	
SCK clock frequency	t_{SCL}	SCL0 SCL1	0	100	0	400	kHz
Bus free time between stop and start conditions	t_{BUF}	SDA0 SDA1	4.7		1.3		µs
Hold time under (resend) start condition	$t_{HD;STA}$	SDA0, SDA1 SCL0, SCL1	4.0		0.6		µs
Hold time in SCL clock low state	t_{Low}	SCL0 SCL1	4.7		1.3		µs
Hold time in SCL clock high state	t_{High}	SCL0 SCL1	4.0		0.6		µs
Setup time under (resend) start condition	$t_{SU;STA}$	SDA0, SDA1 SCL0, SCL1	4.7		0.6		µs
Data hold time	$t_{HD;DAT}$	SDA0, SDA1 SCL0, SCL1	0		0	0.9	µs
Data setup time	$t_{SU;DAT}$	SDA0, SDA1 SCL0, SCL1	250		100		ns
SCL, SDA signal output rise time	t_{Rd} t_{Rc}	SDA0, SDA1 SCL0, SCL1		1000	20 + α*	300	ns
SCL, SDA signal output fall time	t_{Fd} t_{Fc}	SDA0, SDA1 SCL0, SCL1		300	20 + α*	300	ns
Setup time under stop condition	$t_{SU;STO}$	SDA0, SDA1 SCL0, SCL1	4.0		0.6		µs

* Due to the total capacitance of the bus.

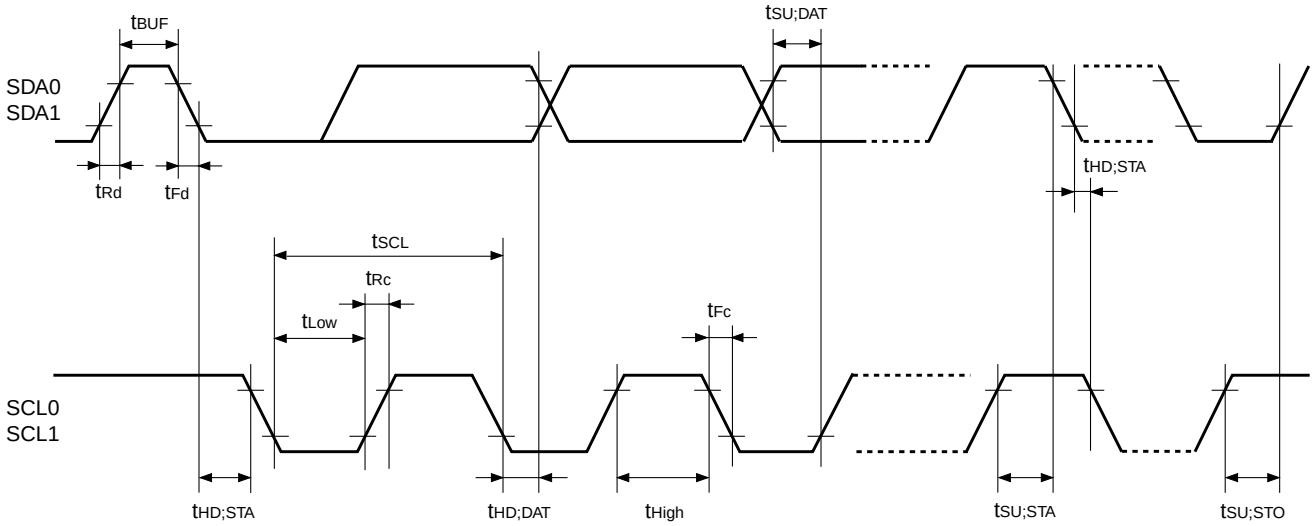


Fig.11. I²C bus timing

(9) Remote control reception (Topr = –20 to +75°C, V_{DD} = 2.7 to 3.3V, Vss = 0V reference)

Item	Symbol	Pins	Conditions		Min.	Max.	Unit
Remote control receive high, low level width	t_{RMC}	RMC	Main mode	PS5 selected	128/f_{EX} + 100		ns
				PS7 selected	512/f_{EX} + 100		
				PS9 selected	2048/f_{EX} + 100		
				32k selected	4/f_{TEX} + 100		
			Sub mode		8/f_{TEX} + 100		

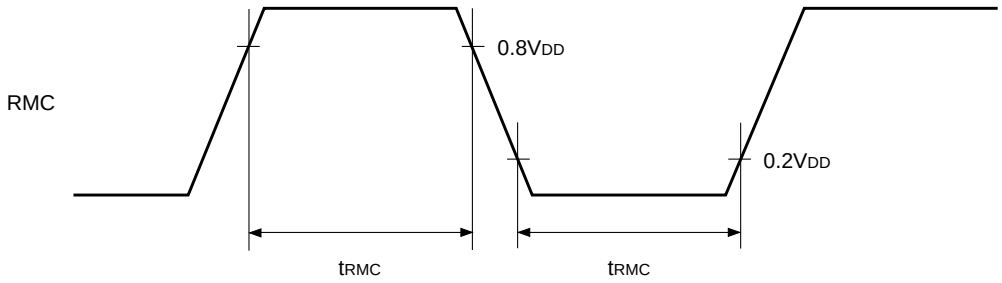


Fig.12. Remote control signal input timing

Appendix

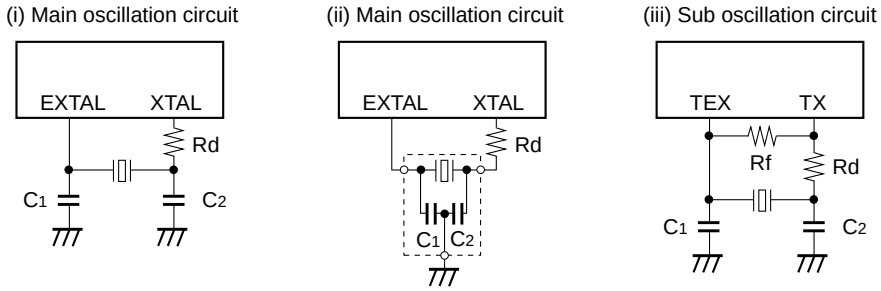


Fig.13. Recommended oscillation circuit

Manufacturer	Model	f_{EX} (MHz)	C_1 (pF)	C_2 (pF)	Rd (Ω)	Circuit example	Remarks
MURATA MFG CO., LTD.	CSA12.0MTZ	12.0	30	30	0	(i)	
	CSA16.00MXZ040	16.0	15	15	0		
	CSA20.00MXZ040	20.00	10	10	0		
	CST12.0MTW*	12.0	30	30	0	(ii)	
	CST16.00MXW0C3*	16.0	15	15	0		
RIVER ELETEC CO., LTD.	HC-49/U03	12.00	10	10	220	(i)	CL = 10pF
KINSEKI LTD.	HC-49/U-S	12.0	12	12	1.0k	(i)	CL = 12pF
		16.0	12	12	470		
		20.0	12	12	390		
TDK Corporation	CCR12.0MSC5*	12.0	20 (±20%)	20 (±20%)	0	(ii)	
	CCR16.0MSC6*	16.0	10 (±20%)	10 (±20%)			
	CCR20.0MSC6*	20.0	10 (±20%)	10 (±20%)			
Seiko Instruments Inc.	VTC-200 SP-T	32.768kHz	20	18	150k	(iii)	Rf = 10MΩ CL = 12.5pF

* Indicates types with on-chip grounding capacitor (C_1, C_2). CCR***: Surface mounted type ceramic oscillator.
CL : Load capacitor

Mask option table

Item	Content	
Reset pin pull-up resistor	Non-existent	Existent

Notes on Using the PF7 Pin

The PF7 pin of the Flash EEPROM incorporated version provides a flash mode setting function. Note the following points when using this pin.

1. Although the PF7 pin output is made at high level during a reset, the pin is driven at a relatively high impedance of about 150kΩ. Note that V_{OH} does not fall below $0.7V_{DD}$ due to partial pressure with the load impedance of the external circuit.

2. When the software reset function is used, the PF7 pin may not rise enough during a reset. Switching the PF7 pin to high output or connecting pull-up resistor is recommended before software reset is executed.

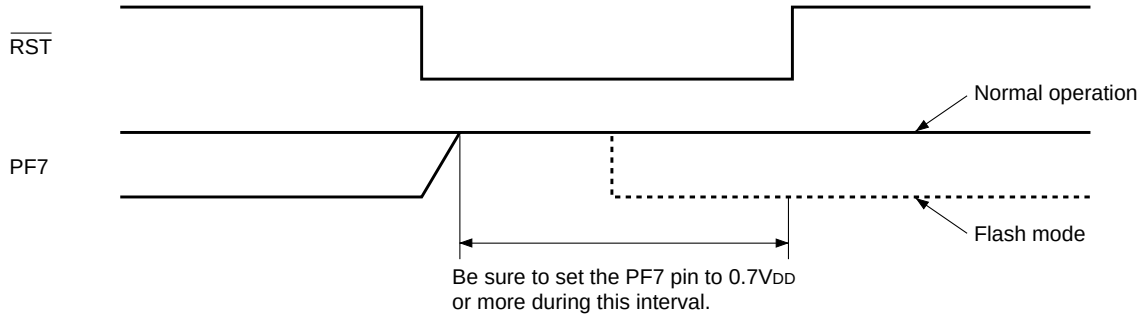


Fig.14. Status of the PF7 pin during a reset

Description of Flash Memory Performance

Item	Performance
Operational mode	Off-board parallel, on-board serial
Programming method	Page units (512-bit units)
Erase method	All erase
Data hold	10 years*1

*1 when data is used and stored under recommended operating conditions.

(Ta = 0 to +50°C, V_{DD} = 2.7 to 3.3V, V_{SS} = 0V reference)

Item	Min.	Typ.	Max.	Unit
Write time*2		8	12	ms/512 bits
Erase time			50	ms
Program/erase count			100	Count

*2 When write clock f_{FCK} = 10MHz is used in off-board parallel mode.

On-board Write

By performing steps 1) through 3) below on the user's hardware, the microcontroller can be reset/started and the Flash EEPROM overwritten,

1) Fix the mode control pin using external hardware
   PF7/TETA pin → Fix to "L" level
   PF6/TETB pin → Fix to "H" level or leave open
   PH7/TETC pin → Fix to "H" level
   PWE pin → Fix to "H" level

2) Connect the microcontroller and SFP-2 using the specified connection method.

3) Overwrite the Flash EEPROM from the SFP-2.

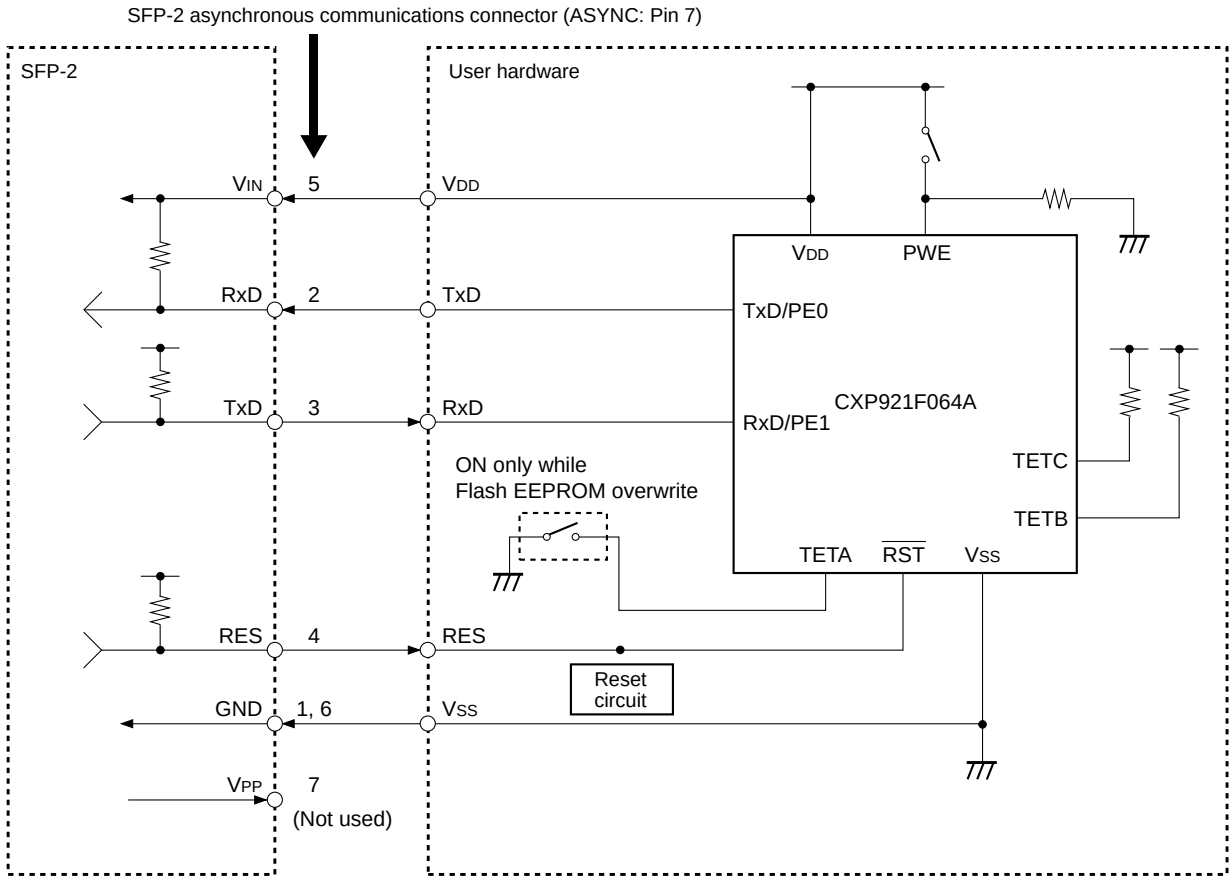


Fig.15. Example of Connection between the SFP-2 and User Hardware

1. The PWE pin provides a function for writing/erasing the Flash EEPROM. Fix this pin to "H" level to overwrite or erase the Flash EEPROM. Fix this pin to "L" level to forcibly prohibit overwriting.
2. Since an AMP-CT receptal 173977-7 is used as the connector for the flash programmer (SFP-2), an AMP-CT connector 175489-7 is recommended for the user hardware.

* The SFP-2 is manufactured and sold by MITEC SYSTEMS, INC.

Off-board Write

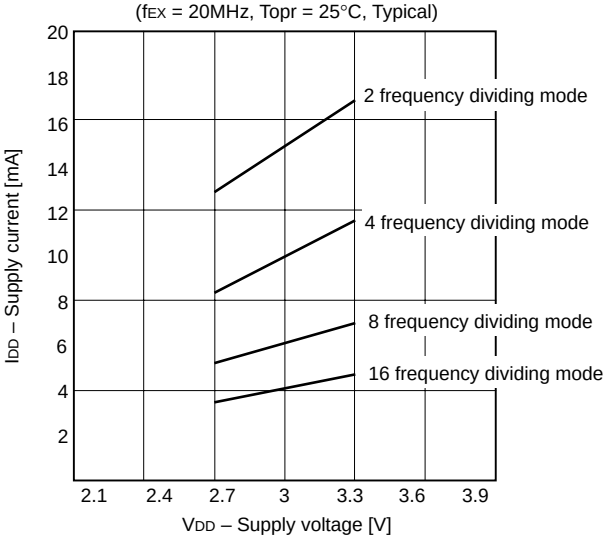
The SFP-2 is used to write data. The setting is as follows.

Device type	SPC970FLSH#0 ADAPTER
ROM area	START : FC0000 END : FFFFFF

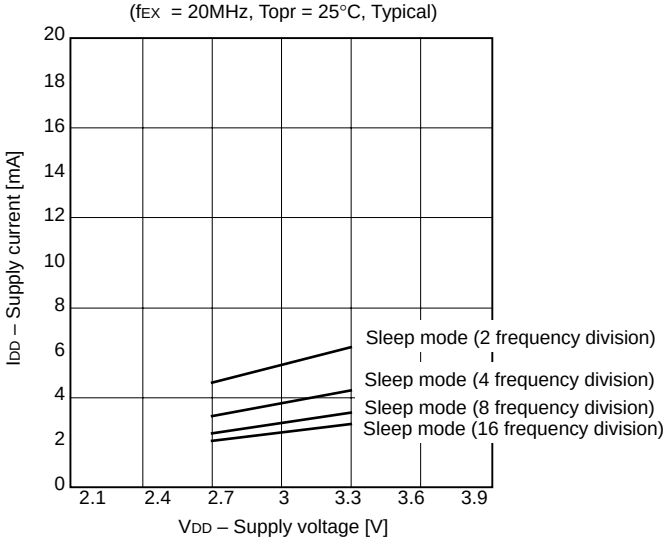
For details on how to write data using the SFP-2, refer to the SFP-2 User's Manual.

Characteristics Curve

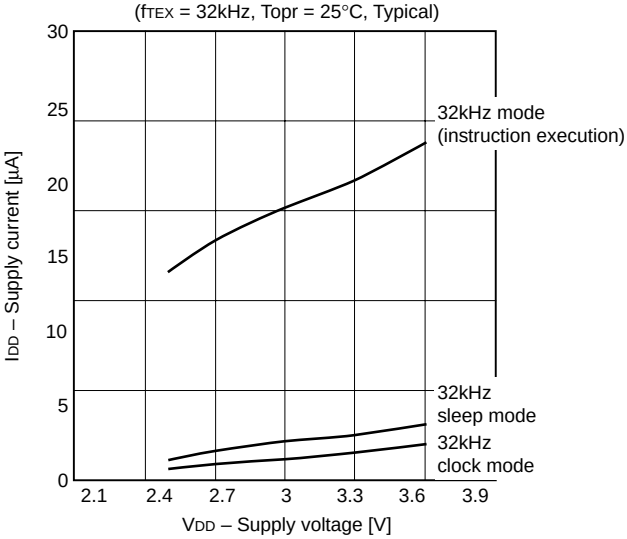
IDD vs. VDD
(fEX = 20MHz, Topr = 25°C, Typical)



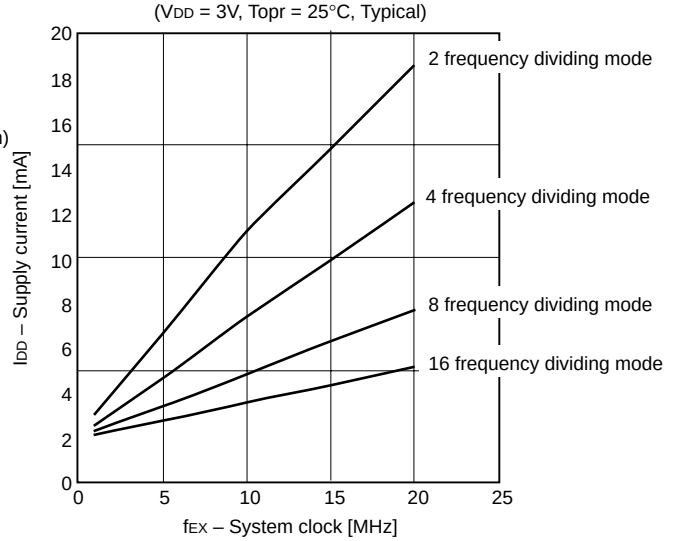
IDD vs. VDD
(fEX = 20MHz, Topr = 25°C, Typical)



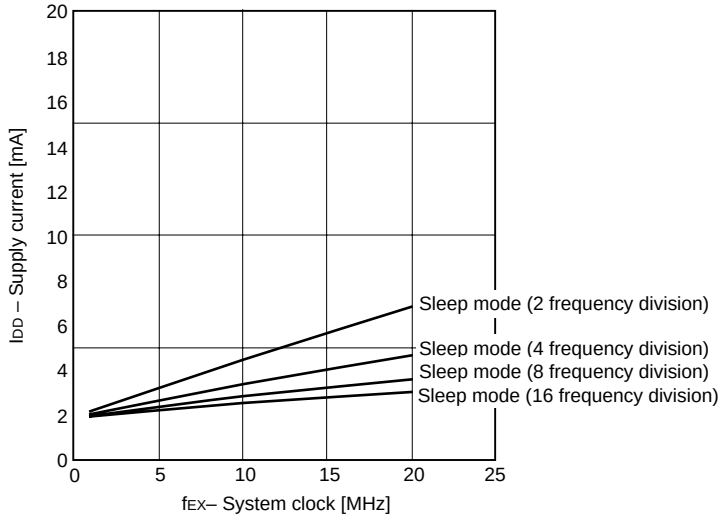
IDD vs. VDD
(fTEX = 32kHz, Topr = 25°C, Typical)



IDD vs. fEX
(VDD = 3V, Topr = 25°C, Typical)

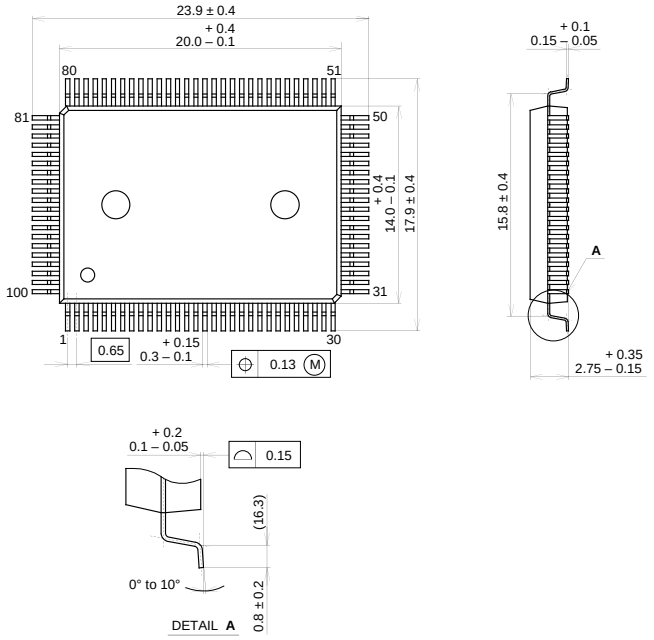


IDD vs. fEX
(VDD = 3V, Topr = 25°C, Typical)



Package Outline Unit: mm

100PIN QFP (PLASTIC)



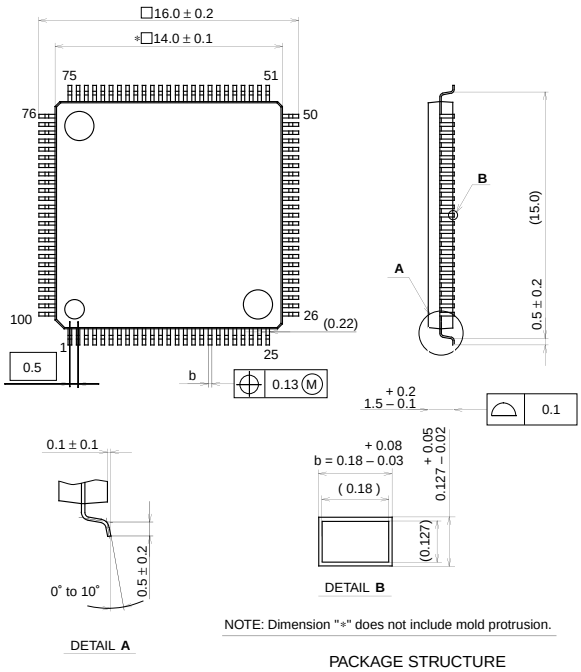
SONY CODE	QFP-100P-L01
EIAJ CODE	QFP100-P-1420
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	1.7g

Package Outline Unit: mm

100PIN LQFP (PLASTIC)



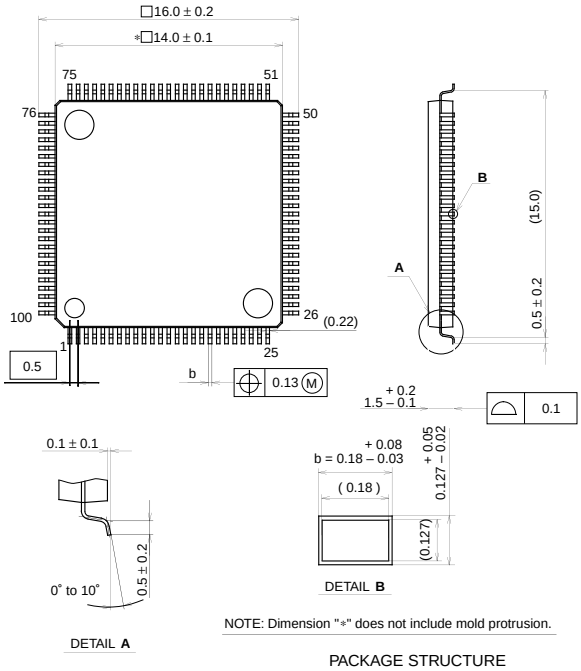
NOTE: Dimension "*" does not include mold protrusion.

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42 / COPPER ALLOY
PACKAGE MASS	0.7g

SONY CODE	LQFP-100P-L01
EIAJ CODE	P-LQFP100-14x14-0.5
JEDEC CODE	————

100PIN LQFP (PLASTIC)



NOTE: Dimension "*" does not include mold protrusion.

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42 / COPPER ALLOY
PACKAGE MASS	0.7g

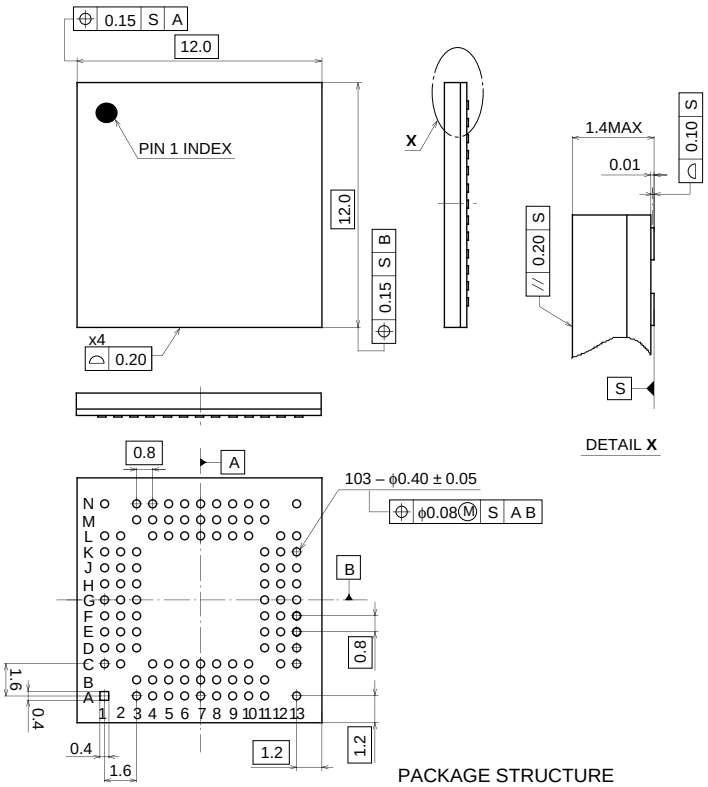
SONY CODE	LQFP-100P-L01
EIAJ CODE	P-LQFP100-14x14-0.5
JEDEC CODE	————

LEAD SPECIFICATIONS

ITEM	SPEC.
LEAD MATERIAL	ALLOY 42
LEAD TREATMENT	Sn-Bi 2.5%
LEAD TREATMENT THICKNESS	5-18μm

Package Outline Unit: mm

104PIN LFLGA



PACKAGE STRUCTURE

SONY CODE	LFLGA-104P-02
EIAJ CODE	LFLGA104-P-1212
JEDEC CODE	————

PACKAGE MATERIAL	ORGANIC SUBSTRATE
TERMINAL TREATMENT	GOLD PLATING
TERMINAL MATERIAL	NICKEL PLATING
PACKAGE MASS	0.4g