

N-Channel 80 V (D-S) MOSFET

PRODUCT SUMMARY					
V _{DS} (V)	$R_{DS(on)}(\Omega)$	I _D (A) ^a	Q _g (Typ.)		
80	0.075 at V _{GS} = 10 V	3.5	7.3 nC		
80			7.3110		

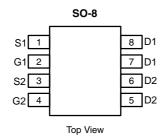
FEATURES

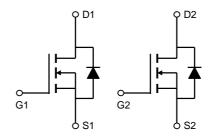
- Halogen-free According to IEC 61249-2-21 Definition
- TrenchFET® Power MOSFET
- 100 % R_a and UIS Tested
- Compliant to RoHS Directive 2002/95/EC



APPLICATIONS

- DC/DC Conversion
 - Notebook System Power





Absolute Maximum Ratings T _A =25℃ unless otherwise noted					
Parameter		Symbol	Maximum	Units	
Drain-Source Voltage		V _{DS}	80	V	
Gate-Source Voltage		V_{GS}	±30	V	
Continuous Drain	T _A =25℃		3.5		
Current	T _A =70℃	I _D	2.9	Α	
Pulsed Drain Current ^C		I _{DM}	18		
Avalanche Current ^C		I _{AR}	16	A	
Repetitive avalanche energy L=0.1mH ^C		E _{AR}	12.8	mJ	
Power Dissipation ^B	T _A =25℃	В	2	W	
	T _A =70℃	$-P_{D}$	1.3	VV	
Junction and Storage Temperature Range		T _J , T _{STG}	-55 to 150	C	

Thermal Characteristics					
Parameter		Symbol	Тур	Max	Units
Maximum Junction-to-Ambient A	t ≤ 10s	D	48	62.5	€/W
Maximum Junction-to-Ambient AD	Steady-State	$R_{\theta JA}$	74	90	€\M
Maximum Junction-to-Lead	Steady-State	$R_{\theta JL}$	32	40	℃/W



Electrical Characteristics (T_J=25℃ unless otherwise noted)

Symbol	Parameter	Conditions	ı	Min	Тур	Max	Units
STATIC F	STATIC PARAMETERS						
BV _{DSS}	Drain-Source Breakdown Voltage	I _D =250μA, V _{GS} =0V		80			V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =80V, V _{GS} =0V	_J=55℃			1 5	μА
I _{GSS}	Gate-Body leakage current	V_{DS} =0V, V_{GS} = ±30V				100	nA
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}$ $I_{D}=250\mu A$		3.5	4.2	5	V
$I_{D(ON)}$	On state drain current	V_{GS} =10V, V_{DS} =5V		18			Α
R _{DS(ON)}	Static Drain-Source On-Resistance	V_{GS} =10V, I_D =3.5A	=125℃		62 113.0	75 135	mΩ
g _{FS}	Forward Transconductance	$V_{DS}=5V, I_{D}=3.5A$			15		S
V_{SD}	Diode Forward Voltage	I _S =1A,V _{GS} =0V			0.77	1	V
I _S	Maximum Body-Diode Continuous Current					2.5	Α
I _{SM}	Pulsed Body-diode Current ^C					18	Α
DYNAMIC	PARAMETERS						
C _{iss}	Input Capacitance		;	510	640	770	pF
C _{oss}	Output Capacitance	V _{GS} =0V, V _{DS} =40V, f=1MHz		28	40	52	pF
C _{rss}	Reverse Transfer Capacitance			12	20	30	pF
R_g	Gate resistance	V _{GS} =0V, V _{DS} =0V, f=1MHz		0.9	1.8	2.7	Ω
SWITCHI	NG PARAMETERS						
$Q_g(10V)$	Total Gate Charge	-V _{GS} =10V, V _{DS} =40V, I _D =3.5A		8	11	13	nC
$Q_g(4.5V)$	Total Gate Charge			4	5.5	7	
Q_{gs}	Gate Source Charge			4	5	6	nC
Q_{gd}	Gate Drain Charge			0.7	1.2	1.7	nC
t _{D(on)}	Turn-On DelayTime				7.2		ns
t _r	Turn-On Rise Time	V_{GS} =10V, V_{DS} =40V, R_L =8 Ω , R_{GEN} =3 Ω			2.2		ns
$t_{D(off)}$	Turn-Off DelayTime				17		ns
t _f	Turn-Off Fall Time				2		ns
t _{rr}	Body Diode Reverse Recovery Time	I_F =3.5A, dI/dt=300A/ μ s		14	20	26	ns
Q_{rr}	Body Diode Reverse Recovery Charge	I_F =3.5A, dI/dt=300A/ μ s		35	50	65	nC

A. The value of $R_{\theta JA}$ is measured with the device mounted on 1in^2 FR-4 board with 2oz. Copper, in a still air environment with T_A =25°C. The value in any given application depends on the user's specific board design.

B. The power dissipation P_D is based on $T_{J(MAX)}=150$ °C, using ≤ 10 s junction-to-ambient thermal resistance.

C. Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}=150$ °C. Ratings are based on low frequency and duty cycles to keep initial $T_J=25$ °C.

D. The $R_{\theta JA}$ is the sum of the thermal impedence from junction to lead $R_{\theta JL}$ and lead to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300 μ s pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-ambient thermal impedence which is measured with the device mounted on 1in² FR-4 board with



TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

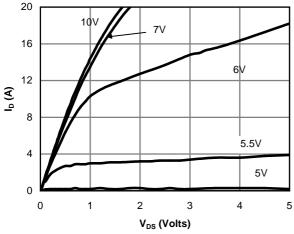


Fig 1: On-Region Characteristics (Note E)

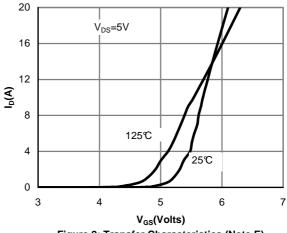


Figure 2: Transfer Characteristics (Note E)

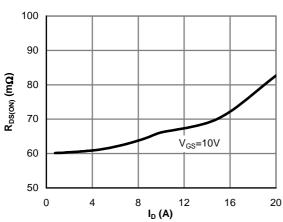
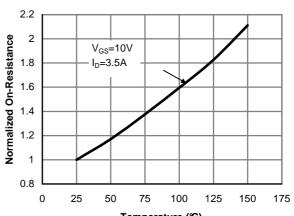


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)



Temperature (℃)
Figure 4: On-Resistance vs. Junction
Temperature (Note E)

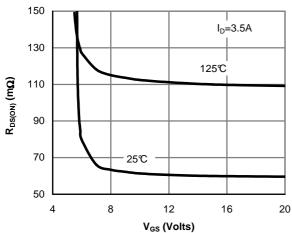


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

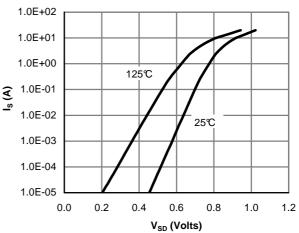


Figure 6: Body-Diode Characteristics (Note E)



TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

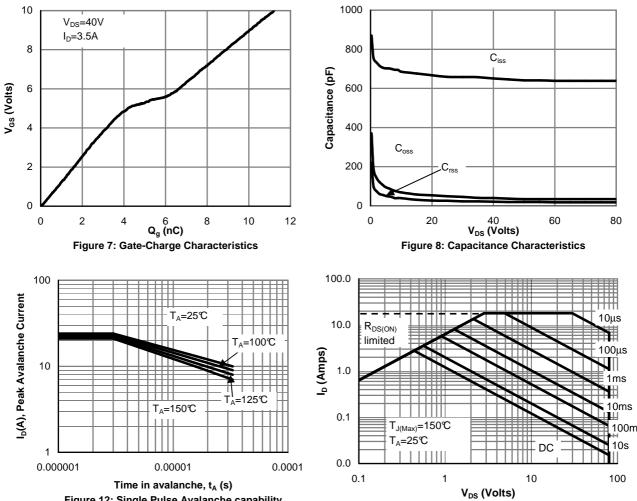
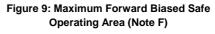


Figure 12: Single Pulse Avalanche capability



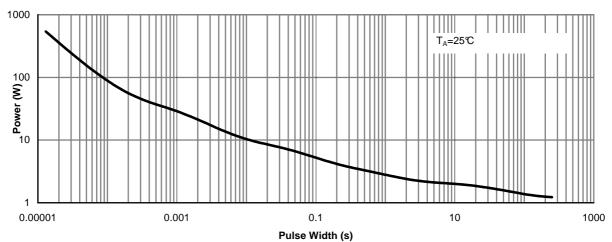


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note F)

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TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

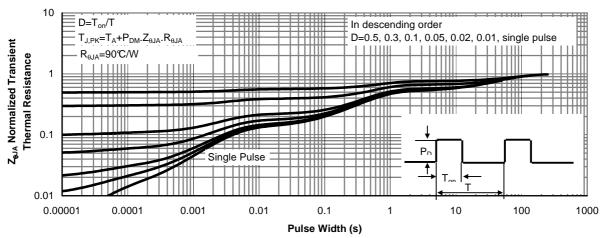
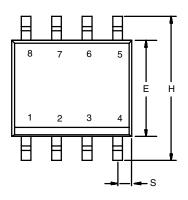
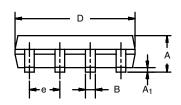


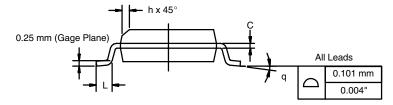
Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)



SOIC (NARROW): 8-LEAD JEDEC Part Number: MS-012







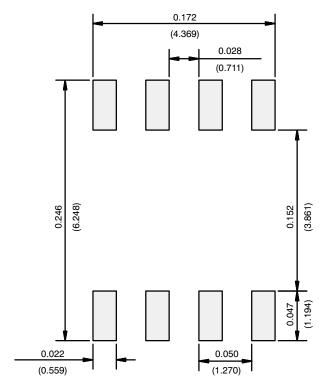
	MILLIM	MILLIMETERS INCHES				
DIM	Min	Max	Min	Max		
Α	1.35	1.75	0.053	0.069		
A ₁	0.10	0.20	0.004	0.008		
В	0.35	0.51	0.014	0.020		
С	0.19	0.25	0.0075	0.010		
D	4.80	5.00	0.189	0.196		
Е	3.80	4.00	0.150	0.157		
е	1.27 BSC		0.050	BSC		
Н	5.80	6.20	0.228	0.244		
h	0.25	0.50	0.010	0.020		
L	0.50	0.93	0.020	0.037		
q	0°	8°	0°	8°		
S	0.44	0.64	0.018	0.026		
ECN: C 06527 Pay I 11 San 06						

ECN: C-06527-Rev. I, 11-Sep-06

DWG: 5498



RECOMMENDED MINIMUM PADS FOR SO-8



Recommended Minimum Pads Dimensions in Inches/(mm)

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