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REV. 2.0

Freescale Semiconductor, Inc.

MC68HC705MC4

General Release Specification

January 29, 1997

CSIC System Design Group
Austin, Texas

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1.2 Introduction

The Freescale MC68HC705MC4 microcontroller is a low-cost M68HC05 Family EPROM microcontroller intended for use in industrial motor control and power supply applications. Features include a 2-channel, 8-bit, high-speed pulse-width modulator (PWM) module (including a commutation multiplexer for brushless permanent magnet motor control), a 6-input, 8-bit analog-to-digital (A/D) controller to accommodate analog feedback signals, and a serial communications interface (SCI) to support multi-controller networking.

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The MC68HC705MC4 is available in the 28-pin plastic dual in-line package (PDIP) and 28-pin small outline integrated circuit (SOIC) package.

1.3 Features

Features of the MC68HC705MC4 are listed below. Note that all timing is based on a 3-MHz bus.

- Low-Cost, HC05 Core Running at 3-MHz Bus Speed at V_{DD} = 5 V ± 10%
- 28-Pin Plastic Dual In-Line Package (PDIP), Small Outline Integrated Circuit (SOIC), or Windowed Ceramic Package with Low Electromagnetic Interference (EMI) Emission Pinout
- 3584 Bytes of User EPROM, Including Eight User Vectors of Two Bytes Each
- 176 Bytes of User RAM
- Dual-Channel, High-Speed PWM, Featuring:
  - 8-Bit Duty Cycle Resolution
  - Independent Prescaler Frequency Selection and Period Counters
  - Two Frequency Ranges, Eight Steps in Each:
    183 Hz to 23.4 kHz
    122 Hz to 15.6 kHz
  - Software Programmable PWM Polarity
  - Dual Software Controllable PWM Output Multiplexer, Each PWM to Three Input/Output (I/O)
- 8-Bit A/D Converter with Six Input Multiplexer
  - High and Low References
  - Conversion Rate = 10.7 µs

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- 16-Bit Timer with Two Input Captures **or** One Input Capture Plus One Output Compare
  - Resolution = 1.33 µs
  - Input Capture Active Edge Software Selectable as Rising or Falling
- 15-Stage, Multi-Function Core Timer with Timer Overflow, Real-Time Interrupt, and Watchdog
- Asynchronous Serial Communications Interface (SCI)
- 22 General-Purpose I/O Lines, Some Shared with Peripheral Functions
- One 8-Bit High Source Current I/O Port
  - 10 mA/Pin
  - 20 mA Maximum/Port
  - Port A
- One High-Sink Current 10 mA Output Pin, PB7
- Mask, Request, Acknowledge, Edge and Sensitivity (Edge- and Level-Sensitive or Edge-Sensitive Only) Control/Status Bits for IRQ Interrupt
- On-Chip Oscillator for Crystal/Ceramic Resonator
- Mask Selectable Computer Operating Properly (COP) Watchdog System
- Illegal Address Reset
- Steering Diode on $\overline{\text{RESET}}$ Pin to V_{DD}

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General Description

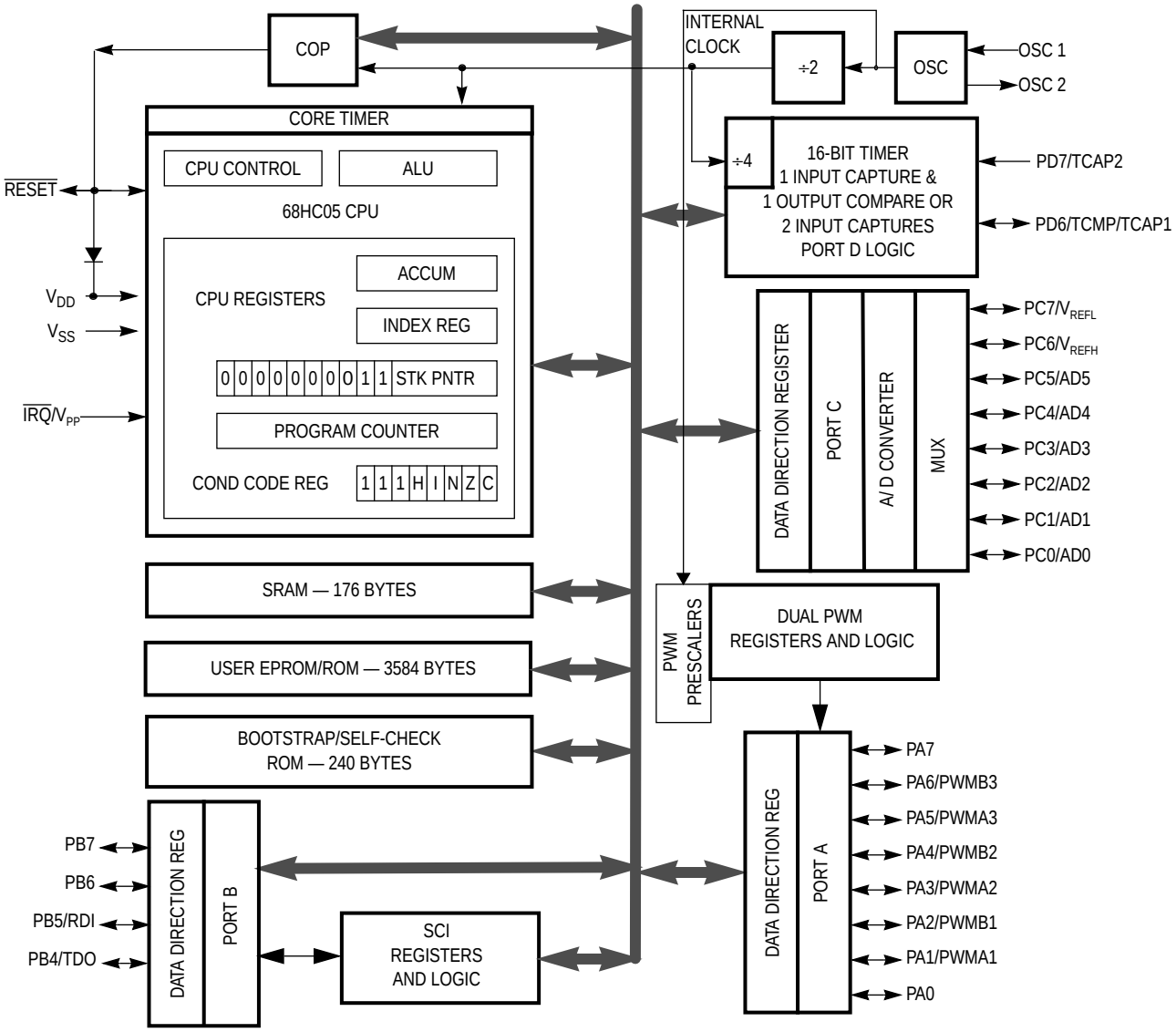

Figure 1-1. Block Diagram

NOTE: *A line over a signal name indicates an active low signal. For example, RESET is active high and $\overline{RESET}$ is active low.*

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1.4 Mask Options

There is one user selectable option on the MC68HC705MC4; the COP timer. This option is provided through a bit within a mask option register (MOR) in the EPROM device, which is located and programmed at $0F00. This option will be hard wired in the ROM-based device.

The ROM-based device (MC68HC05MC4) will offer these hard-wired options.

- COP Watchdog Timer Enabled with Option to Disable
- Stop Instruction Enabled with Option to Disable

These options are compatible with the typical application environment in which the device is expected to be used and will consequently allow the OTP devices to be used in production.

1.5 Functional Pin Description

The following paragraphs describe the functionality of each pin on the MC68HC705MC4 package (see **Figure 1-2** and **Figure 1-3**). Pins connected to subsystems which are described in other sections of this document provide a reference to the section instead of a detailed functional description.

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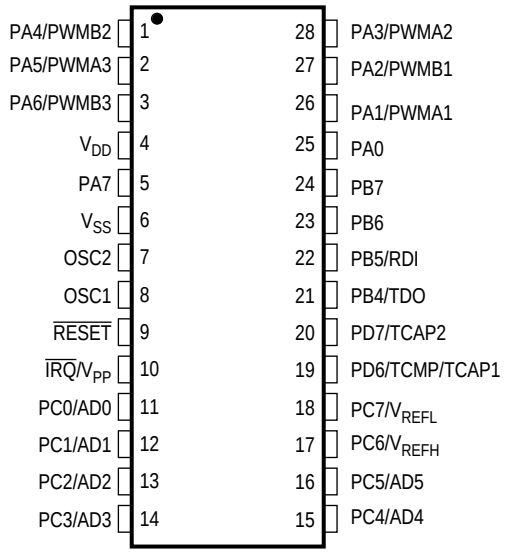

Figure 1-2. 28-Pin DIP Pinout

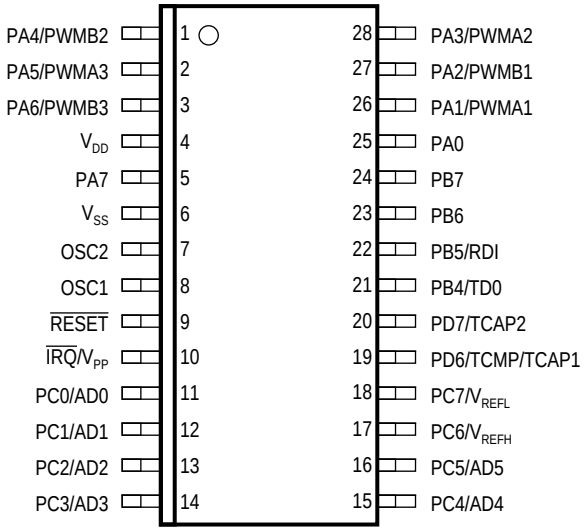

Figure 1-3. 28-Pin SOIC Assignments

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1.5.1 V_{DD} and V_{SS}

Power is supplied to the MCU through V_{DD} and V_{SS}. V_{DD} is connected to a regulated +5-volt supply and V_{SS} is connected to ground. These pins are located close to each other for low electromagnetic interference (EMI) emissions and optimal decoupling.

Very fast signal transitions occur on the MCU pins. The short rise and fall times place very high short-duration current demands on the power supply. To prevent noise problems, take special care to provide good power supply bypassing at the MCU. Use bypass capacitors with good high-frequency characteristics, and position them as close to the MCU as possible. Bypassing requirements vary, depending on how heavily the MCU pins are loaded.

1.5.2 OSC1 and OSC2

These pins provide control input for an on-chip clock oscillator circuit. A crystal, a ceramic resonator, or an external signal to these pins provides the system clock. The oscillator frequency is two times the internal bus rate.

The OSC1 and OSC2 pins can accept:

- A crystal as shown in **Figure 1-4(a)**
- A ceramic resonator as shown in **Figure 1-4(a)**
- An external clock signal as shown in **Figure 1-4(b)**

The frequency, f_{OSC}, of the oscillator or external clock source is divided by two to produce the internal bus clock operating frequency, f_{OP}. The oscillator cannot be turned off by software if the stop disable option is enabled via mask option.

1.5.2.1 Crystal

The circuit in **Figure 1-4(a)** shows a typical oscillator circuit for an AT-cut, parallel resonant crystal. Follow the crystal manufacturer's recommendations, as the crystal parameters determine the external component values required to provide maximum stability and reliable

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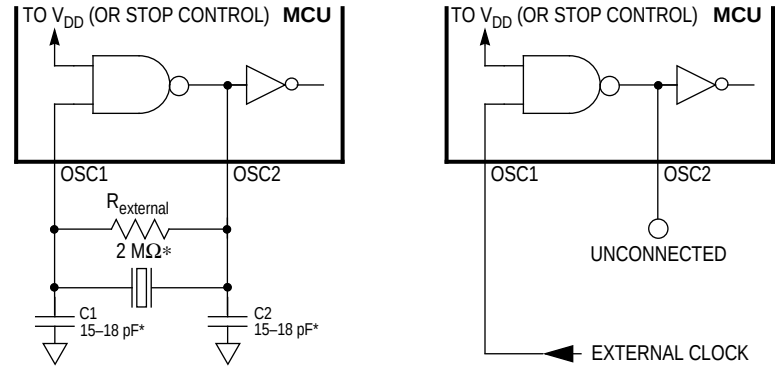
startup. The load capacitance values used in the oscillator circuit design should include all stray capacitances. Mount the crystal and components as close as possible to the pins for startup stabilization and to minimize output distortion. The ground return path for C1 and C2 should be as direct to V_{SS} (pin 6) as possible to minimize the oscillator loop area.



(a) Crystal or Ceramic Resonator Connections

(b) External Clock Source Connections

*Typical values shown. Follow the ceramic resonator manufacturer's recommendations for values of R, C1, and C2.

Figure 1-4. Oscillator Connections

1.5.2.2 Ceramic Resonator

In cost-sensitive applications, use a ceramic resonator in place of a crystal. Use the circuit in **Figure 1-4(a)** for a ceramic resonator and follow the resonator manufacturer's recommendations, as the resonator parameters determine the external component values required for maximum stability and reliable starting. The load capacitance values used in the oscillator circuit design should include all stray capacitances. Mount the resonator and components as close as possible to the pins for startup stabilization and to minimize output distortion.

1.5.2.3 External Clock

An external clock from another CMOS-compatible device can be connected to the OSC1 input, with the OSC2 input not connected, as shown in **Figure 1-4(b)**.

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1.5.3 $\overline{\text{RESET}}$

Driving this input low will reset the MCU to a known startup state. This pin is pulled low by internal resets. The $\overline{\text{RESET}}$ pin contains an internal Schmitt trigger to improve its noise immunity. Refer to **Section 5. Resets**.

1.5.4 PA0, PA1/PWMA1, PA2/PWMB1, PA3/PWMA2, PA4/PWMB2, PA5/PWMA3, PA6/PWMB3, and PA7

These eight I/O pins comprise port A and are shared with the PWM subsystem. The state of any pin is software programmable and all port A lines are configured as inputs during power-on or reset. All port A pins have high source current capability to simplify interfacing to external devices, such as small triacs. Refer to **Section 7. Input/Output Ports** and **Section 10. Pulse Width Modulator**.

1.5.5 PB4/TDO, PB5/RDI, PB6, and PB7

These four I/O pins comprise port B. Two pins are shared with the SCI communication subsystem. The state of any pin is software programmable and all port B lines are configured as inputs during power-on or reset. Refer to **Section 7. Input/Output Ports** and **Section 11. Serial Communications Interface**.

1.5.6 PC0:5/AD0:5, PC6/V_{REFH}, and PC7/V_{REFL}

These eight I/O pins comprise port C and are shared with the A/D converter subsystem. The state of any pin is software programmable and all port C lines are configured as inputs during power-on or reset. Refer to **Section 7. Input/Output Ports** and **Section 8. Analog Subsystem**.

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1.5.7 PD6/TCAP1/TCMP, PD7/TCAP2

These two I/O pins comprise port D and are shared with the 16-bit timer subsystem. PD7 is always an input. PD6 can be used as an input or output port if the TCAP1 interrupt is disabled and the TCAP1/TCMP bit is clear in the TCR. This is the state upon $\overline{\text{RESET}}$. Writes to PD7 have no effect. They may be read at any time, regardless of the mode of operation of the 16-bit timer. Refer to **Section 7. Input/Output Ports** and **Section 9. 16-Bit Timer**.

1.5.8 $\overline{\text{IRQ}}/V_{PP}$

This pin has two different choices of interrupt triggering sensitivity through the IRQ (maskable interrupt request) bit in the interrupt status and control register (ISCR). The choices are:

1. Edge-sensitive triggering only
2. Both edge-sensitive and level-sensitive triggering

In addition, the $\overline{\text{IRQ}}$ pin may be selected to trigger an interrupt on either the rising or falling edge of the $\overline{\text{IRQ}}$ pin signal through the EDGE bit in the ISCR.

The MCU completes the current instruction before it responds to the interrupt request.

If the option is selected to include level-sensitive triggering, the IRQ input requires an external resistor to V_{DD} for wire-OR operation.

The $\overline{\text{IRQ}}$ pin contains an internal Schmitt trigger as part of its input to improve noise immunity. Refer to **Section 4. Interrupts**.

This pin also is used to supply the MC68HC705MC4 EPROM array with the programming voltage.

NOTE: *If the voltage level applied to the $\overline{IRQ}$ pin exceeds V_{DD}, it can affect the MCU's mode of operation. See* **Section 6. Operating Modes***.*

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Section 2. Memory

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2.4 Bootstrap Mode Memory Map 29
2.5 I/O and Control Registers 29
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2.2 Introduction

The MC68HC705MC4 utilizes 12 address lines to access an internal memory space of 4 Kbytes. This memory space is divided into input/output (I/O) registers, RAM, and EPROM/ROM areas.

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2.3 User Mode Memory Map

When the MC68HC705MC4 is in the user mode, the 48 bytes of I/O registers, 176 bytes of RAM, 3584 bytes of user EPROM, 240 bytes of bootstrap ROM, and 16 bytes of user vectors EPROM are all active, as shown in **Figure 2-1**. The MOR resides at address $0F00 (first byte of the bootstrap code area) and the EPROM program register resides at $0026.

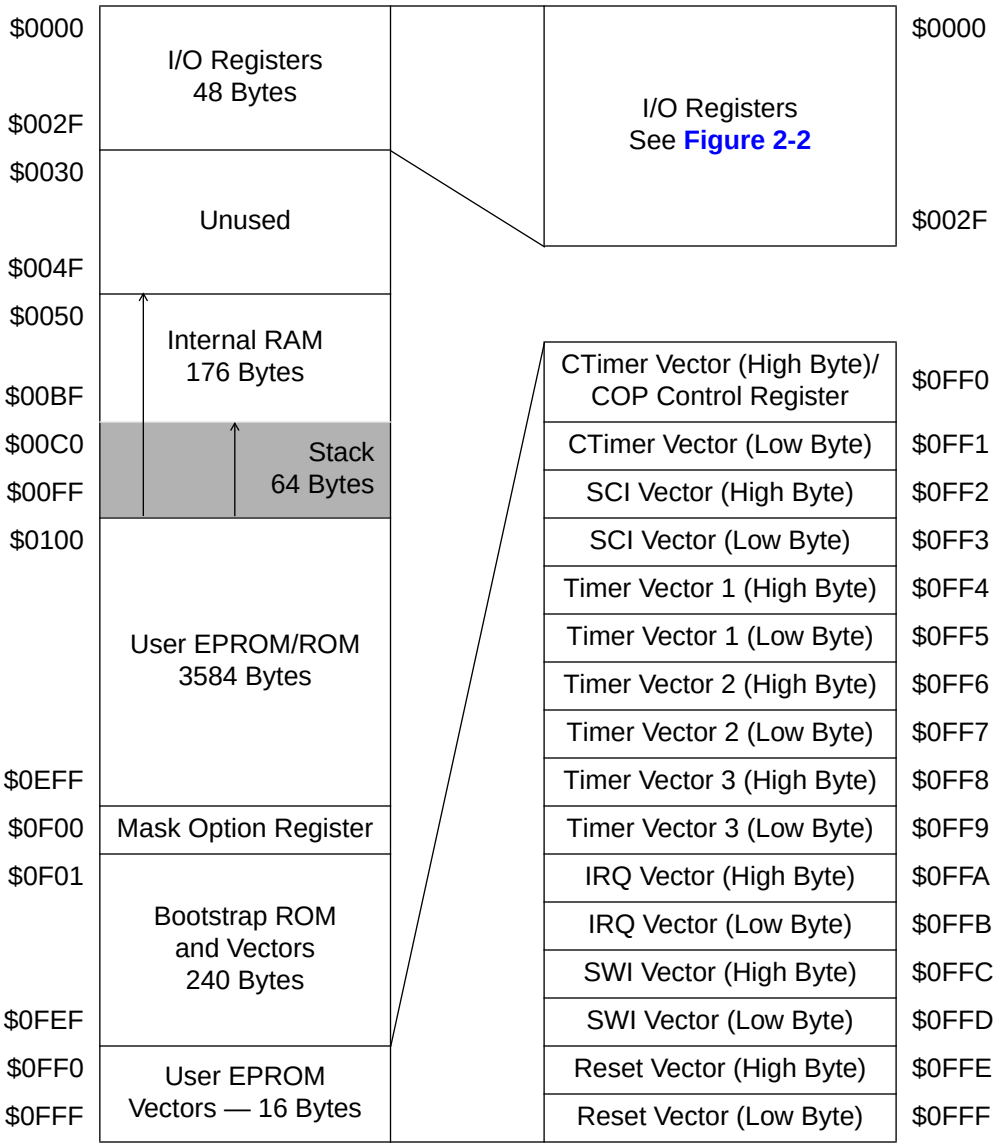

Figure 2-1. User Mode Memory Map

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2.4 Bootstrap Mode Memory Map

Memory space is identical to the user mode, as shown in **Figure 2-1**.

2.5 I/O and Control Registers

Figure 2-3, **Figure 2-4**, and **Figure 2-5** briefly describe the I/O and control registers according to their locations ($0000–$002F) as shown in **Figure 2-2**. Reading unimplemented bits will return unknown states, and writing unimplemented bits will be ignored.

Port A Data Register	$0000
Port B Data Register	$0001
Port C Data Register	$0002
Port D Data Register	$0003
Port A Data Direction Register	$0004
Port B Data Direction Register	$0005
Port C Data Direction Register	$0006
Port D Data Direction Register	$0007
Core Timer Control & Status Register	$0008
Core Timer Counter Register	$0009
SCI Baud Rate Register	$000A
SCI Control Register 1	$000B
SCI Control Register 2	$000C
SCI Status Register	$000D
SCI Data Register	$000E
IRQ Status and Control Register	$000F
PWMA-D Data Direct Register	$0010
PWMA-I Data Interlock Register	$0011
PWMB-D Data Direct Register	$0012

Figure 2-2. I/O and Control Registers Memory Map

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PWMB-I Data Interlock Register	$0013
PWM Control Register A	$0014
PWM Control Register B	$0015
PWM Control Rate Register	$0016
Timer Control Register	$0017
Timer Status Register	$0018
Input Capture2 Register MSB	$0019
Input Capture2 Register LSB	$001A
Input Capture1 Register MSB	$001B
Input Capture1 Register LSB	$001C
Output Compare Register MSB	$001D
Output Compare Register LSB	$001E
Reserved	$001F
Timer Register MSB	$0020
Timer Register LSB	$0021
Alternate Counter Register MSB	$0022
Alternate Counter Register LSB	$0023
A/D Converter Data Register	$0024
A/D Control & Status Register	$0025
EPROM Program Register*	$0026
PWM Update Register	$0027
Unimplemented	$0028 to $002F

* EPROM device only, unimplemented on ROM device

Figure 2-2. I/O and Control Registers Memory Map (Continued)

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Addr.	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
$0000	Port A Data Register	Read:	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0
		Write:								
$0001	Port B Data Register	Read:	PB7	PB6	PB5	PB4				
		Write:								
$0002	Port C Data Register	Read:	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
		Write:								
$0003	Port D Data Register	Read:	PD7	PD6						
		Write:								
$0004	Port A Data Direction Register	Read:	DDRA7	DDRA6	DDRA5	DDRA4	DDRA3	DDRA2	DDRA1	DDRA0
		Write:								
$0005	Port B Data Direction Register	Read:	DDRB7	DDRB6	DDRB5	DDRB4				
		Write:								
$0006	Port C Data Direction Register	Read:	DDRC7	DDRC6	DDRC5	DDRC4	DDRC3	DDRC2	DDRC1	DDRC0
		Write:								
$0007	Port D Data Direction Register	Read:		DDRD6						
		Write:								
$0008	Core Timer Control & Status Register	Read:	CTOF	RTIF	CTOIE	RTIE	0	0	RT1	RT0
		Write:								
$0009	Core Timer Counter Register	Read:	CTCR7	CTCR6	CTCR5	CTCR4	CTCR3	CTCR2	CTCR1	CTCR0
		Write:								
$000A	SCI Baud Rate Register	Read:	0	0	SCP1	SCP0	0	SCR2	SCR1	SCR0
		Write:								
$000B	SCI Control Register 1	Read:	R8		0	M	WAKE	0	0	0
		Write:		T8						
$000C	SCI Control Register 2	Read:	TIE	TCIE	RIE	ILIE	TE	RE	RWU	SBK
		Write:								
$000D	SCI Status Register	Read:	TDRE	TC	RDRF	IDLE	OR	NF	FE	0
		Write:								
$000E	SCI Data Register	Read:	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
		Write:								
$000F	IRQ Status and Control Register	Read:	IRQM	IRQS	EDGE	0	REQ	0	0	0
		Write:							ACK	

= Unimplemented

Figure 2-3. I/O and Control Registers $0000–$000F

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Addr.	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
$0010	PWMA Data Register (Effective) PWMA Data-Direct Register	Read: Write:	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
$0011	PWMA Data Register (Effective) PWMA Data-Interlock Register	Read: Write:	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
$0012	PWMB Data Register (Effective) PWMB Data-Direct Register	Read: Write:	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
$0013	PWMB Data Register (Effective) PWMB Data-Interlock Register	Read: Write:	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
$0014	PWM CTL-A Register (Effective) PWM CTL-A Register (Buffer)	Read: Write:	MEA	POLA	MSKA3	MSKA2	MSKA1	CSA3	CSA2	CSA1
$0015	PWM CTL-B Register (Effective) PWM CTL-B Register (Buffer)	Read: Write:	MEB	POLB	MSKB3	MSKB2	MSKB1	CSB3	CSB2	CSB1
$0016	PWM Rate Register (Effective) PWM Rate Register (Buffer)	Read: Write:	RA3	RA2	RA1	RA0	RB3	RB2	RB1	RB0
$0017	Timer Control Register	Read: Write:	ICIE2	ICIE1	TOIE	OCIE	TCMP/ TCAP1	IEDG1	IEDG2	OLVL
$0018	Timer Status Register	Read: Write:	ICF2	ICF1	TOF	OCF	0	0	0	0
$0019	Input Capture Register 2 MSB	Read: Write:	BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8
$001A	Input Capture Register 2 LSB	Read: Write:	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
$001B	Input Capture Register 1 MSB	Read: Write:	BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8
$001C	Input Capture Register 1 LSB	Read: Write:	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
$001D	Output Compare Register MSB	Read: Write:	BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8
$001E	Output Compare Register LSB	Read: Write:	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
$001F	Reserved	Read: Write:	R	R	R	R	R	R	R	R

= Unimplemented R = Reserved

Figure 2-4. I/O and Control Registers $0010–$0001F

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Addr.	Register Name		7	6	5	4	3	2	1	0
$0020	Timer Register MSB	Read:	BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8
		Write:								
$0021	Timer Register LSB	Read:	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
		Write:								
$0022	Alternate Counter Register MSB	Read:	BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8
		Write:								
$0023	Alternate Counter Register LSB	Read:	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
		Write:								
$0024	A/D Converter Data Register	Read:	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
		Write:								
$0025	A/D Status and Control Register	Read:	COCO	ADRC	ADON	0	CH3	CH2	CH1	CH0
		Write:								
$0026	EPROM Prog Register*	Read:							LATCH	EPGM
		Write:								
$0027	PWM Update Register	Read:	UPDATE A	UPDATE B						
		Write:								
$0028–$002F	Unimplemented	Read:								
		Write:								

= Unimplemented

* EPROM device only, unimplemented on ROM device

Figure 2-5. I/O and Control Registers $0020–$002F

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2.6 RAM

The user RAM consists of 176 bytes (including the stack) at locations $0050 through $00FF. The stack begins at address $00FF. The stack pointer can access 64 bytes of RAM from $00FF to $00C0.

NOTE: *Using the stack area for data storage or temporary work locations requires care to prevent it from being overwritten due to stacking from an interrupt or subroutine call.*

2.7 EPROM

There are 3584 bytes of user EPROM at locations $0100 through $0EFF and 16 additional bytes for user vectors at locations $0FF0 through $0FFF. The bootstrap ROM, MOR, and vectors are at locations $0F00 through $0FEF. The erased state of an EPROM cell is $FF. The erased state of the MOR byte is $00.

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Section 3. Central Processing Unit

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3.4 Index Register 36
3.5 Condition Code Register 36
3.6 Stack Pointer 37
3.7 Program Counter 38

3.2 Introduction

This section describes the five CPU registers. CPU registers are not part of the memory map.

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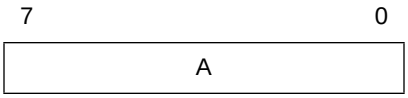
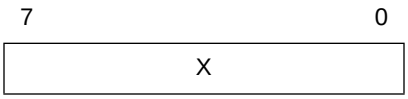
3.3 Accumulator

The accumulator (A) is a general-purpose 8-bit register used to hold operands and results of arithmetic calculations or data manipulations.



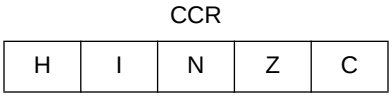
3.4 Index Register

The index register (X) is an 8-bit register used for the indexed addressing value to create an effective address. The index register also may be used as a temporary storage area.



3.5 Condition Code Register

The condition code register (CCR) is a 5-bit register in which four bits are used to indicate the results of the instruction just executed, and the fifth bit indicates whether interrupts are masked. These bits can be tested individually by a program, and specific actions can be taken as a result of their state. Each bit is explained in the following paragraphs.



H — Half Carry

This bit is set during ADD and ADC operations to indicate that a carry occurred between bits 3 and 4.

I — Interrupt

When this bit is set, timer and external interrupts are masked (disabled). If an interrupt occurs while this bit is set, the interrupt is latched and processed as soon as the interrupt bit is cleared.

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N — Negative

When set, this bit indicates that the result of the last arithmetic, logical, or data manipulation was negative.

Z — Zero

When set, this bit indicates that the result of the last arithmetic, logical, or data manipulation was zero.

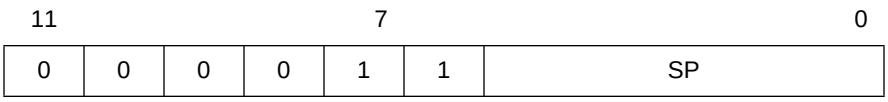
C — Carry/Borrow

When set, this bit indicates that a carry or borrow out of the arithmetic logical unit (ALU) occurred during the last arithmetic operation. This bit is also affected during bit test and branch instructions and during shifts and rotates.

3.6 Stack Pointer

The stack pointer (SP) contains the address of the next free location on the stack. During an MCU reset or the reset stack pointer (RSP) instruction, the stack pointer is set to location $00FF. The stack pointer is then decremented as data is pushed onto the stack and incremented as data is pulled from the stack.

When accessing memory, the six most significant bits are permanently set to 000011. These six bits are appended to the six least significant register bits to produce an address within the range of $00FF to $00C0. Subroutines and interrupts may use up to 64 (decimal) locations. If 64 locations are exceeded, the stack pointer wraps around and loses the previously stored information. A subroutine call occupies two locations on the stack; an interrupt uses five locations.



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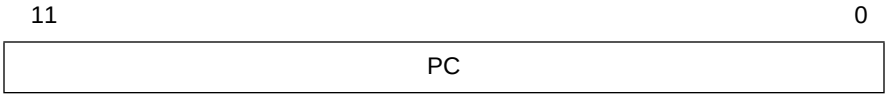
3.7 Program Counter

The program counter (PC) is a 12-bit register that contains the address of the next byte to be fetched.



NOTE: *The HC05 CPU core is capable of addressing a 64-Kbyte memory map. For this implementation, however, the addressing registers are limited to a 4-Kbyte memory map.*

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Section 4. Interrupts

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4.5.2.3 Timer Overflow Interrupt 46
4.5.3 Serial Communications Interface Interrupt 47
4.5.4 Core Timer Interrupt 47

4.2 Introduction

The MCU can be interrupted eight different ways:

1. Nonmaskable software interrupt instruction (SWI)
2. External asynchronous interrupt ($\overline{\text{IRQ}}$)
3. Input capture interrupt (TIMER)
4. Output compare interrupt (TIMER)
5. Timer overflow interrupt (TIMER)
6. Serial communications interrupt (SCI)
7. Core timer overflow interrupt (CTIMER)
8. Real-time interrupt (CTIMER)

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Interrupts cause the processor to save the register contents on the stack and to set the interrupt mask (I-bit) to prevent additional interrupts. Unlike RESET, hardware interrupts do not cause the current instruction execution to be halted, but are considered pending until the current instruction is completed.

When the current instruction is completed, the processor checks all pending hardware interrupts. If interrupts are not masked (I-bit in the condition code register is clear), and the corresponding interrupt enable bit is set, the processor proceeds with interrupt processing. Otherwise, the next instruction is fetched and executed. The SWI is executed the same as any other instruction, regardless of the I-bit state.

When an interrupt is to be processed, the CPU puts the register contents on the stack, sets the I-bit in the CCR, and fetches the address of the corresponding interrupt service routine from the vector table at locations $0FF0 through $0FFF. If more than one interrupt is pending when the interrupt vector is fetched, the interrupt with the highest vector location shown in **Table 4-1** will be serviced first.

Table 4-1. Vector Addresses for Interrupts and Reset

Register	Flag Name	Interrupts	CPU Interrupt	Vector Address
N/A	N/A	Reset	RESET	$0FFE–$0FFF
N/A	N/A	Software	SWI	$0FFC–$0FFD
ISCR	REQ	External Interrupt	IRQ	$0FFA–$0FFB
TSR	ICF2	Timer Input Capture 2	TIMER	$0FF8–$0FF9
TSR	ICF1	Timer Input Capture 1	TIMER	$0FF6–$0FF7
TSR	OCF	Timer Output Compare*	TIMER	$0FF4–$0FF5
TSR	TOF	Timer Overflow*	TIMER	$0FF4–$0FF5
SCSR	Various	SCI	SCI	$0FF2–$0FF3
CTCSR	CTOF	Core Timer Overflow*	CTIMER	$0FF0–$0FF1
CTCSR	RTIF	Core Timer Real Time*	CTIMER	$0FF0–$0FF1

* Vector is shared

An RTI instruction is used to signify when the interrupt software service routine is completed. The RTI instruction causes the CPU state to be recovered from the stack and normal processing to resume at the next

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instruction that was to be executed when the interrupt took place. **Figure 4-1** shows the sequence of events that occur during interrupt processing.

The interrupts fall into three categories: reset, software, and hardware.

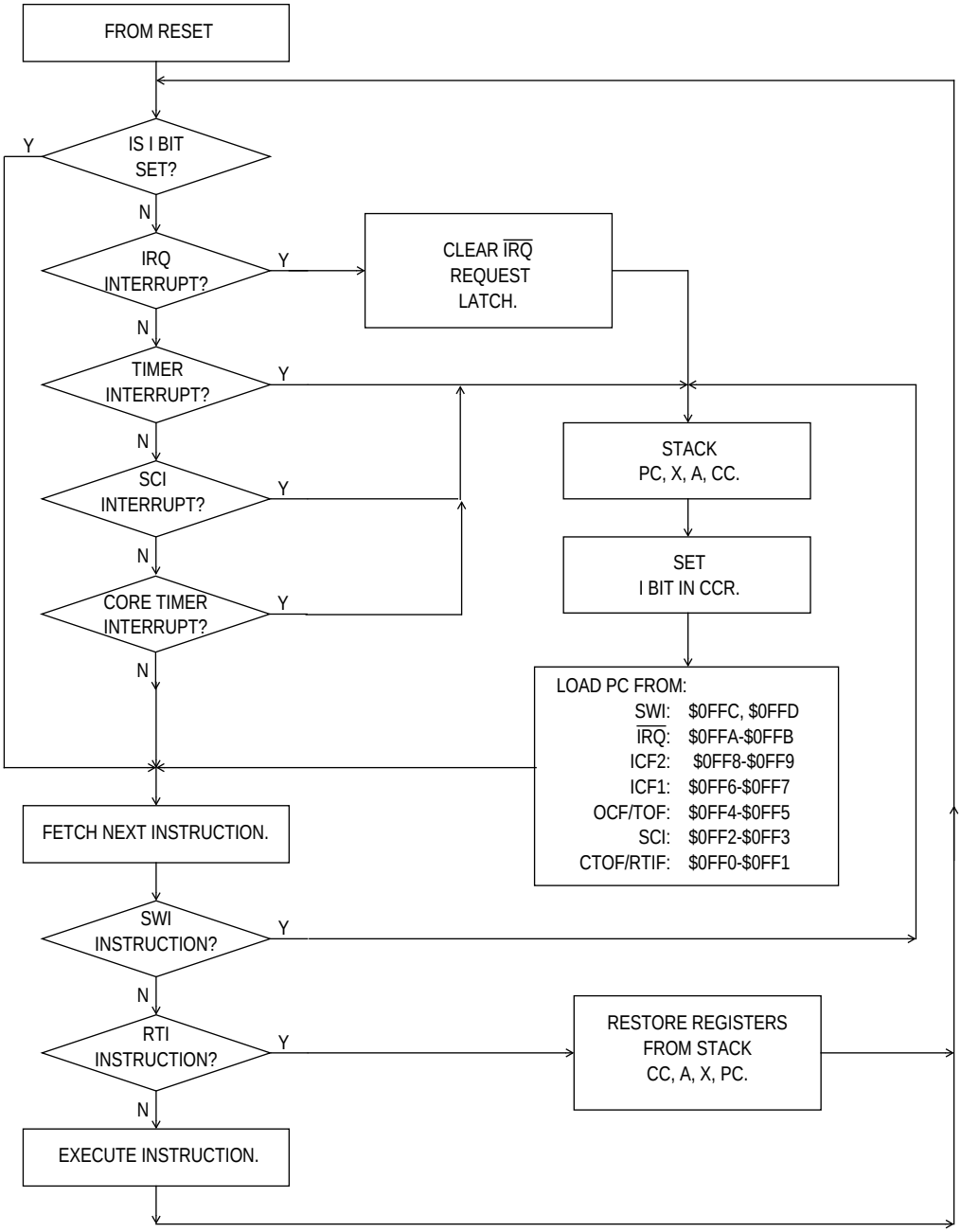

Figure 4-1. Interrupt Processing Flowchart

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4.3 Reset Interrupt Sequence

The reset function is not in the strictest sense an interrupt; however, it is acted upon in a similar manner as shown in **Figure 4-1**. A low level input on the $\overline{\text{RESET}}$ pin or internally generated RST signal causes the program to vector to its starting address which is specified by the contents of memory locations $0FFE and $0FFF. The I bit in the condition code register (CCR) is also set. The MCU is configured to a known state during this type of reset, as described in **Section 5. Resets**.

4.4 Software Interrupt

The software interrupt (SWI) is an executable instruction. It is also a nonmaskable interrupt since it is executed regardless of the state of the I bit in the CCR. As with any instruction, interrupts pending during the previous instruction will be serviced before the SWI opcode is fetched. The interrupt service routine address for the SWI instruction is specified by the contents of memory locations $0FFC and $0FFD.

4.5 Hardware Interrupts

All hardware interrupts are maskable by the I bit in the CCR. If the I bit is set, all hardware interrupts (internal and external) are disabled. Clearing the I bit enables the hardware interrupts. Four hardware interrupts are explained in the following sections.

4.5.1 External Interrupt

If the interrupt mask bit (I bit) of the CCR is set, all maskable interrupts (internal and external) are disabled. Clearing the I bit enables interrupts (subject to their individual interrupt enable control flag status). External interrupt (IRQ) now has an independent interrupt mask bit in the IRQ status and control register (ISCR) that also must be cleared to enable its corresponding interrupt.

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The interrupt mask bit operates by inhibiting the interrupt signal ***after*** the appropriate interrupt request latch. This feature allows the interrupt to be recognized and latched even if the mask is set.

When the IRQ input goes to the active level for at least one t_{ILIH}, a logic 1 is latched internally to signify an interrupt has been requested. When the MCU completes its current instruction, the interrupt latch is tested. If the interrupt latch contains a logic 1, and the interrupt mask bit (I bit) in the condition code register and the IRQ mask bit (IRQM) in the ISCR are both clear, then the MCU can begin the interrupt sequence. The state of the interrupt latch is reflected in the interrupt request bit (REQ) in the ISCR and is cleared automatically during interrupt processing. See **Figure 4-2**.

IRQ interrupt requests are acknowledged automatically and cleared during interrupt processing. It also may be cleared through software by setting the acknowledge bit in the ISCR. Setting this bit is a one-shot operation and will not affect subsequent interrupt operation. The action of clearing the acknowledge bit will clear the request bit. This allows the programmer the option to cancel spurious interrupts that occur while the interrupt mask bits are set. This may be necessary in systems where it is desirable to prevent redundant (ghost) entries to the interrupt service routine (where the interrupt mask is eventually cleared).

NOTE: *The IRQM is cleared (enabled) during reset, although no interrupts can occur until the interrupt mask bit of the CCR is cleared. The interrupt mask bit (I bit) of the CCR is set during reset. The interrupt request latches also are cleared during reset.*

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Address: $000F

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	IRQM	IRQS	EDGE	0	REQ	0	0	0
Write:							ACK	
Reset:	0	0	0	0	0	0	0	0

= Unimplemented

Figure 4-2. IRQ Status and Control Register (ISCR)

IRQM — IRQ Enable Mask

The IRQM bit is a read/write bit that will disable the IRQ interrupt when set. IRQM is cleared by reset.

1 = IRQ interrupt request disabled
0 = IRQ interrupt request enabled

IRQS — IRQ Sensitivity

The IRQS bit is a read/write bit that will select whether the IRQ interrupt is edge-sensitive only or both edge-sensitive and level-sensitive. IRQS is cleared by reset.

1 = Both edge-sensitive and level-sensitive
0 = Edge-sensitive only

EDGE — IRQ Active Edge Select

The EDGE bit is a read/write bit that allows the user to select which edge, rising or falling, of the signal at the $\overline{\text{IRQ}}$ pin will generate an interrupt. Both rising and falling edge sensitivity may be achieved in software by toggling the EDGE bit from within the IRQ service routine. EDGE is cleared by reset.

1 = Rising edge IRQ interrupt
0 = Falling edge IRQ interrupt

REQ — IRQ Interrupt Request

The REQ bit is a read-only bit. The IRQ interrupt request bit and latch are cleared during IRQ exception processing. Therefore, one external IRQ interrupt pulse can be latched and subsequently serviced as soon as the I bit is cleared. REQ will be cleared by reset.

1 = IRQ interrupt request pending
0 = No IRQ interrupt request pending

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ACK — IRQ Interrupt Request Acknowledge

This bit is write only and will always read as a logic 0. Writing a logic 1 to this bit will acknowledge the interrupt by clearing the corresponding interrupt request bit.

NOTE: *The use of separate request and acknowledge bits allows the safe use of read-modify-write instructions (for example, BSET and BCLR) on the ISCR register.*

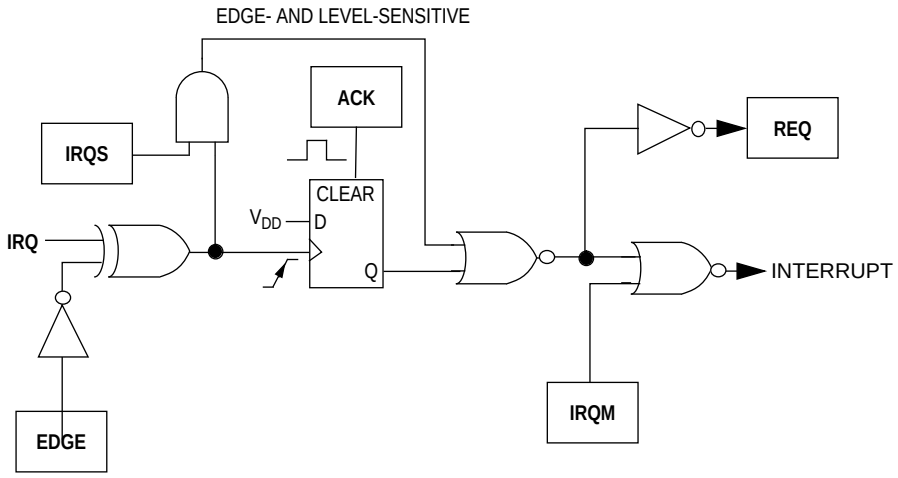

Figure 4-3. Interrupt Hardware Structure

NOTE: *When the edge- and level-sensitive mask option is selected, the voltage applied to the $\overline{IRQ}$ pin must return to the inactive state before the RTI instruction in the interrupt service routine is executed. If the $\overline{IRQ}$ pin remains in the active level, the interrupt service routine will be re-entered after the RTI is executed. Setting the ACK bit will have no effect under these circumstances.*

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4.5.2 Timer Interrupts

The following paragraphs describe the timer interrupts.

4.5.2.1 Input Capture Interrupts

The input capture interrupts are generated by the 16-bit timer as described in **Section 9. 16-Bit Timer**. The input capture interrupt flags are located in the timer status register (TSR) and the corresponding enable bits can be found in the timer control register (TCR). The interrupt service routine addresses are specified by the contents of memory locations $0FF8 and $0FF9 for input capture 2 and by the contents of memory locations $0FF6 and $0FF7 for input capture 1.

4.5.2.2 Output Compare Interrupt

The output compare interrupt is generated by the 16-bit timer, as described in **Section 9. 16-Bit Timer**. The output compare interrupt flag is located in register TSR and its corresponding enable bit can be found in register TCR. The interrupt service routine address is specified by the contents of memory locations $0FF4 and $0FF5.

NOTE: *The output compare interrupt is not available when the TCMP/TCAP1 timer channel is configured for input capture. See **9.4 Output Compare**.*

4.5.2.3 Timer Overflow Interrupt

The timer overflow interrupt is generated by the 16-bit timer as described in **Section 9. 16-Bit Timer**. The timer overflow interrupt flag is located in register TSR and its corresponding enable bit can be found in register TCR. The I bit in the CCR must be clear for the timer overflow interrupt to be enabled. This internal interrupt will vector to the interrupt service routine located at the address specified by the contents of memory locations $0FF4 and $0FF5. The timer overflow and the output compare function share the same interrupt vector, thus requiring the user to poll interrupt request flags.

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4.5.3 Serial Communications Interface Interrupt

Five different serial communications interface (SCI) interrupt flags that cause an SCI interrupt whenever they are set and enabled. The interrupt flags are in the SCI status register (SCSR), and the enable bits are in the SCI control register 2 (SCCR2). Any of these interrupts will vector to the same interrupt service routine, located at the address specified by the contents of memory location $0FF2 and $0FF3. See **Section 11. Serial Communications Interface**.

4.5.4 Core Timer Interrupt

Two different core timer (CTIMER) interrupt flags cause a CTIMER interrupt whenever they are set and enabled. The interrupt flags and enable bits are located in the CTIMER control and status register (CTCSR). Any of these interrupts will vector to the same interrupt service routine, located at the address specified by the contents of memory location $0FF0 and $0FF1. See **Section 12. Core Timer**.

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Interrupts

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Section 5. Resets

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5.4.3 Computer Operating Properly Reset 51

5.2 Introduction

The MCU can be reset from four sources: one external input and three internal reset conditions. The $\overline{\text{RESET}}$ pin is an input with a Schmitt trigger as shown in **Figure 5-1**. The CPU and all peripheral modules will be reset by the RST signal which is the logical OR of internal reset functions and is clocked by the internal bus clock. The $\overline{\text{RESET}}$ pin will also be pulled low by internal reset for four bus cycles.

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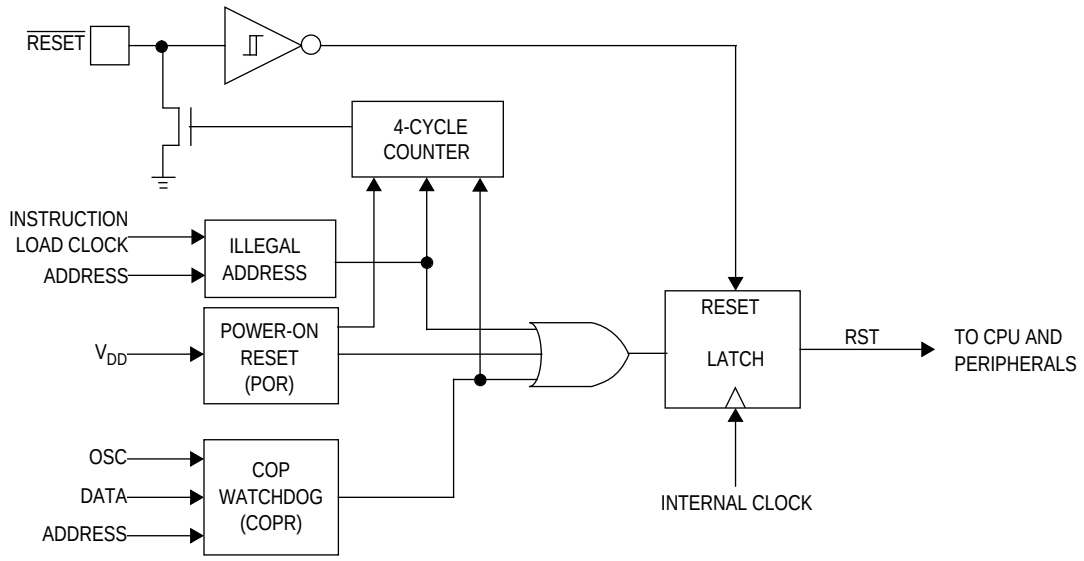

Figure 5-1. Reset Block Diagram

5.3 External Reset

The $\overline{\text{RESET}}$ input is the only external reset and is connected to an internal Schmitt trigger. The external reset occurs whenever the $\overline{\text{RESET}}$ input is driven below the lower threshold and remains in reset until the $\overline{\text{RESET}}$ pin rises above the upper threshold. The upper and lower thresholds are given in **Section 14. Electrical Specifications**.

5.4 Internal Resets

The three internally generated resets are the illegal address, the initial power-on reset (POR) function, and the computer operating properly (COP) watchdog timer function.

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5.4.1 Illegal Address Reset

When an opcode fetch occurs at an address that is not in the RAM or ROM/EPROM, the part automatically resets. The part will also reset when an opcode fetch inadvertently occurs at an address within the bootstrap ROM while the device is in user mode.

5.4.2 Power-On Reset

An internal reset is generated on power-up to allow the internal clock generator to stabilize. The power-on reset is strictly for power turn-on conditions and should not be used to detect a drop in the power supply voltage. There is a 4064 internal processor clock cycle (t_{cyc}) oscillator stabilization delay after the oscillator becomes active. If the $\overline{\text{RESET}}$ pin is active at the end of this 4064-cycle delay, the MCU will remain in the reset condition until $\overline{\text{RESET}}$ goes inactive.

The POR will generate the RST signal and reset the MCU. If any other reset function is active at the end of this 4064-internal clock cycle delay, the RST signal will remain active until the other reset condition(s) end. During POR, $\overline{\text{RESET}}$ will be driven low for four cycles. Although the external reset pulse is short, it is recommended that the user tie $\overline{\text{RESET}}$ to V_{DD} through a 1 kΩ resistor (not directly).

5.4.3 Computer Operating Properly Reset

When the COP watchdog timer is enabled (by mask option), the internal COP reset is generated automatically by a time-out of the COP watchdog timer. This timer is implemented as part of the core timer. See **Section 12. Core Timer**. The COP watchdog counter is cleared by writing a logical 0 to bit 0 at location $0FF0.

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The COP register is shared with the most significant byte (MSB) of the core timer interrupt vector as shown in **Figure 5-2**. Reading this location will return the MSB of the core timer interrupt vector. Writing a logic 0 to this location will clear the COP watchdog timer.

Address: $0FF0

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	U	U	U	U	U	U	U	U
Write:								COPR
Reset:	0	0	0	0	0	0	0	0

= Unimplemented U = Undefined

Figure 5-2. COP Watchdog Timer Register

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Section 6. Operating Modes

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6.2 Introduction

The MC68HC705MC4 has two modes of operation that affect the pinout and architecture of the MCU: user mode and bootloader (EPROM self-programming) mode. The user mode normally will be used, and the bootloader mode is required for the special needs of EPROM programming.

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The conditions required to enter each mode are shown in **Table 6-1**. The mode of operation is determined by:

1. The voltages on the $\overline{IRQ}$ and PD7/TCAP2 pins on the rising edge of the external $\overline{RESET}$ pin.
2. The subsequent rising edge of $\overline{RESET}$ after an internal reset pulls the $\overline{RESET}$ pin low.

Table 6-1. Operating Mode Conditions after Reset

$\overline{RESET}$ Pin	$\overline{IRQ}/V_{PP}$	PD7/TCAP2	Mode
	V_{SS} to V_{DD}	V_{SS} to V_{DD}	User
	V_{PP}	V_{DD}	Bootloader

6.3 User Mode

The user mode allows the MCU to function as a self-contained microcontroller, with maximum use of the pins for on-chip peripheral functions. All address and data activity occurs within the MCU and are not available externally. User mode is entered on the rising edge of $\overline{RESET}$ if the $\overline{IRQ}$ pin is within the normal operating voltage range.

In the user mode, port A shares six of its eight input/output (I/O) lines with the dual channel pulse-width modulator (PWM) subsystem. Port B shares two of its four I/O lines with the serial communications interface (SCI) subsystem. Port C shares all of its 8-bit I/O lines with the analog-to-digital (A/D) subsystem. Port D shares its two port lines with the 16-bit timer subsystem.

The pinout for user mode is shown in **Figure 1-2** and **Figure 1-3**.

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6.4 Bootloader Mode

Bootloader mode is entered upon the rising edge of $\overline{\text{RESET}}$ if the $\overline{\text{IRQ}}/V_{PP}$ pin is at V_{PP} and the PD7/TCAP2 pin is at logic 1. The bootloader code resides in ROM between $0F01 and $0FEF. This program handles copying of user code from an external EPROM or host computer into the on-chip EPROM. **Figure 6-1** shows the timing required to interface the device being programmed to a host. The bootloader performs one programming pass at t_{EPGM} per byte. When programming is complete, the bootloader code then performs a verify pass.

NOTE: *The external user code addresses must correspond directly with the internal EPROM addresses.*

6.4.1 Bootloader Functions

Two pins are used to select various bootloader functions. These pins are PC2 and PC3. In addition, PC1 must be connected to V_{SS}. PC0 is a SYNC pin, which is used to synchronize the MCU to an off-chip source driving data to be programmed into the MCU as shown in **Figure 6-1**. Two other pins, PC6 and PC7 are used to drive the PROG LED and the VERF LED respectively. The PC2 and PC3 configurations required to enter the programming modes are shown in **Table 6-1**.

NOTE: *PC0 must be connected to V_{SS} through a resistor.*

Table 6-2. Bootloader Functions

PC2	PC3	Mode
1	1	Program/Verify
1	0	Verify Only
0	0	Dump EPROM

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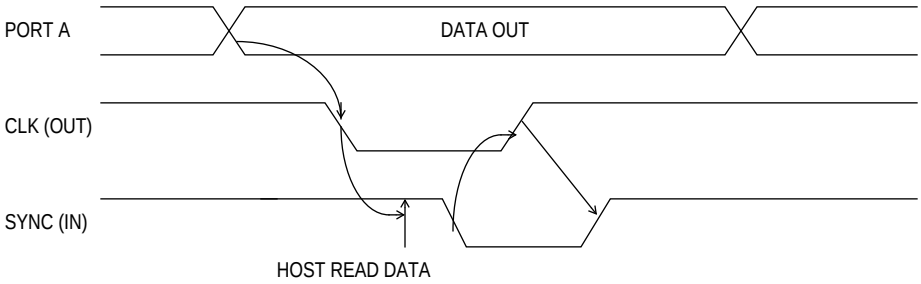
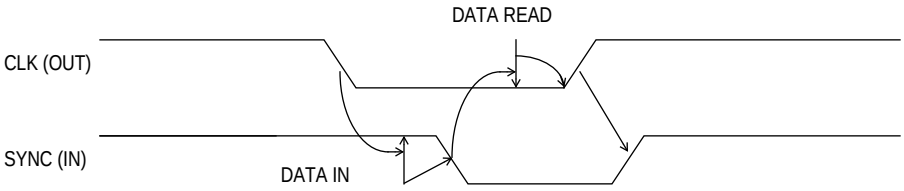
Operating Modes

The bootloader uses an external 12-bit counter to address the external memory device containing the code to be copied. This counter requires a clock and a reset function and can address up to 4 Kbytes of memory.



(a) Dump EPROM Interface to a Host



(b) Program/Verify Interface to a Host

Figure 6-1. Programmer Interface to Host

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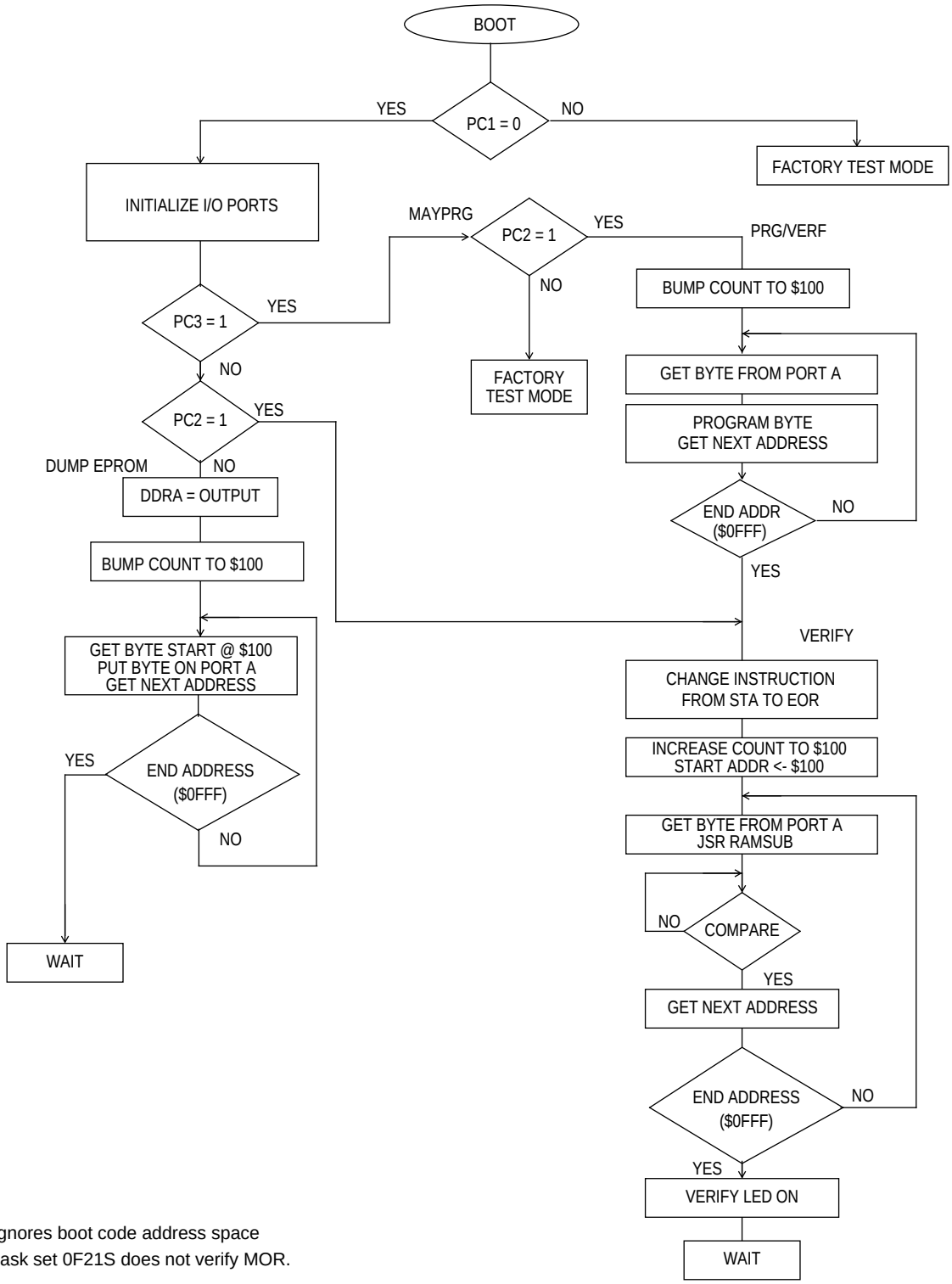

*Ignores boot code address space
Mask set 0F21S does not verify MOR.

Figure 6-2. Bootloader Flowchart

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Operating Modes

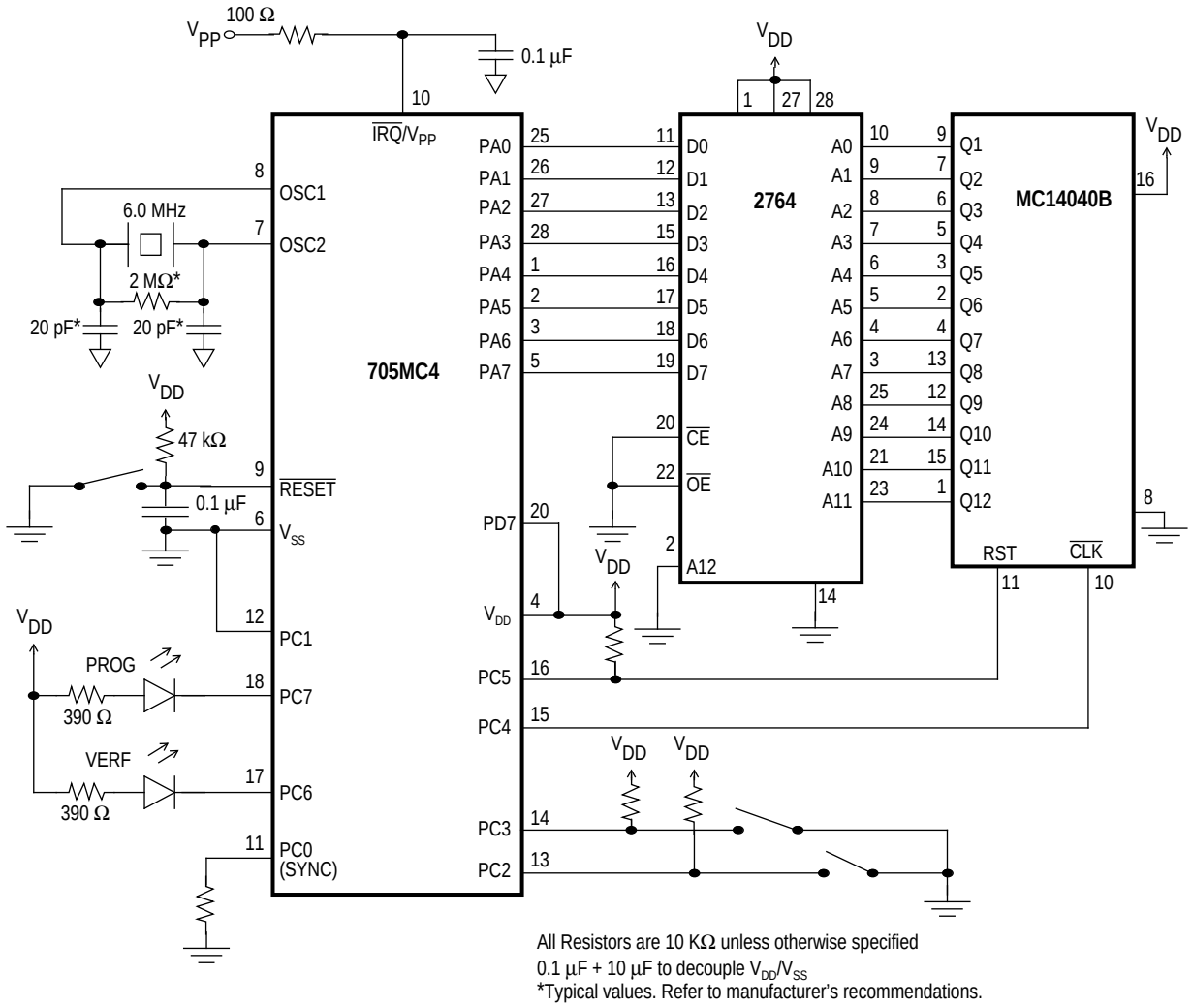

Figure 6-3. Programming Circuit

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6.4.2 EPROM Programming Register

This register is used to program the EPROM array. To program a byte of EPROM, set LATCH, then write data to the desired address, and set EPGM for t_{EPGM}.

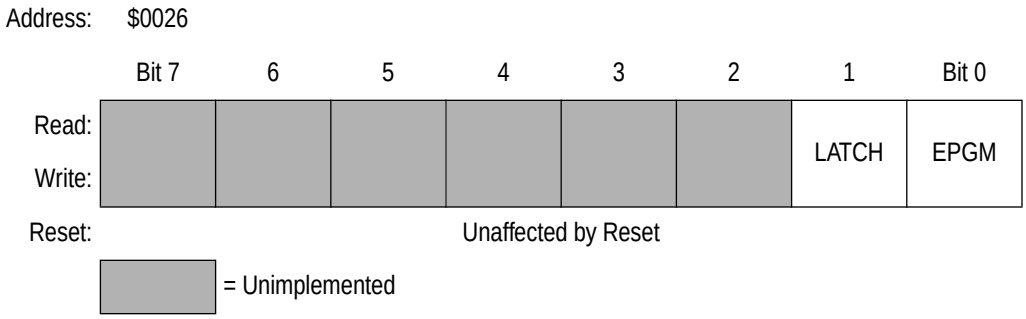

Figure 6-4. EPROM Programming Register (EPGM)

LATCH — EPROM Latch Control

The LATCH bit is a read/write bit. When set, the address and data buses are latched when a write to EPROM is done. EPROM cannot be read if LATCH = 1.

1 = EPROM address and data bus configured for programming
0 = EPROM address and data bus configured for normal reads

EPGM — EPROM Program Control

The EPGM bit may be read or cleared at any time. It may only be set if LATCH = 1. If LATCH = 0, the EPGM is cleared automatically. LATCH and EPGM must be set sequentially. They cannot both be set on the same write.

1 = Programming power switched on to the EPROM array
0 = Programming power switched off the EPROM array

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6.4.3 Mask Option Register

This register is latched upon RESET and at regular intervals as determined by the COP timeout period. The register is an EPROM byte located at $0F00 and holds the option bit for COP disable/enable.

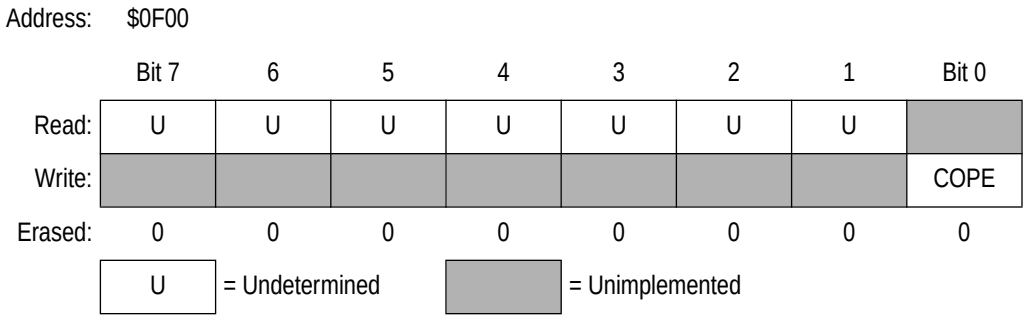

Figure 6-5. Mask Option Register (MOR)

COPE — COP Enable/Disable

1 = The COP is enabled.

0 = (erased state) The COP is disabled.

NOTE: *The COPE bit is not readable.*

6.5 Low-Power Mode

MC68HC705MC4 is capable of running in a low-power mode in each of its configurations. The WAIT instruction reduces the power required for the MCU by stopping various internal clocks and/or the on-chip oscillator. The WAIT instruction is not normally used if the COP watchdog timer is enabled. Execution of the stop instruction will take the effect of a NOP. The flow of wait mode is shown in **Figure 6-6**.

NOTE: *The ROM option will include the STOP functions.*

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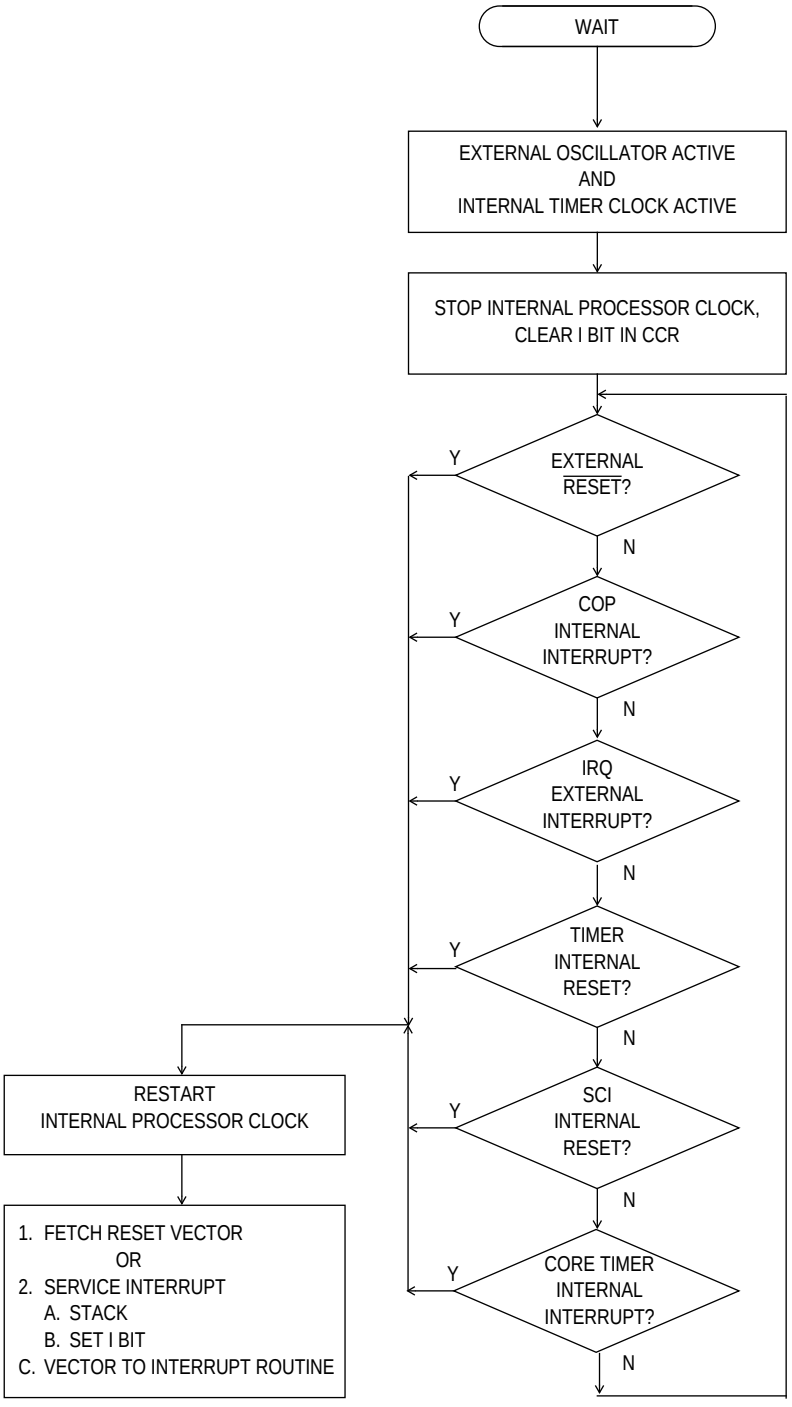

Figure 6-6. Wait Flowchart

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6.6 WAIT Instruction

The WAIT instruction places the MCU in a low-power mode. In wait mode, the bus clock is halted, suspending all processor and internal bus activity but the timer. COP, ADC, PWM, and SCI subsystems remain active. To save more power, the user may optionally disable each individual subsystem through software before entering wait mode. Execution of the WAIT instruction automatically clears the I bit in the condition code register, enabling the $\overline{\text{IRQ}}$ external interrupt. All other registers, memory, and input/output lines remain in their previous state unless modified by an active peripheral.

If the 16-bit timer interrupt is enabled, it will cause the processor to exit wait mode and resume normal operation. The 16-bit timer may be used to generate a periodic exit from wait mode. The wait mode may also be exited when an $\overline{\text{IRQ}}$ external interrupt, SCI interrupt, or $\overline{\text{RESET}}$ occurs.

6.7 COP Watchdog Timer Considerations

The COP watchdog timer is active in single-chip mode when selected by mask option. The COP watchdog timer should be disabled for applications that will use the wait mode with time periods that will exceed the COP timeout period.

COP watchdog timer interactions are summarized in **Table 6-3**.

Table 6-3. COP Watchdog Timer Recommendations

IF the following conditions exist during WAIT period:	THEN the COP watchdog timer should be:
WAIT period *less than* COP time-out	Enable or disable COP via Mask Option
WAIT period *more than* COP time-out	Disable COP via Mask Option
any length WAIT period	Disable COP via Mask Option

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Section 7. Input/Output Ports

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7.2 Introduction

In the user mode, 22 bidirectional input/output (I/O) lines are arranged as two 8-bit I/O ports (port A and port C), one 4-bit I/O port (port B), and one 2-bit port (port D). These ports are programmable as either inputs or outputs, except port D bit 7 (input only), under software control of the data direction registers (DDRs).

NOTE: *Enabling any module that is shared with a port could corrupt port data written to the port before or during the time that module is enabled.*

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7.3 Port A

Port A is an 8-bit bidirectional port that shares PA1–PA6 with the pulse width modulator (PWM) subsystem. (See **Figure 7-1**.) The port A data register is located at address $0000 and its data direction register (DDR) is located at address $0004. Reset does not affect the data registers, but clears the DDRs, thereby setting all of the port pins to input mode. Writing a 1 to a DDR bit sets the corresponding port pin to output mode. PA1–PA6 may be used for general I/O applications when the PWM subsystem is disabled. PA0–PA7 feature larger P-channel output devices and are capable of sourcing more current than a standard port (refer to **Section 14. Electrical Specifications**).

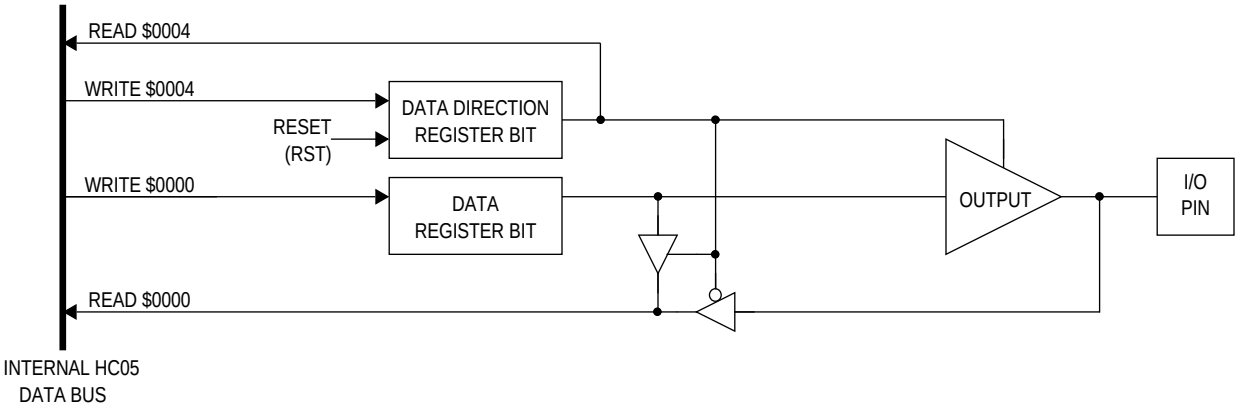

Figure 7-1. Port A I/O Circuitry

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7.4 MCU Line Interface Recommendations

It is expected that some applications appropriate to the MC68HC705MC4 will be required to determine the presence of line (mains) voltage using the MCU. A low-cost MCU line interface is shown in **Figure 7-2**. PA7 has been intentionally located between V_{DD} and V_{SS} to provide a lowest possible impedance path for the injected currents in particular fast transients. Although any I/O port will function in this manner, it is recommended that only PA7 be used for such an interface. The positive and negative excursions of the input voltage relative to the neutral return are clamped between V_{SS} and V_{DD} using the internal parasitic input diodes. The series resistor limits the injected currents to the specified value. (Refer to **Section 14. Electrical Specifications**.) The resistor value must be calculated based upon maximum expected transient voltage levels (for example, not line peak values). Care should be taken to ensure parasitic series resistor and PCB capacitance will not couple transients to the MCU input. Additional filtering is also highly recommended to help prevent EMC and electrical overstress (EOS) problems.

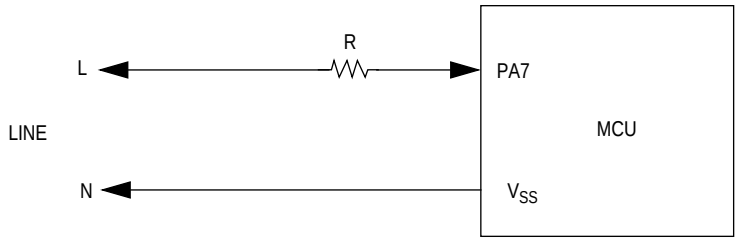

Figure 7-2. Line Interface Circuitry

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7.5 Port B

Port B is a 4-bit bidirectional port that can share pins PB4–PB5 with the SCI subsystem. Port B data register is located at address $0001 and its data direction register (DDR) is located at address $0005. Reset does not affect the data registers, but clears the DDRs, thereby setting all of the port pins to input mode. Writing a 1 to a DDR bit sets the corresponding port pin to output mode. (See **Figure 7-3**.)

PB7 features a larger n-channel output device and can, therefore, sink more current than a standard port. (Refer to **Section 14. Electrical Specifications**.)

PB4–PB5 may be used for general I/O applications when the SCI subsystem is disabled. When the serial communications interface (SCI) subsystem is enabled, port B registers are still accessible to software. Writing to either of the port B registers could corrupt the SCI data. See **Section 11. Serial Communications Interface** for a discussion of the SCI subsystem.

PB6–PB7 remain as I/O pins when the SCI subsystem is enabled.

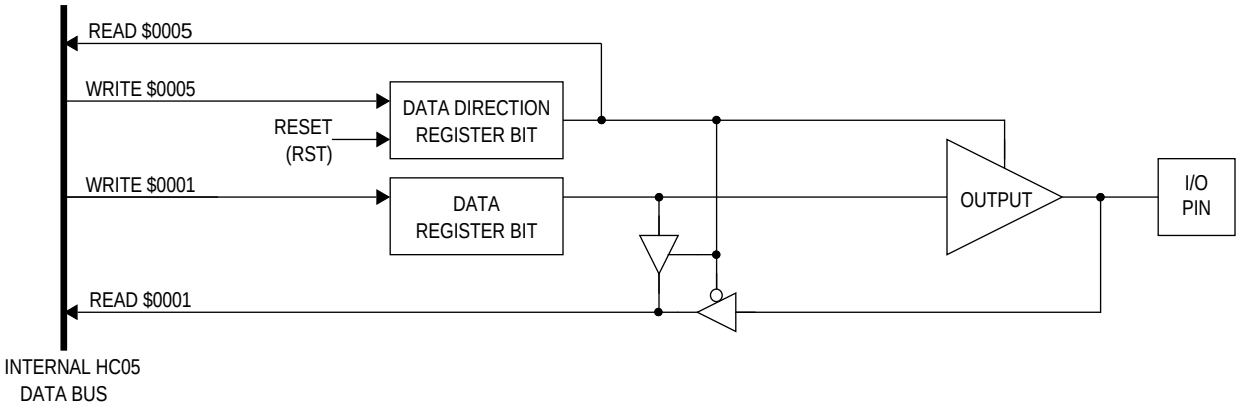

Figure 7-3. Port B I/O Circuitry

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7.6 Port C

Port C is an 8-bit bidirectional port that has shared pins with the analog-to-digital (A/D) subsystem. The port C data register is located at address $0002 and its data direction register (DDR) is located at address $0006. Reset does not affect the data registers, but clears the DDRs, thereby setting all of the port pins to input mode. Writing a 1 to a DDR bit sets the corresponding port pin to output mode. (See **Figure 7-4**.)

The ADON bit in register ADSC is used to enable/disable the A/D subsystem. Port C may be used for general I/O applications when the A/D subsystem is disabled or when all A/D input channels are not required. Unselected channels revert to general-purpose I/O. See **Section 8. Analog Subsystem**.

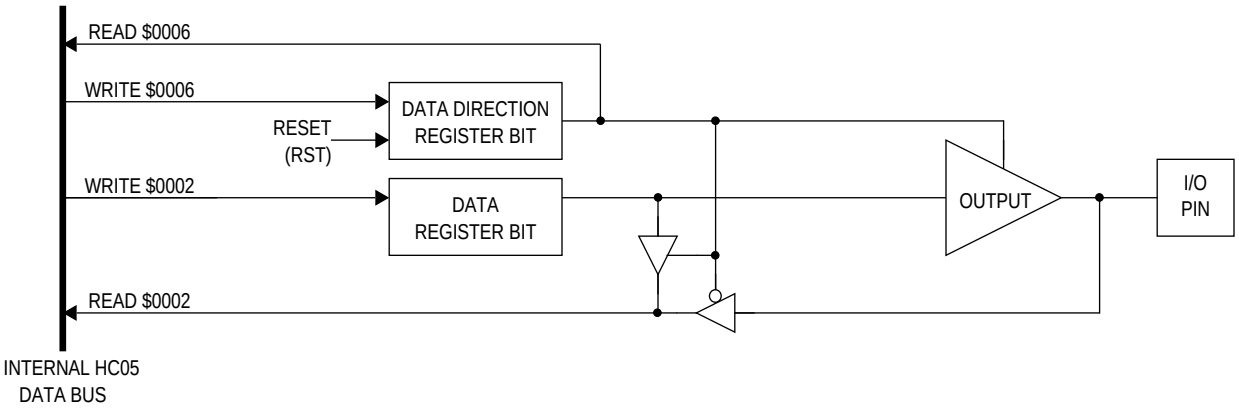

Figure 7-4. Port C I/O Circuitry

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7.7 Port D

Port D is a 2-bit port. PD7 and PD6 are shared with the 16-bit timer. PD6 is a bidirectional I/O pin but PD7 is an input-only pin. The port D data register is located at address $0003 and its data direction register (DDR) is located at address $0007. Reset clears the DDR, setting PD6 to an input but does not affect the data registers. (See **Figure 7-5**.)

PD6 may be used for general I/O applications when the timer subsystem is disabled. PD7 may be used as a general-purpose input when the timer subsystem is disabled. When the timer subsystem is enabled, port D registers are still accessible to software. Writing to either of the port D registers with the timer enabled could interfere with timer operation. See **Section 9. 16-Bit Timer** for a discussion of the timer subsystem.

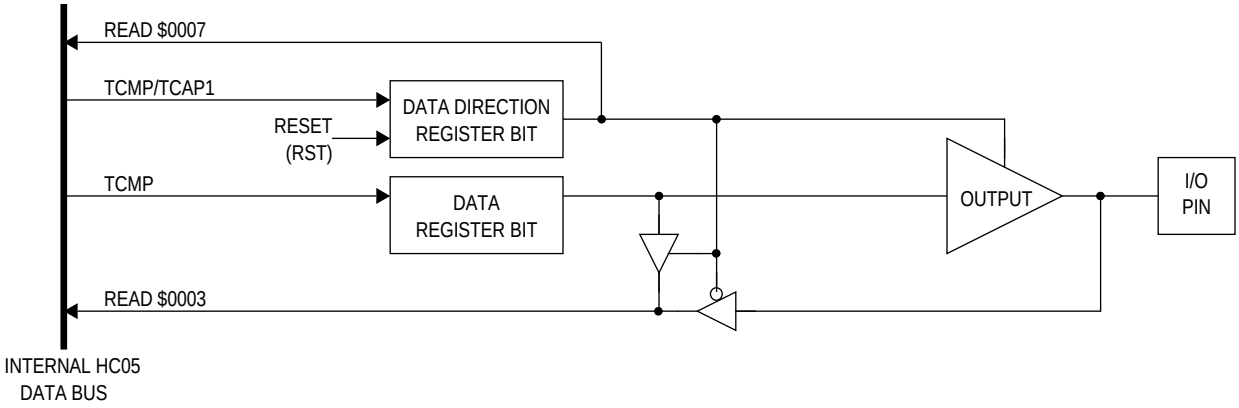

Figure 7-5. Port D Circuitry

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7.8 I/O Port Programming

Each pin on ports A–C may be programmed as an input or an output under software control as shown in **Table 7-1**, **Table 7-2**, and **Table 7-3**. Port D6 may be programmed as an input or an output and port D7 may be used as an input only as shown in **Table 7-4**. The direction of a pin is determined by the state of its corresponding bit in the associated port data direction register (DDR). A pin is configured as an output if its corresponding DDR bit is set to a logic 1. A pin is configured as an input if its corresponding DDR bit is cleared to a logic 0.

At power-on or reset, all DDRs are cleared, which configures all port pins as inputs. The DDRs are capable of being written to or read by the processor. During the programmed output state, a read of the data register will actually read the value of the output data latch and not the level on the I/O port pin.

Table 7-1. Port A I/O Functions

DDRA	I/O Pin Mode	Accesses to DDRA @ $0004	Accesses to Data Register @ $0000	
		Read/Write	Read	Write
0	IN, Hi-Z	DDRA0–DDRA7	PA0–PA7	*
1	OUT	DDRA0–DDRA7	PA0–PA7	PA0–PA7

* Does not affect input, but stored to data register

Table 7-2. Port B I/O Functions

DDRB	I/O Pin Mode	Accesses to DDRA @ $0005	Accesses to Data Register @ $0001	
		Read/Write	Read	Write
0	IN, Hi-Z	DDRB4–DDRB7	PB4–PB7	*
1	OUT	DDRB4–DDRB7	PB4–PB7	PB4–PB7

* Does not affect input, but stored to data register

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Table 7-3. Port C I/O Functions

DDRC	I/O Pin Mode	Accesses to DDRA @ $0006	Accesses to Data Register @ $0002	
		Read/Write	Read	Write
0	IN, Hi-Z	DDRC0–DDRC7	PC0–PC7	*
1	OUT	DDRC0–DDRC7	PC0–PC7	PC0–PC7

* Does not affect input, but stored to data register

Table 7-4. Port D I/O Functions

DDRD	I/O Pin Mode	Accesses to DDRA @ $0007	Accesses to Data Register @ $0003	
		Read/Write	Read	Write
0	IN, Hi-Z	DDRD6	PD6–PD7	*
1	OUT	DDRD6	PD6	PD6

* Does not affect input, but stored to data register

NOTE: *To avoid generating a glitch on an I/O port pin, data should be written to the I/O port data register before writing a logical 1 to the corresponding data direction register.*

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Section 8. Analog Subsystem

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8.2 Introduction

The MC68HC705MC4 includes a 6-channel, 8-bit, multiplexed input, successive approximation analog-to-digital (A/D) converter, with six of the inputs available on external pins and four additional internal channels. Refer to **Figure 8-1** for a block diagram of the analog subsystem.

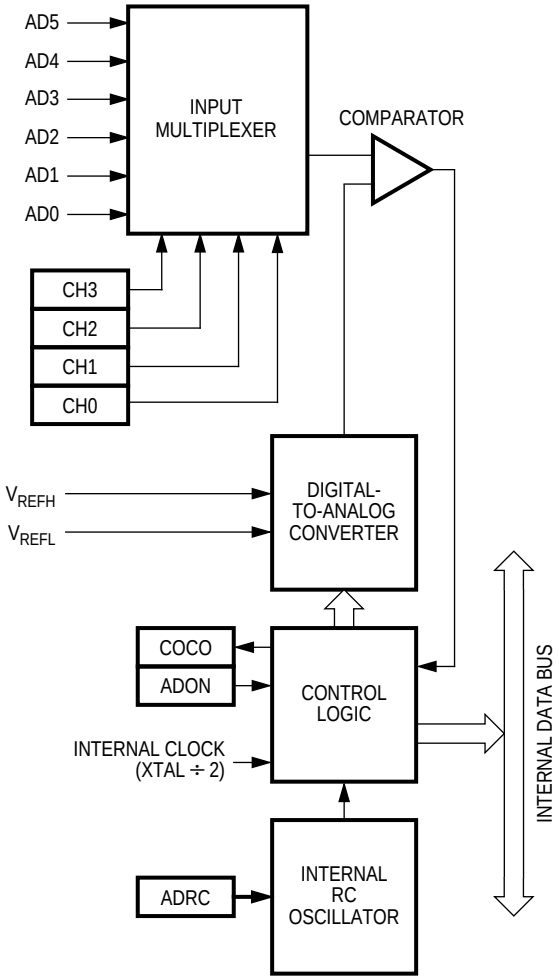

Figure 8-1. Analog Subsystem Block Diagram

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8.3 Analog Section

The following subsections describe the analog section of this subsystem.

8.3.1 Ratiometric Conversion

The A/D is ratiometric, with two dedicated pins supplying the reference voltages (V_{REFH} and V_{REFL}). An input voltage equal to V_{REFH} converts to $FF (full scale) and an input voltage equal to V_{REFL} converts to $00. An input voltage greater than V_{REFH} will convert to $FF with no overflow indication. For ratiometric conversions, the source of each analog input should use V_{REFH} as the supply voltage and be referenced to V_{REFL}.

8.3.2 V_{REFH} and V_{REFL}

The reference supply for the converter uses two dedicated pins rather than being driven by the system power supply lines because the voltage drops in the bonding wires of those heavily loaded pins would degrade the accuracy of the A/D conversion. V_{REFH} and V_{REFL} are internally wired to the analog supply voltages AV_{DD} and AV_{SS}. These pins are located next to each other to permit optimal decoupling.

8.3.3 Accuracy and Precision

The 8-bit conversions shall be accurate to within $\pm 1^1/_2$ LSB including quantization.

8.4 Conversion Process

The A/D reference inputs are applied to a precision internal digital-to-analog converter. Control logic drives this D/A and the analog output is successively compared to the selected analog input that was sampled at the beginning of the conversion time. The conversion process is monotonic and has no missing codes.

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8.5 Digital Section

The following subsections describe the digital section of this subsystem.

8.5.1 Conversion Times

Each channel of conversion takes 32 clock cycles, which must be at a frequency equal to or greater than 1 MHz. For applications in which the bus speed is below 1 MHz, the A/D internal RC oscillator must be enabled.

8.5.2 Multi-Channel Operation

In user mode, a multiplexer allows the single A/D converter to select one of eight analog signals, two of which are V_{REFH} and V_{REFL}. The eight pins of port C are input signals to the multiplexer.

8.5.3 Unused A/D Inputs as I/O

When the A/D system is enabled, two pins, V_{REFH} (PC6) and V_{REFL} (PC7), are automatically assumed to have their dedicated functions. The channel select bits define which port C pin will be used as the analog in pin and overrides any control from the port C I/O logic by forcing that pin as the input to the analog circuitry. The port C pins that are not selected by the channel select bits [CH3:0], are controlled by the port C I/O logic, and thus can be used as general-purpose I/O. Writes to port C will not have any effect on the selected channel.

NOTE: *The DDR bits corresponding to an A/D channel used by the application must be cleared. For example, AD2 shares a pin with PC2, so the DDRC2 bit must be cleared (unless this is the only channel the A/D ever selects). This is to ensure that the port output value held in the port C data register is not driven out of the pin when the A/D has selected another channel for conversion.*

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8.6 A/D Status and Control Register

The following paragraphs describe the function of the A/D status and control register.

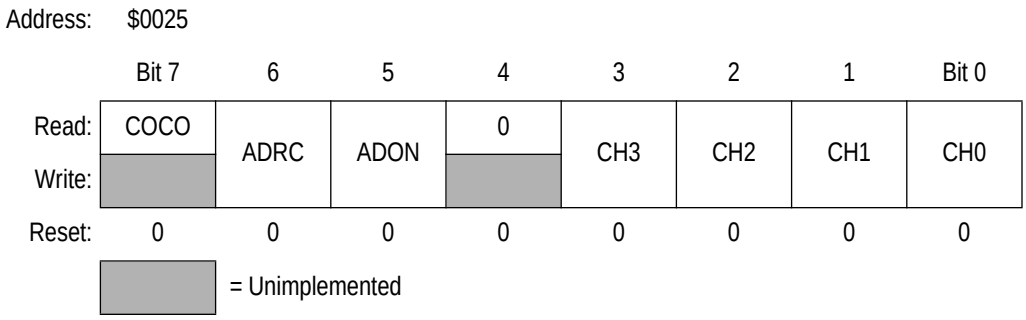

Figure 8-2. A/D Status and Control Register (ADSCR)

COCO — Conversions Complete

This read-only status bit is set when a conversion is completed, indicating that the A/D data register contains valid results. This bit is cleared whenever the A/D status and control register is written and a new conversion is automatically started or whenever the A/D data register is read. Once a conversion has been started by writing to the A/D status and control register, conversions of the selected channel will continue every 32 cycles until the A/D status and control register is written again. In this continuous conversion mode, the A/D data register will be filled with new data and the COCO bit set every 32 cycles. Data from the previous conversion will be overwritten regardless of the state of the COCO bit prior to writing.

ADRC — A/D RC Oscillator Control

When the RC oscillator is selected (ADRC = 1) to be the A/D clock source, it requires a time, t_{ADRC}, to stabilize. Results can be inaccurate during this time. If the CPU clock is running below 1 Mhz, the RC oscillator must be used.

When ADRC = 0, the A/D uses the CPU clock.

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ADON — A/D On

When the A/D is turned on (ADON = 1), it requires a time t_{ADON} for the current sources to stabilize, and results can be inaccurate during this time. This bit turns on the charge pump. If the ADRC is set, clearing this bit disables the RC oscillator to save power.

CH3:CH0 — Channel Select Bits

CH3, CH2, CH1, and CH0 form a 4-bit field, which is used to select one of eight A/D channels. Channels 0–5 correspond to port C input pins on the MCU. Channels 8-a are used for internal reference points. In user mode, channel b is reserved and converts to $00. **Table 8-1** shows the signals selected by the channel select field.

Using a port C pin as both an analog and digital input simultaneously is prohibited to prevent excess power dissipation. When the A/D is enabled (ADON = 1) and one of the channels 0-5 is selected, the corresponding port C pin will appear as a logic 0 to a digital read. The remaining port C pins (0-5) will read normally. To digitally read all eight port C pins simultaneously, the A/D must be disabled (ADON = 0).

Table 8-1. A/D Channel Assignments

Channel	Signal
0	AD0 Port C Bit 0
1	AD1 Port C Bit 1
2	AD2 Port C Bit 2
3	AD3 Port C Bit 3
4	AD4 Port C Bit 4
5	AD5 Port C Bit 5
6	Unused
7	Unused
8	V_{REFH}
9	V_{REFL}
a	$(V_{REFH} + V_{REFL})/2$
b–f	V_{REFL}

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8.7 A/D Data Register

One 8-bit result register is provided. This register is updated each time COCO is set. Reset has no effect on this register.

Address: $0024

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Write:								
Reset:	Unaffected by Reset							

Figure 8-3. A/D Converter Data Register (ADDR)

8.8 A/D During Wait Mode

The A/D continues normal operation during wait mode. To decrease power consumption during wait, it is recommended that both the ADON and ADRC bits in the A/D status and control register be cleared if the A/D converter is not being used. If the A/D converter is in use and the system clock rate is above 1.0 MHz, it is recommended that the ADRC bit be cleared.

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Analog Subsystem

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Section 9. 16-Bit Timer

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9.2 Introduction

The MC68HC705MC4 MCU contains a single 16-bit programmable timer with two input capture functions or one input capture function and an output compare function. The 16-bit timer is driven by the output of a fixed divide-by-four prescaler operating from the internal clock. The 16-bit timer may be used for many applications including input waveform measurement while simultaneously generating an output waveform. Pulse widths can vary from microseconds to seconds depending on the oscillator frequency selected. The 16-bit timer is also capable of generating periodic interrupts. See **Figure 9-1**.

Because the timer has a 16-bit architecture, each function is represented by two registers. Each register pair contains the high and low byte of that function. Generally, accessing the low byte of a specific timer function allows full control of that function; however, an access of the high byte inhibits that specific timer function until the low byte is also accessed.

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NOTE: *The I bit in the condition code register (CCR) should be set while manipulating both the high and low byte registers of a specific timer function. This prevents interrupts from occurring between the time that the high and low bytes are accessed.*

9.3 Timer

The key element of the programmable timer is a 16-bit free-running counter or timer registers, preceded by a prescaler which divides the internal clock by four. The prescaler gives the timer a resolution of 1.33 microseconds when a 6 MHz (3 MHz internal bus) crystal is used. The counter is incremented to increasing values during the low portion of the internal clock cycle.

NOTE: *Four internal bus cycles must be completed before subsequent access of TMRH and ACRH. This ensures the timer count has released the TMRH and ACRH buffers.*

The double byte free-running counter can be read from either of two locations: the timer registers (TMRH, TMRL) or the alternate counter registers (ACRH, ACRL). Both locations will contain identical values. A read sequence containing only a read of the LSB of the counter (TMRL/ACRL) will return the count value at the time of the read. If a read of the counter accesses the MSB first (TMRH/ACRH) it causes the LSB (TMRL/ACRL) to be transferred to a buffer. This buffer value remains fixed after the first MSB byte read even if the MSB is read several times. The buffer is accessed when reading the counter LSB (TMRL/ACRL), and thus completes a read sequence of the total counter value. When reading either the timer or alternate counter registers, if the MSB is read, the LSB must also be read to complete the read sequence. See **Figure 9-2** and **Figure 9-3**.

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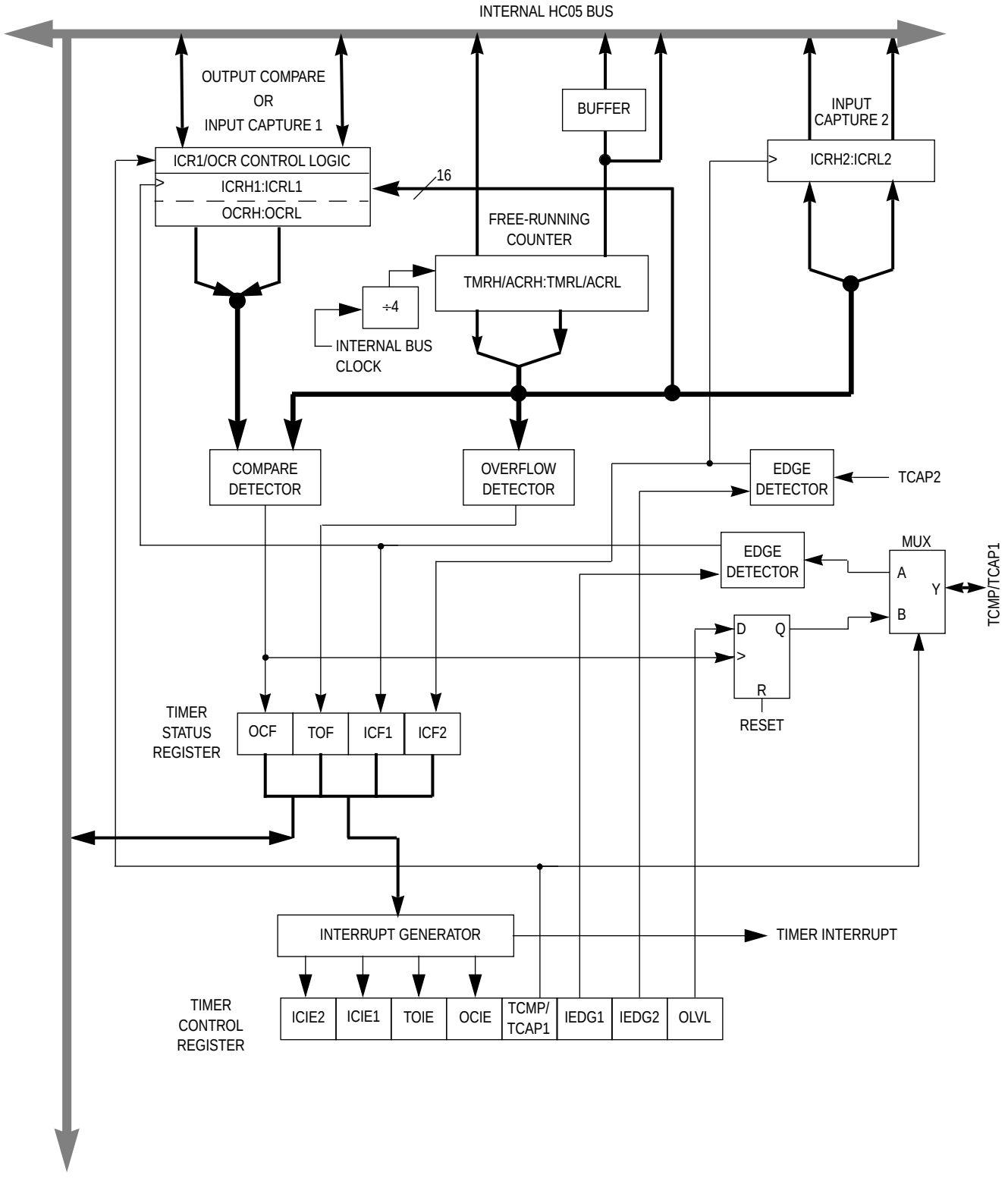

Figure 9-1. 16-Bit Timer Block Diagram

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Address:	$0020							
	Bit 7	6	5	4	3	2	1	Bit 0
Read:	BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8
Write:								
Reset:	1	1	1	1	1	1	1	1
Address:	$0021							
	Bit 7	6	5	4	3	2	1	Bit 0
Read:	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Write:								
Reset:	1	1	1	1	1	1	0	0

= Unimplemented

Figure 9-2. Timer Registers (TMRH/TMRL)

Address:	$0022							
	Bit 7	6	5	4	3	2	1	Bit 0
Read:	BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8
Write:								
Reset:	1	1	1	1	1	1	1	1
Address:	$0023							
	Bit 7	6	5	4	3	2	1	Bit 0
Read:	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Write:								
Reset:	1	1	1	1	1	1	0	0

= Unimplemented

Figure 9-3. Alternate Counter Registers (ACRH/ACRL)

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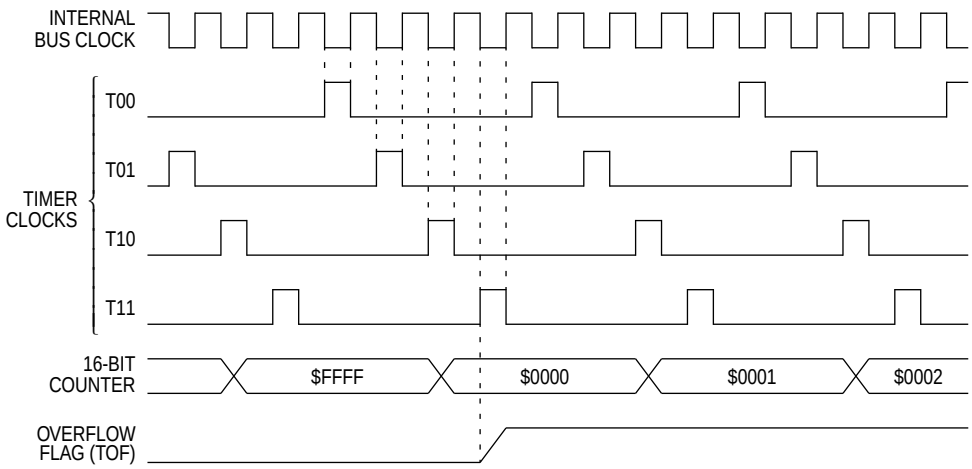
The timer registers and alternate counter registers can be read at any time without affecting their values. However, the alternate counter registers differ from the timer registers in one respect: a read of the timer register LSB can clear the timer overflow flag (TOF). Therefore, the alternate counter registers can be read at any time without the possibility of missing timer overflow interrupts due to clearing of the TOF. See **Figure 9-4**.

The free-running counter is initialized to $FFFC during reset and is a read-only register.



NOTE:
The TOF bit is set at timer state T11 (transition of counter from $FFFF to $0000). It is cleared by reading the timer status register (TSR) during the high portion of the internal clock followed by reading the LSB of the counter register pair (TMRL).

Figure 9-4. State Timing Diagram for Timer Overflow

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9.4 Output Compare

The output compare function may be used to generate an output waveform and/or as an elapsed time indicator. If the TCMP/TCAP1 bit of the TCR is set, output to the port pin is enabled. All of the bits in the output compare register pair OCRH/OCRL are readable and writeable and are not altered by the 16-bit timer's control logic. Reset does not affect the contents of these registers. See **Figure 9-5**.

Address: $001D

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8
Reset:	Unaffected by Reset							

Address: $001E

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reset:	Unaffected by Reset							

Figure 9-5. Output Compare Registers (OCRH/OCRL)

The contents of the output compare registers are compared with the contents of the free-running counter once every four internal clock cycles. If a match is found, the output compare flag bit (OCF) is set and the output level bit (OLVL) is clocked to the output latch. The values in the output compare registers and output level bit should be changed after each successful comparison to control an output waveform, or to establish a new elapsed time-out. An interrupt can also accompany a successful output compare if the output compare interrupt enable bit (OCIE) is set.

After a CPU write cycle to the MSB of the output compare register pair (OCRH), the output compare function is inhibited until the LSB (OCRL) is written. Both bytes must be written if the MSB is written. A write made only to the LSB will not inhibit the compare function. The free-running

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counter increments every four internal clock cycles. The minimum time required to update the output compare registers is a function of software rather than hardware.

The output compare output level bit (OLVL) will be clocked to its output latch regardless of the state of the output compare flag bit (OCF). A valid output compare must occur before the OLVL bit is clocked to its output latch (TCMP).

NOTE: *The input capture 1 and the output compare functions share the same data register and are, therefore, mutually exclusive. For example, the output compare function is not available (including interrupts) when input capture 1 is enabled.*

Since neither the output compare flag (OCF) nor the output compare registers are affected by reset, care must be exercised when initializing the output compare function. The following procedure is recommended:

1. Block interrupts by setting the I bit in the condition code register (CCR).
2. Write the MSB of the output compare register pair (OCRH) to inhibit further compares until the LSB is written.
3. Read the timer status register (TSR) to arm the output compare flag (OCF).
4. Write the LSB of the output compare register pair (OCRL) to enable the output compare function and to clear its flag OCF (and interrupt).
5. Unblock interrupts by clearing the I bit in the CCR.

This procedure prevents the output compare flag bit (OCF) from being set between the time it is read and the time the output compare registers are updated. A software example is shown in **Figure 9-6**.

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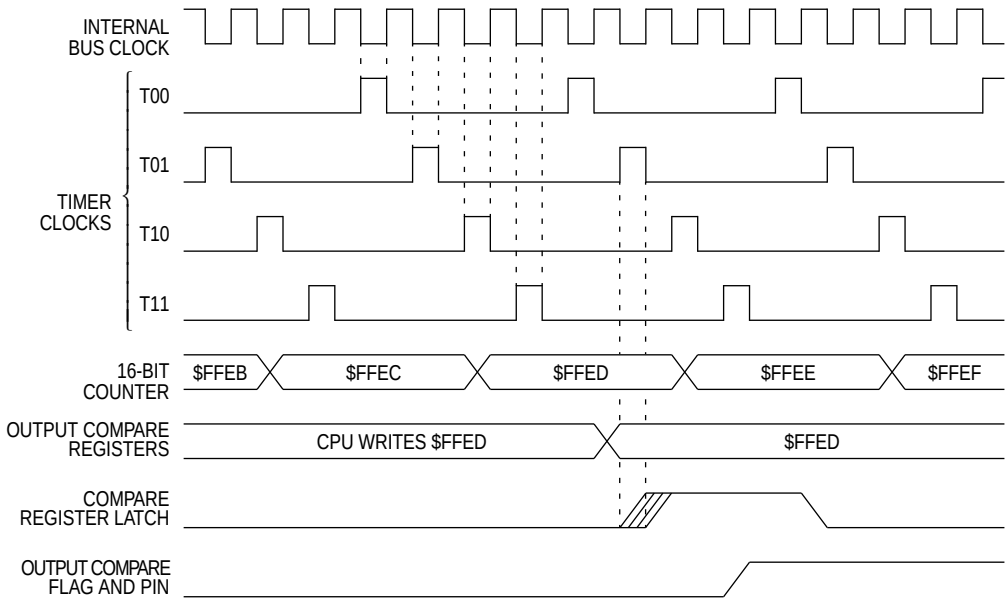
```
9B          SEI             BLOCK INTERRUPTS
.   .   .   .   .
.   .   .   .   .
B6  XX  LDA DATAH HI BYTE FOR COMPARE
BE  XX  LDX DATAL LO BYTE FOR COMPARE
B7  1D  STA OCRH  INHIBIT OUTPUT COMPARE
B6  18  LDA TSR   ARM OCF BIT TO CLEAR
BF  1E  STX OCRL  READY FOR NEXT COMPARE
.   .   .   .   .
.   .   .   .   .
9A          CLI             UNBLOCK INTERRUPTS
```

Figure 9-6. Output Compare Software Initialization Example



NOTES:

1. A write to the output compare registers may occur at any time, but a compare only occurs at timer state T01. Therefore, the compare may follow the write by up to four cycles.
2. The output compare flag is set at the timer state T11 that follows the comparison latch.

Figure 9-7. State Timing Diagram for Output Compare

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9.5 Input Capture

Registers are used to latch the value of the free-running counter after a defined transition is sensed by the input capture edge detector (*Note:* The input capture edge detector contains a Schmitt trigger to improve noise immunity.) The edge that triggers the counter transfer is defined by each input edge bit (IEDG1, IEDG2) in register TCR. Dynamically changing from Capture to Compare function will not affect the contents of the registers. All of the bits in the Input Capture register pair ICRH / ICRL are readable and are not altered by the 16-bit timer's control logic. Writes have no effect. Reset does not affect the contents of these registers. See **Figure 9-8** and **Figure 9-9**.

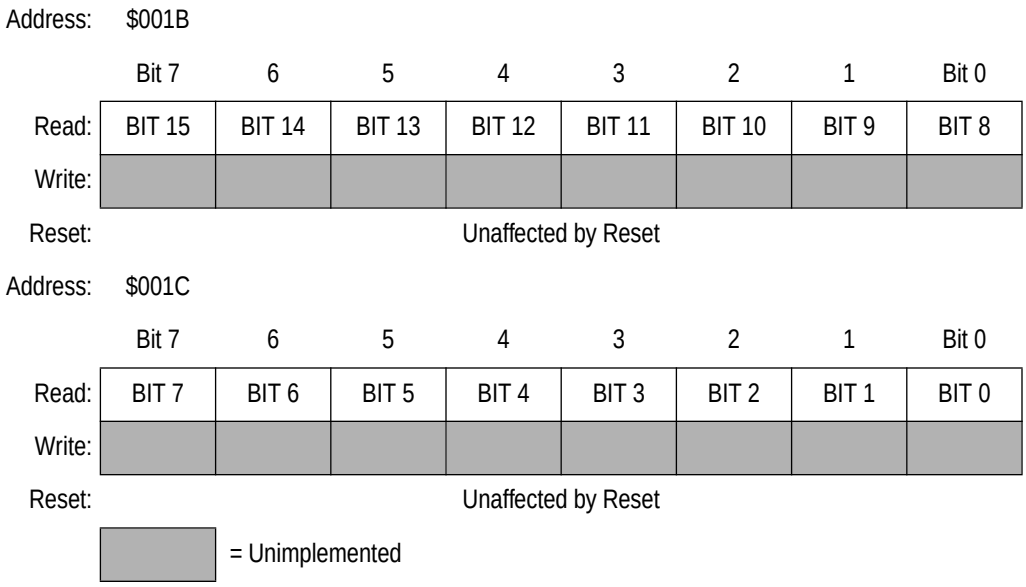

Figure 9-8. Input Capture Registers (ICRH1/ICRL1)

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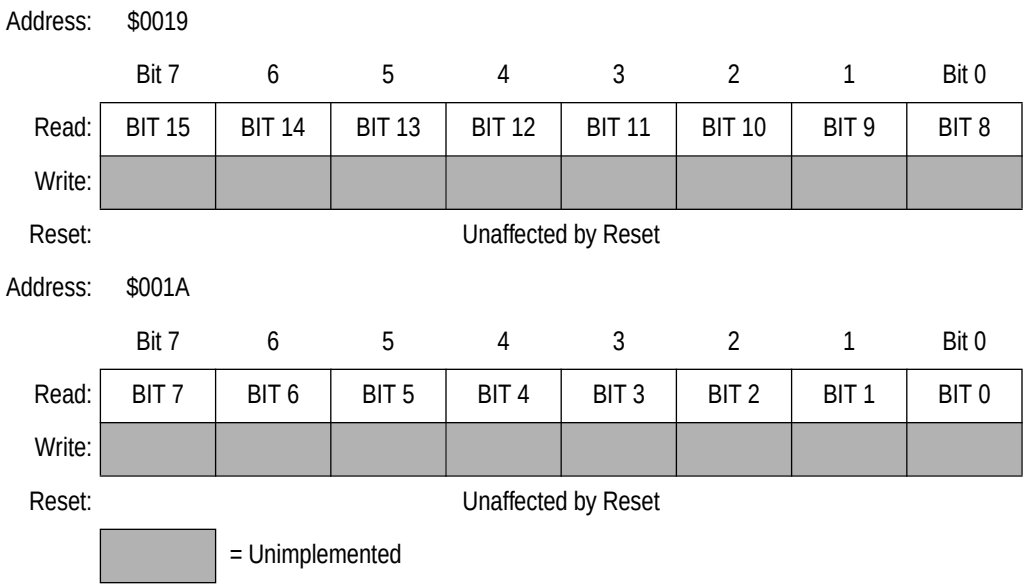

Figure 9-9. Input Capture Registers (ICRH2/ICRL2)

The result obtained by an input capture will be one more than the value of the free-running counter on the rising edge of the internal clock preceding the external transition (see **Figure 9-10**). This delay is required for internal synchronization. Resolution is affected by the prescaler, allowing the free-running counter to increment once every four internal clock cycles.

The contents of the free-running counter are transferred to the input capture registers on each proper signal transition regardless of the state of the respective input capture flag bit (ICF1, ICF2) in register TSR, the respective flag will be set. The input capture registers always contain the free-running counter value, which corresponds to the most recent input capture. An interrupt can also accompany a successful input capture if the respective input capture interrupt enable bit (ICIE) is set.

When the TCMP/TCAP1 bit of TCR is set, input capture function for TCAP1 is inhibited.

After a read of the MSB of the input capture register pair (ICRH1, ICRH2), counter transfers are inhibited until the respective LSB of the register pair (ICRL1, ICRL2) is also read. This characteristic forces the minimum pulse period attainable to be determined by the time required to execute an input capture software routine in an application.

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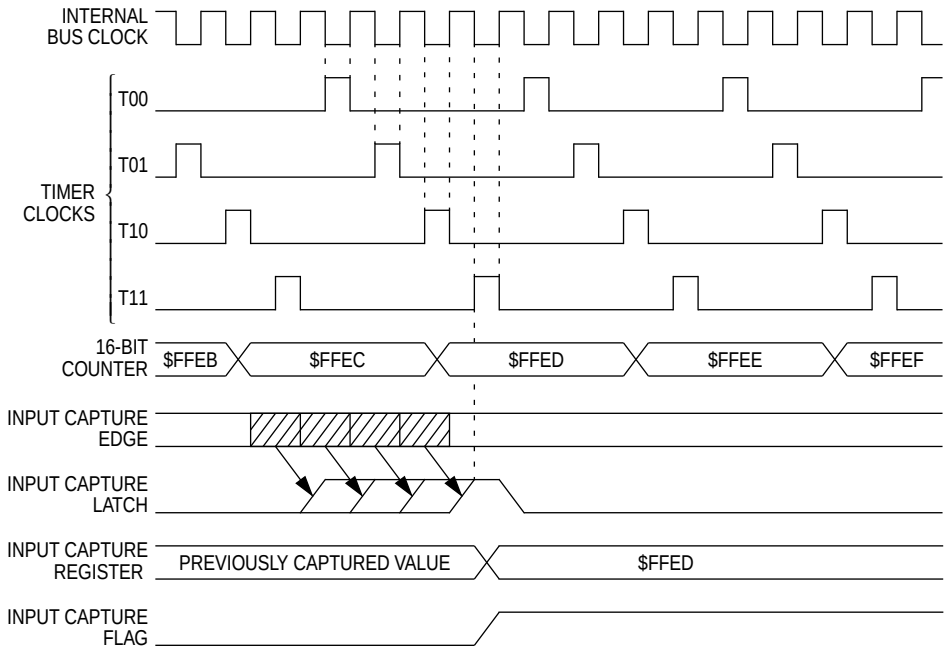
Reading the LSB of the input capture register pair (ICRL1, ICRL2) does not inhibit transfer of the free-running counter. Again, minimum pulse periods are ones that allow software to read the LSB of the register pair (ICRL1, ICRL2) and perform needed operations. There is no conflict between reading the LSB (ICRL1, ICRL2) and the free-running counter transfer since they occur on opposite edges of the internal clock.



NOTE:

If the input capture edge occurs in the shaded area between T10 states, then the input capture flag becomes set during the next T11 state.

Figure 9-10. State Timing Diagram for Input Capture

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9.6 Timer Control Register

The timer control (TCR) and free-running counter (TMRH, TMRL, ACRH, ACRL) registers are the only registers of the 16-bit timer affected by reset. The output compare port (TCMP) is forced low after reset and remains low until OLVL is set and a valid output compare occurs.

Address: $0017

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	ICIE2	ICIE1	TOIE	OCIE	TCMP/ TCAP1	IEDG1	IEDG2	OLVL
Reset:	0	0	0	0	0	U	U	0

= Unimplemented U= Unaffected

Figure 9-11. Timer Control Register (TCR)

ICIE2 — Input Capture Interrupt Enable 2

Bit 7, when set, enables input capture 2 interrupts to the CPU. The interrupt will occur at the same time bit 7 (ICF2) in the TSR register is set.

ICIE1 — Input Capture Interrupt Enable 1

Bit 6, when set, enables input capture 1 interrupts to the CPU if and only if the TCMP/TCAP1 bit (bit 3) is cleared. The interrupt will occur at the same time bit 6 (ICF1) in the TSR register is set. If the TCMP/TCAP1 bit is set, the input capture 1 interrupt is disabled, regardless of the state of the ICIE1 bit.

TOIE — Timer Overflow Interrupt Enable

Bit 5, when set, enables timer overflow (rollover) interrupts to the CPU. The interrupt will occur at the same time bit 5 (TOF) in the TSR register is set.

OCIE — Output Compare Interrupt Enable

Bit 4, when set, enables output compare interrupts to the CPU if and only if the TCMP/TCAP1 bit (bit 3) is set. The interrupt will occur at the same time bit 4 (OCF) in the TSR register is set. If the TCMP/TCAP1 bit is cleared, the output compare interrupt is disabled, regardless of the state of the OCIE bit.

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TCMP/TCAP1

Bit 3, when set, enables the TCMP function, when clear, the TCAP1 function. Reset clears this bit. When set it enables the TCMP output latch value to be output to the port pin and disables the edge detect of TCAP1. When clear, it disables the TCMP output latch from the port pin and enables the edge detect of TCAP1. Note that this bit has no effect on the setting of OCF and ICF1.

NOTE: *The input capture 1 and the output compare functions share the same data register and are, therefore, mutually exclusive. For example, the output compare function is not available (including interrupts) when input capture 1 is enabled.*

IEDG1 — Input Capture Edge Select 1

Bit 2 selects which edge of the input capture signal will trigger a transfer of the contents of the free-running counter registers to the input capture registers (ICRH1, ICRL1). Clearing this bit will select the falling edge, setting it selects the rising edge.

IEDG2 — Input Capture Edge Select 2

Bit 1 selects which edge of the input capture signal will trigger a transfer of the contents of the free-running counter registers to the input capture registers (ICRH2, ICRL2). Clearing this bit will select the falling edge, setting it selects the rising edge.

OLVL — Output compare Output level Select

Bit 0 selects the output level (high or low) that is clocked into the output compare output latch at the next successful output compare.

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9.7 Timer Status Register

Reading the timer status register (TSR) satisfies the first condition required to clear status flags and interrupts. The only remaining step is to read (or write) the register associated with the active status flag (and/or interrupt). This method does not present any problems for input capture or output compare functions.

However, a problem can occur when using a timer interrupt function and reading the free-running counter at random times to, for example, measure an elapsed time. If the proper precautions are not designed into the application software, a timer overflow flag (TOF) could unintentionally be cleared if:

1. The TSR is read when bit 5 (TOF) is set, and
2. The LSB of the free-running counter is read, but not for the purpose of servicing the flag or interrupt.

The alternate counter registers (ACRH, ACRL) contain the same values as the timer registers (TMRH, TMRL). Registers ACRH and ACRL can be read at any time without affecting the timer overflow flag (TOF) or interrupt.

Address: $0018

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	ICF2	ICF1	TOF	OCF	0	0	0	0
Write:								
Reset:	U	U	U	U	0	0	0	0

= Unimplemented U = Unaffected

Figure 9-12. Timer Status Register (TSR)

ICF2 — Input Capture 1 Flag

Bit 7 is set when the edge specified by IEDG2 in register TCR has been sensed by the input capture edge detector fed by pin TCAP2. This flag, and the input capture interrupt, can be cleared by reading register TSR followed by reading the LSB of the input capture register pair (ICRL2).

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ICF1 — Input Capture 1 Flag

Bit 6 is set when the edge specified by IEDG1 in register TCR has been sensed by the input capture edge detector fed by pin TCAP1. This flag, and the input capture interrupt, can be cleared by reading register TSR followed by reading the LSB of the input capture register pair (ICRL1).

TOF — Timer Overflow Flag

Bit 5 is set by a rollover of the free-running counter from $FFFF to $0000. This flag, and the timer overflow interrupt, can be cleared by reading register TSR followed by reading the LSB of the timer register pair (TMRL).

OCF — Output Compare Flag

Bit 4 is set when the contents of the output compare registers match the contents of the free-running counter. This flag, and the output compare interrupt, can be cleared by reading register TSR followed by writing the LSB of the output compare register pair (OCRL).

9.8 Timer Operation during Wait/Halt Modes

During wait mode, the 16-bit timer continues to operate normally and may generate an interrupt to trigger the MCU out of the wait mode.

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Section 10. Pulse Width Modulator

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10.2 Introduction

The pulse width modulator (PWM) subsystem has two 8-bit channels (PWMA and PWMB). The PWM has a programmable prescaler, divide by 1.5 added to the initial prescaler, polarity, and mux enable with channel masking for motor control applications. The PWM is capable of generating signals from 0% to 100% duty cycle. A $00 in either PWM data register yields an OFF output (0%) with the polarity control bit set to one for that channel (for example, PWMA or PWMB), but a $FF yields a duty of 255/256. To achieve the 100% duty (ON output), the polarity control bit is set to zero for that channel (for example, PWMA or PWMB) while the data register has $00.

NOTE: *The symbol 'x' is used in this section to indicate either channel A or channel B. For example, PWMx refers to either PWMA or PWMB.*

10.3 PWM Registers

The PWM subsystem is controlled through four control registers: CTL-A, CTL-B, RATE, and UPDATE. CTL-A, CTL-B, and the data registers feature a write interlock and buffer mechanism to permit their contents to be updated simultaneously, preventing undesirable glitching of the associated port A output. The CTL-A and CTL-B registers contain bits to control the PWM subsystem outputs on PA1–PA6 (PWM, logic 0 or logic 1) and PWM polarity bits.

The PWM subsystem control and data registers are all buffered, as shown in **Figure 10-2**. Each register consists of an active register, which contains the data used by the PWM subsystem, and a buffer register, which contains the data most recently written to the register address. Writes to the buffer registers are transferred to the active registers at the end of the PWM period if the respective bit in the UPDATE register is set to 0. If it is set to 1, the transfer will occur immediately. In addition, when the respective update bit is clear, a predefined sequence of register accesses may also need to be completed before the new contents of these registers are transferred. This sequence of accesses is referred to as a register interlock mechanism and is intended to allow more than one register to be modified before effecting the PWM operation. The

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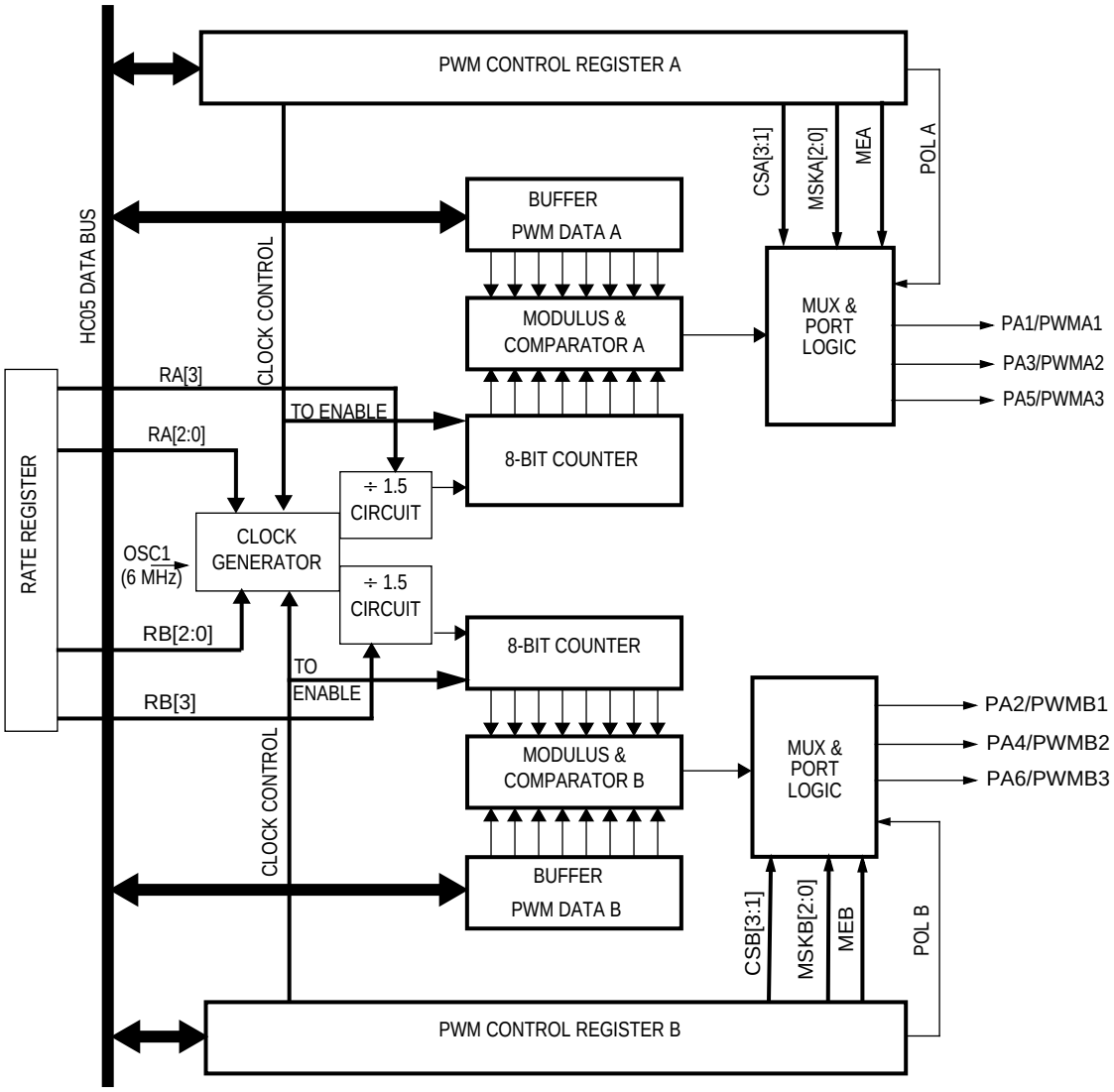

Figure 10-1. PWM Block Diagram

data register interlock mechanism is managed by mapping each data register to an interlock address (PWMx-I) and a direct address (PWMx-D). Writes to the interlock address will engage the interlock mechanism. Writes to the direct address will not engage the interlock mechanism unless it is already engaged prior to the write. A write to the direct address will therefore take immediate effect (if the corresponding update bit is set) or at the end of the current PWM cycle (if the corresponding update bit is cleared).

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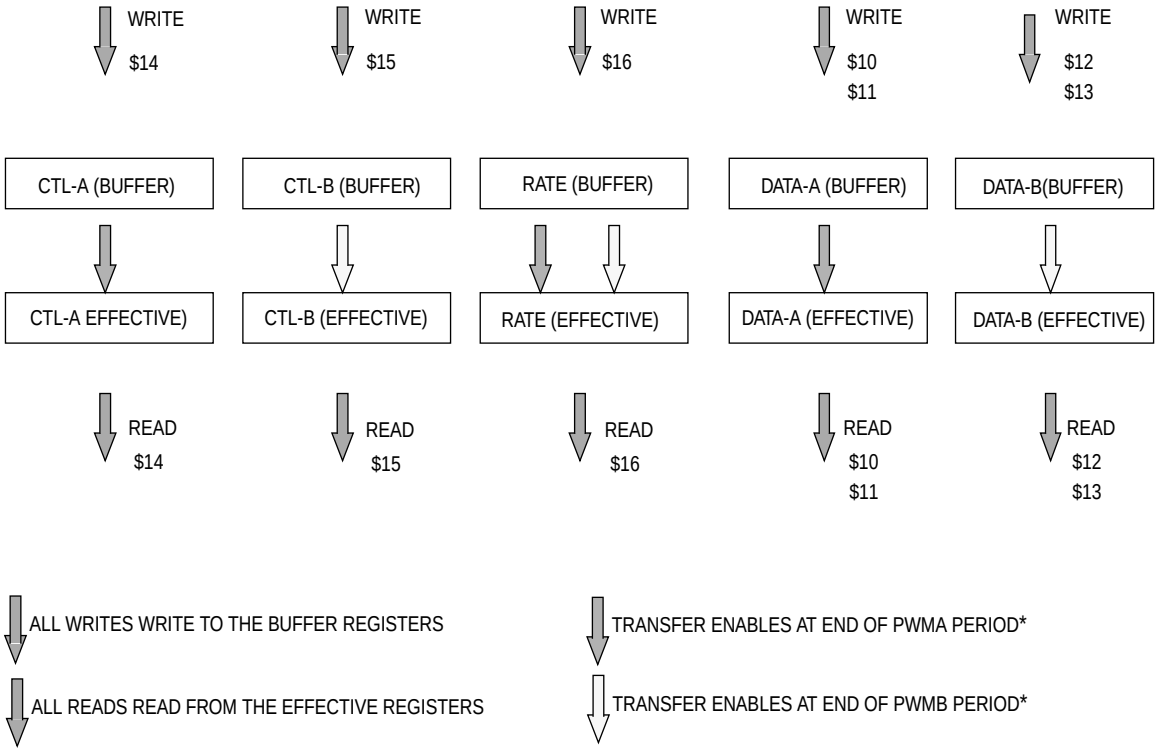
The RATE register selects the PWM counter input clock rate, defining the PWM period. This register is buffered but not interlocked with other registers. Therefore, writes to the RATE register will become effective immediately (if the corresponding update bit has been set) or at the end of the current PWM period (if the corresponding update bit has been cleared), irrespective of the state of any interlock mechanism.



*Subject to satisfying interlock conditions and the state of the corresponding UPDATE bit

Figure 10-2. PWM Register Structure

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10.4 PWM Control Registers

The following control registers direct the function of the PWM subsystem.

- Control register A (CTL-A)
- Control register B (CTL-B)
- Rate register (RATE)
- Update register (UPDATE)

10.4.1 Control Register A and Control Register B

Control register A directs PWM channel A which can drive PA1, PA3, and PA5. Control register B directs PWM channel B which can drive PA2, PA4, and PA6. As the function of CTL-A and CTL-B are identical except for the channel name. The descriptions below apply to both, and the channel is referred to as 'x'.

Address: $0014

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	MEA	POLA	MSKA3	MSKA2	MSKA1	CSA3	CSA2	CSA1
Reset:	0	0	0	0	0	0	0	0

Figure 10-3. PWM Control-A Register (CTL-A)

Address: $0015

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	MEB	POLB	MSKB3	MSKB2	MSKB1	CSB3	CSB2	CSB1
Reset:	0	0	0	0	0	0	0	0

Figure 10-4. PWM Control-B Register (CTL-B)

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Mask Enable (MEx)

When set, MEx enables the output mask feature of the PWMx subsystem. When enabled, all three pins of a channel will be used for subsystem output, that is the port registers will have no effect. All unselected pins (pins that have their corresponding CSx bit clear) will output the corresponding value of the MSKx bit. All selected pins (pins that have their corresponding CSx bit set) will output the PWM waveform. See **Table 10-1**.

The mask feature allows the user to drive any of the PWM subsystem ports (PA1–PA6) to a logic 1 or logic 0 synchronous with the register interlock timing. All PWM outputs can therefore be modified simultaneously to either drive PWM, logic 1, or logic 0 signals.

When MEx is clear, output mask feature is disabled and the port will function as a normal I/O port if the CSx bit is cleared. This feature allows some of the ports to be freed up for normal I/O when not used for PWM output. If the corresponding CSx bit is set, the selected channel will output the PWM waveform.

Polarity (POLx)

The polarity bit initializes the PWM output to a logic 1 or logic 0 at the start of each PWM cycle. See **Figure 10-5** and **Figure 10-6**.

1 = Initialize output to one. Toggles to zero at data PWMx match.

0 = Initialize output to zero. Toggles to one at data PWMx match.

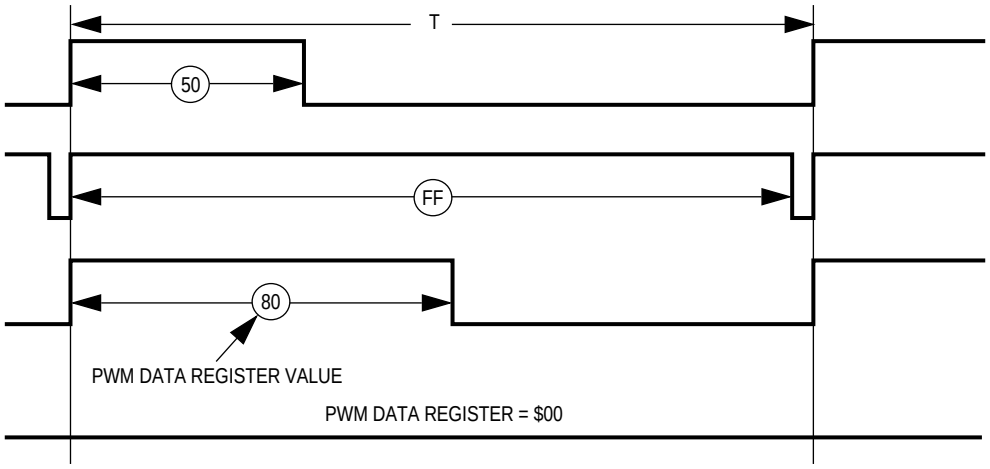

Figure 10-5. PWM Waveforms (POLx = 1)

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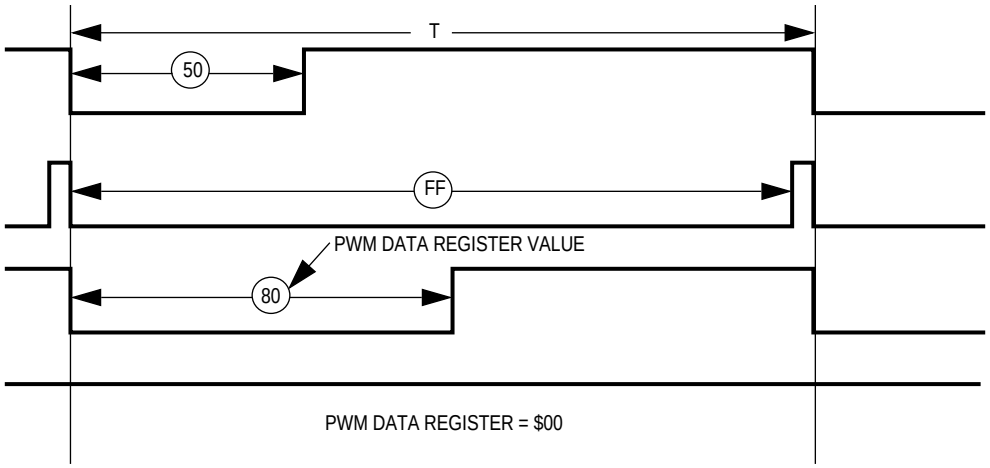

Figure 10-6. PWM Waveforms (POLx = 0)

Mask (MSKx[3:1])

When MEx is set, the MSKx bits establish mask values for pins that are not selected by CSx. A mask value of 1 drives unselected PWM subsystem pins high. A mask value of 0 drives unselected PWM subsystem pins low. When MEx is clear, the mask bits have no effect.

If the mask feature is enabled (MEx =1), the mask bits also provide an alternative method of generating 0% or 100% values. The conventional method generates 100% duty cycle by inverting the output polarity and simultaneously clearing the PWM data bits.

See **Figure 10-7**, **Table 10-1**, and **Figure 10-8** for schematic, truth table, and example waveform view for the PWM subsystem multiplexer.

Channel Select (CSx[3:1])

These bits select which pin or pins will receive the PWM waveform output. Channel select has higher priority than mask enable. When CSx[y] is set, the pin is selected and the PWMx output waveform will be sent to the port logic. When CSx[y] is clear, the output will depend on the MEx bit and the corresponding port register bit. See **Figure 10-7**, **Table 10-1**, and **Figure 10-8** for schematic, truth table, and example waveform view for the PWM subsystem multiplexer.

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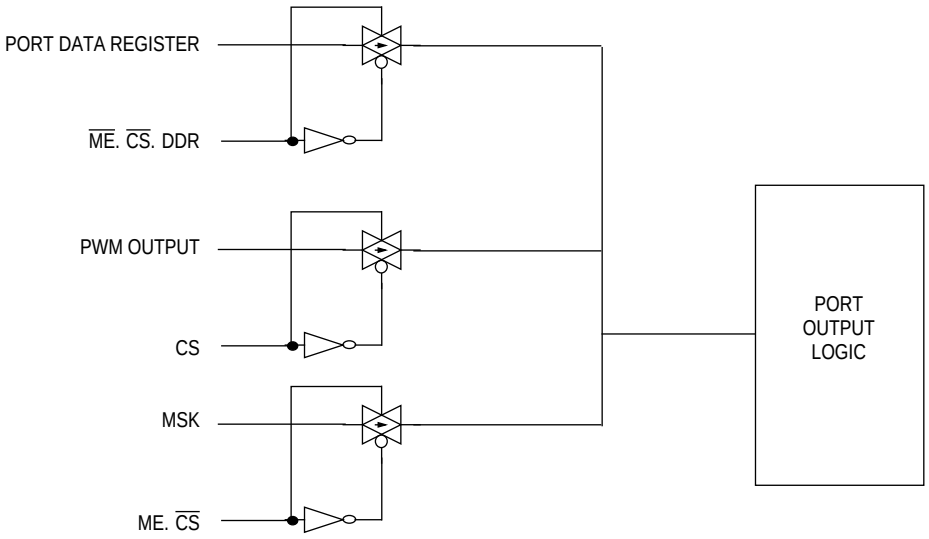

Figure 10-7. PWM Output MUX Logic

Table 10-1. PWM Output MUX Truth Table for PWMA1

MEA	MSKA1	CSA1	DDRA1	Port A1 Function
0	X	0	0	Digital Input
0	X	0	1	Digital Output
1	0	0	X	Drive Low
1	1	0	X	Drive High
X	X	1	X	PWMA

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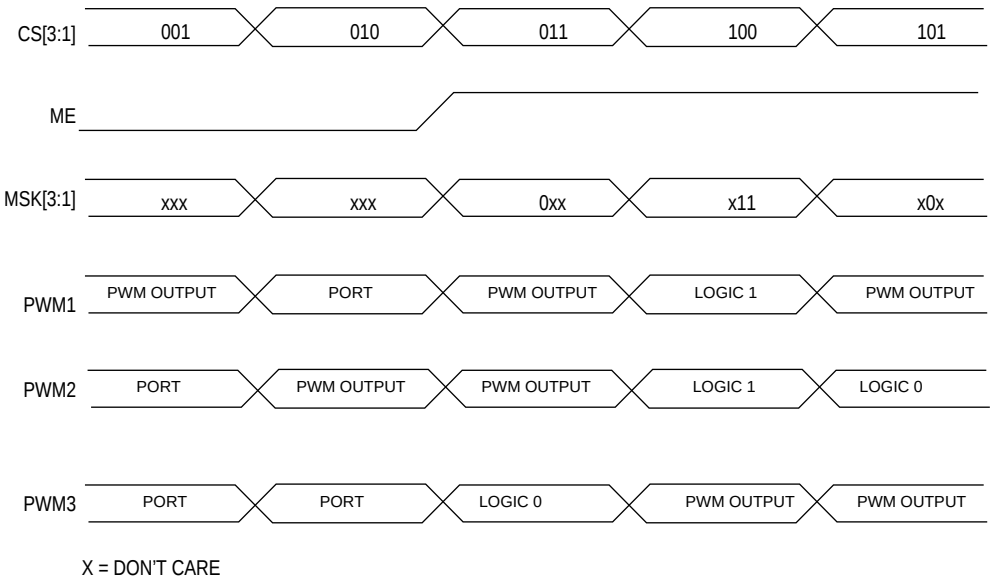

Figure 10-8. PWM Control Example

Refer to **Table 10-2** for information on mapping the PWM channels to Port A.

Table 10-2. Mapping of PWM Channels to Port A

PWM Pin	Associated PWM Control Bits	Corresponding Port A I/O
A1	MSKA1 : CSA1 : DDRA1	PA1
A2	MSKA2 : CSA2 : DDRA3	PA3
A3	MSKA3 : CSA3 : DDRA5	PA5
B1	MSKB1 : CSB1 : DDRA2	PA2
B2	MSKB2 : CSB2 : DDRA4	PA4
B3	MSKB3 : CSB3 : DDRA6	PA6

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10.4.2 RATE Register

The RATE register, shown in **Figure 10-9**, selects the 8-bit PWM counter input clock. The PWM output rate select bits (Rx[3:0]) for each channel allow for 16 different PWM duty cycles.

Address: $0016

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	RA3	RA2	RA1	RA0	RB3	RB2	RB1	RB0
Reset:	0	0	0	0	0	0	0	0

Figure 10-9. PWM Rate Register (RATE)

The PWM output rate select register selects the 8-bit PWM counter input clock. **Table 10-3** provides a rate selection table for a 6-MHz crystal.

Table 10-3. PWM Rate Select Table for 6-MHz Crystal

Rx[3:0]	PWM Output Cycle
0	23.4 kHz
1	11.7 kHz
2	5.86 kHz
3	2.93 kHz
4	1.46 kHz
5	732 Hz
6	366 Hz
7	183 Hz
8	15.6 kHz
9	7.8 kHz
A	3.9 kHz
B	1.95 kHz
C	975 Hz
D	488 Hz
E	244 Hz
F	122 Hz

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10.4.3 UPDATE Register

Some applications cannot always wait until the end of the PWM cycle in process before new control or data values take effect (for example, during fault conditions). The UPDATEx bits provide a mechanism to override the register interlock for these situations. The UPDATE register is shown in **Figure 10-10**.

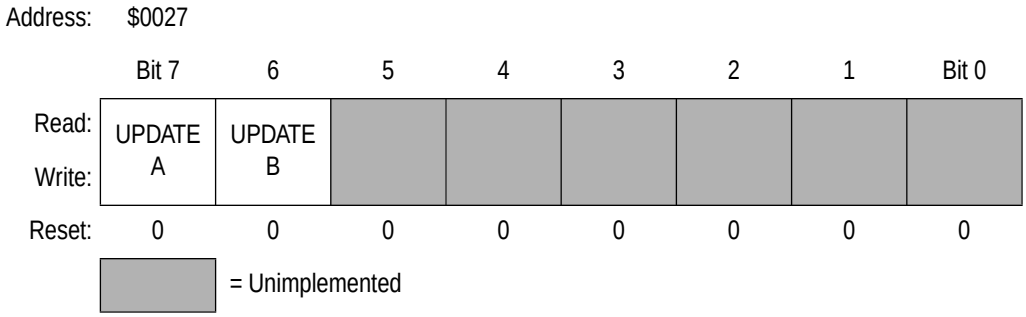

Figure 10-10. PWM Update Register (UPDATE)

If the register interlock is satisfied and the corresponding update bit is clear, the PWM registers are updated at the end of the current PWM cycle. If the register interlock is satisfied and the corresponding update bit is set the PWM registers are updated immediately. **Figure 10-11** shows the different timing cases of applying the update condition and its affects on PWM output.

After a $\overline{\text{RESET}}$ or subsequent to re-enabling the PWM channels, it is necessary for the user to write to the data registers RATE, CTL-B (if PWMB is used), and CTL-A (in that order) before writing to the UPDATE register. Writing to the UPDATE register before turning on PWMA or PWMB (writing to CTL-A or CTL-B) may disable the PWM.

After disabling a PWM channel, the corresponding UPDATE bit must be cleared before enabling the channel again. After clearing the corresponding UPDATE bit, the sequence of writing to the RATE, CTL-B, CTL-A, and then setting the corresponding UPDATE bit must be followed before re-enabling the PWM channels.

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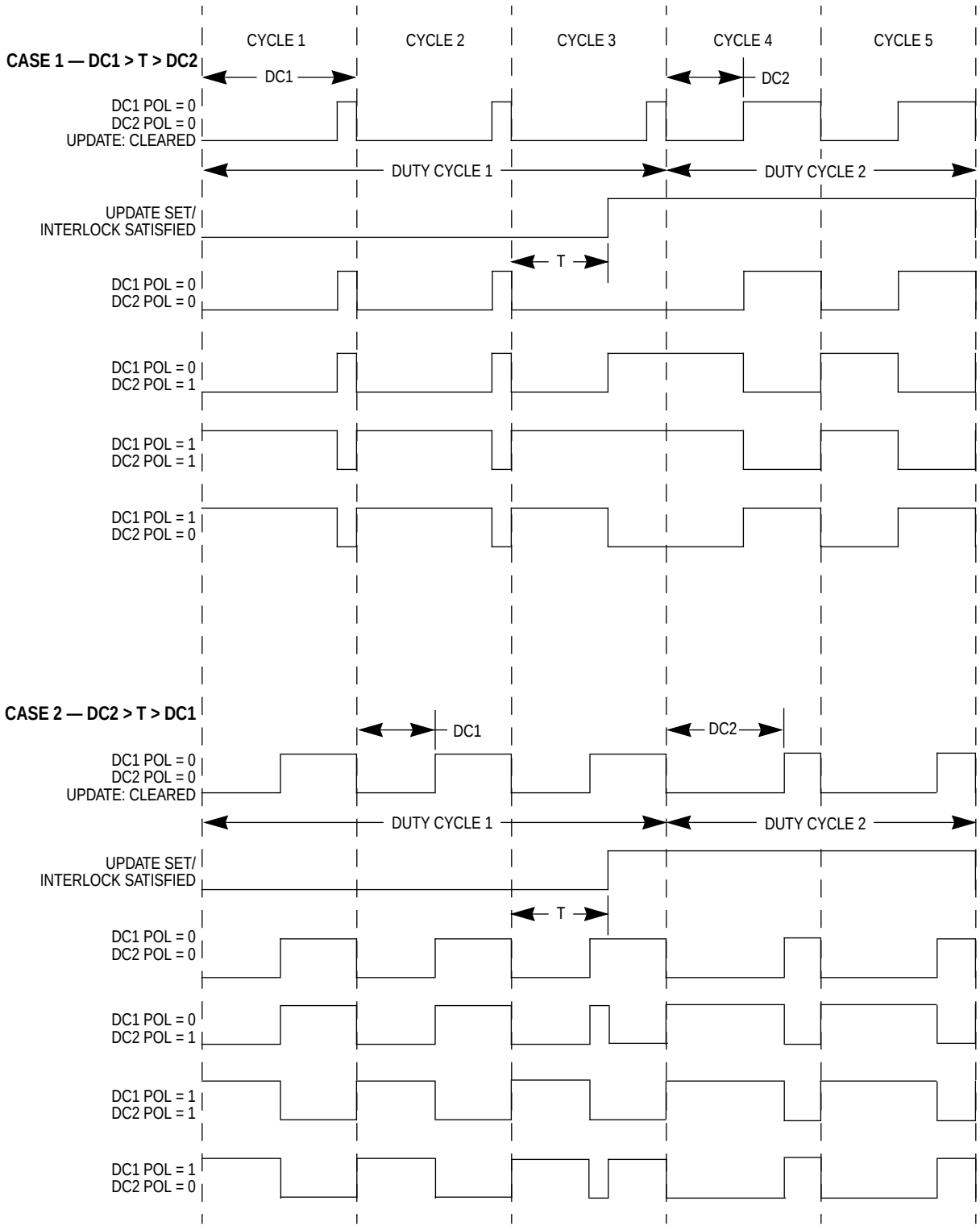

Figure 10-11. State Timing Diagram for PWM UPDATE Generator (Sheet 1 of 3)

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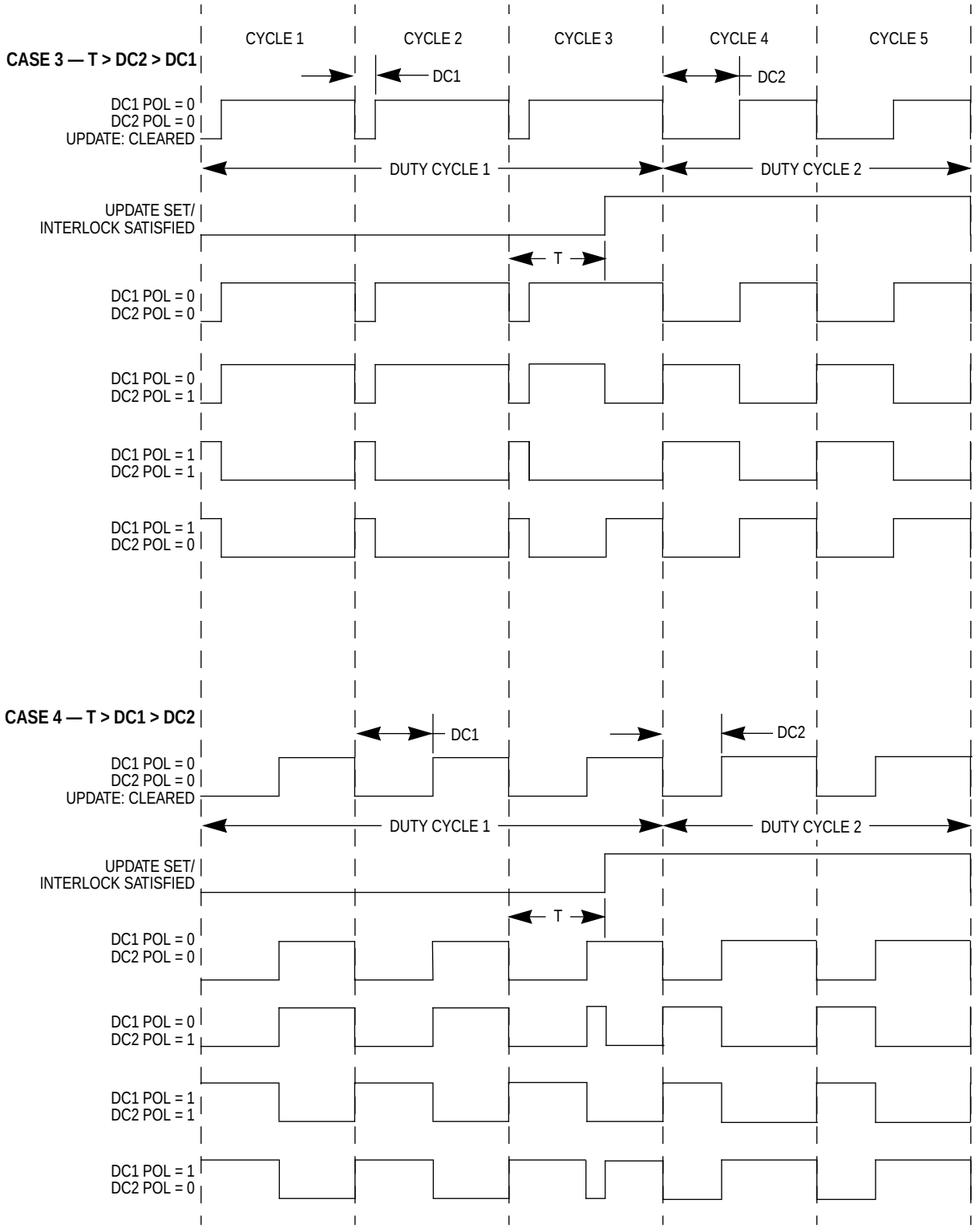

Figure 10-11. State Timing Diagram for PWM UPDATE Generator (Sheet 2 of 3)

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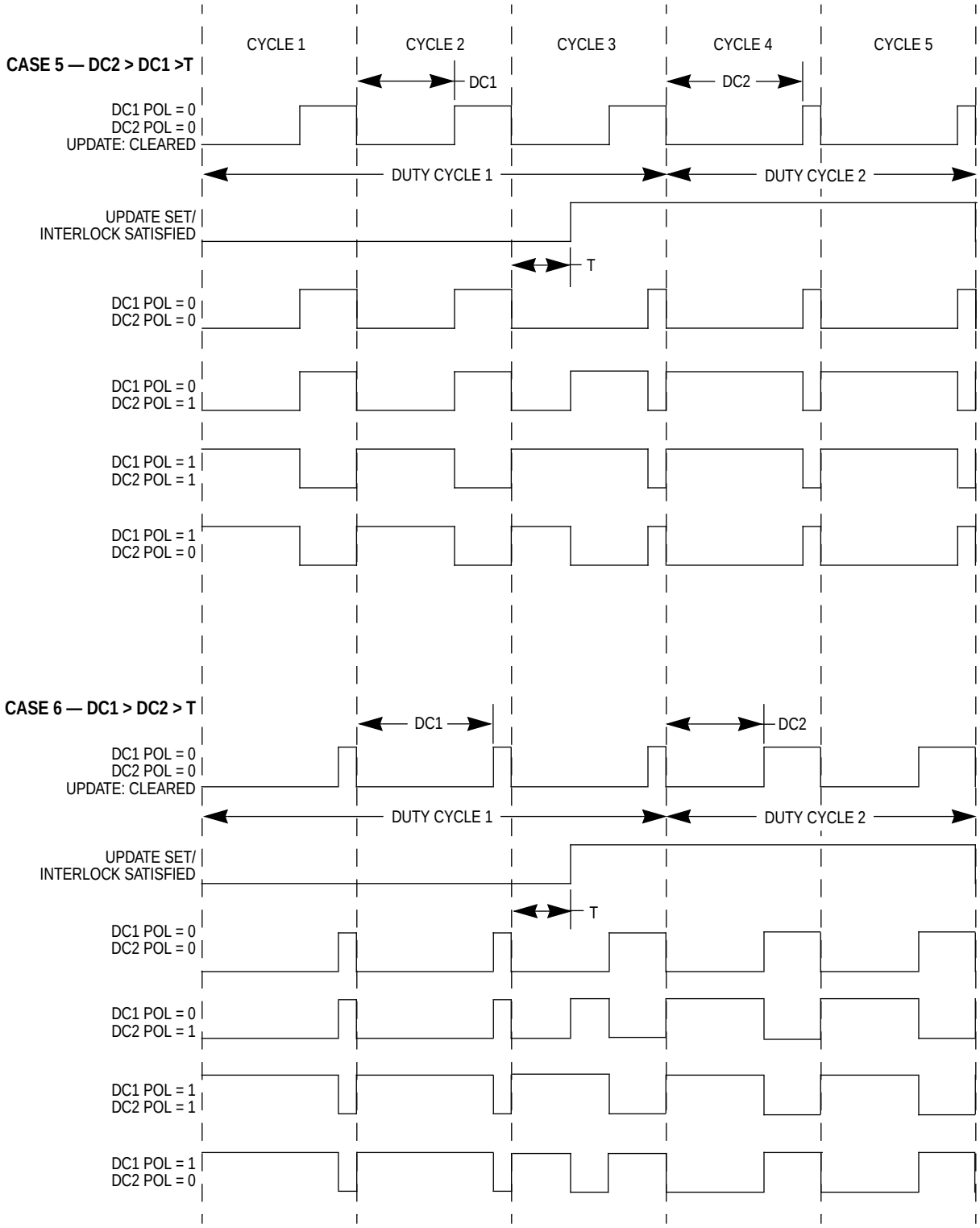

Figure 10-11. State Timing Diagram for PWM UPDATE Generator (Sheet 3 of 3)

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10.5 PWM Data Registers

The pulse width of the PWM waveform is controlled by the two data registers PWMA and PWMB. Each data register can be accessed from one of two locations, PWMx-D (direct) and PWMx-I (interlock). A write interlock and buffer mechanism is used to permit their contents to be updated simultaneously, preventing undesirable glitching of the associated port A I/O. See **10.7 PWM Operation in User Mode**.

The PWMA and PWMB data registers have been mapped to two different addresses: the direct address and the interlock address. The PWMA-D direct address is $10 and the PWMA-I interlock address is $11. The PWMB-D direct address is $12 and the PWMB-I interlock address is $13. A read from either the direct or the interlock address will read the PWM active register. A write to either address will write to the PWM buffer register.

Address: $0010

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reset:	Unaffected by Reset							

Figure 10-12. PWMA-D Data Register (PWMA-D)

Address: $0011

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reset:	Unaffected by Reset							

Figure 10-13. PWMA-I Data Register (PWMA-I)

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Address: $0012

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reset:	Unaffected by Reset							

Figure 10-14. PWMB-D Data Register (PWMB-D)

Address: $0013

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reset:	Unaffected by Reset							

Figure 10-15. PWMB-I Data Register (PWMB-I)

10.6 PWM during Resets

The PWM subsystem has two types of resets. One is a hardware reset denoted by $\overline{\text{RESET}}$. The other is a PWM reset denoted by PRESET.

After a $\overline{\text{RESET}}$, the user should write to the data registers RATE, CTL-B, then CTL-A (in that order). This will avoid an erroneous duty cycle from being driven on any of the selected PWM port pins.

To save power, a PRESET condition is possible by clearing the MEB bit and the CSB[3:1] bits in CTL-B, then the MEA bit and the CSA[3:1] bits in CTL-A. This disables the PWM subsystem, resets the 8-bit counters, resets the clock generator, and sets the port pins to the state defined by the respective port data registers and data direction registers. PRESET preserves the value of the PWMx-D registers written to them before the PRESET condition. Activating the PWM after a PRESET will commence operation of these preserved values.

The data registers are unaffected by $\overline{\text{RESET}}$. The CTL-x registers are cleared by $\overline{\text{RESET}}$.

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10.7 PWM Operation in User Mode

The following subsections describe the PWM operation in user mode.

10.7.1 Interlock Operation

All PWM registers are buffered. The register buffering prevents data written to either the control or data registers from affecting the PWM cycle under way at the time of the data write. The interlock mechanism extends this principle to multiple registers by preventing data written to groups of data and/or control registers from affecting the PWM configuration currently active until all writes are complete. There are several interlock options from which the user can pick depending upon the change of function desired. The register interlock mechanism operation is shown in **Figure 10-16**.

Writing to a PWMx interlock address will activate a data/control interlock mechanism with the corresponding CTL-x register. Under such a condition, the new value written to the PWM interlock data register will not be effective until the end of the current PWM cycle during which a write to the corresponding control register was executed.

A typical application for such a mechanism is to generate 100% duty cycle when not using the PWM output mask feature (MEx = 0). Synchronized changes to both data and control registers are, therefore, necessary to avoid PWM glitches. 100% duty cycle can be generated by clearing PWMx-I, then toggling the state of the POLx bit in the corresponding CTL-x register. Any new data written to either register will become effective at the end of the current PWM cycle during which the write to CTL-x took place.

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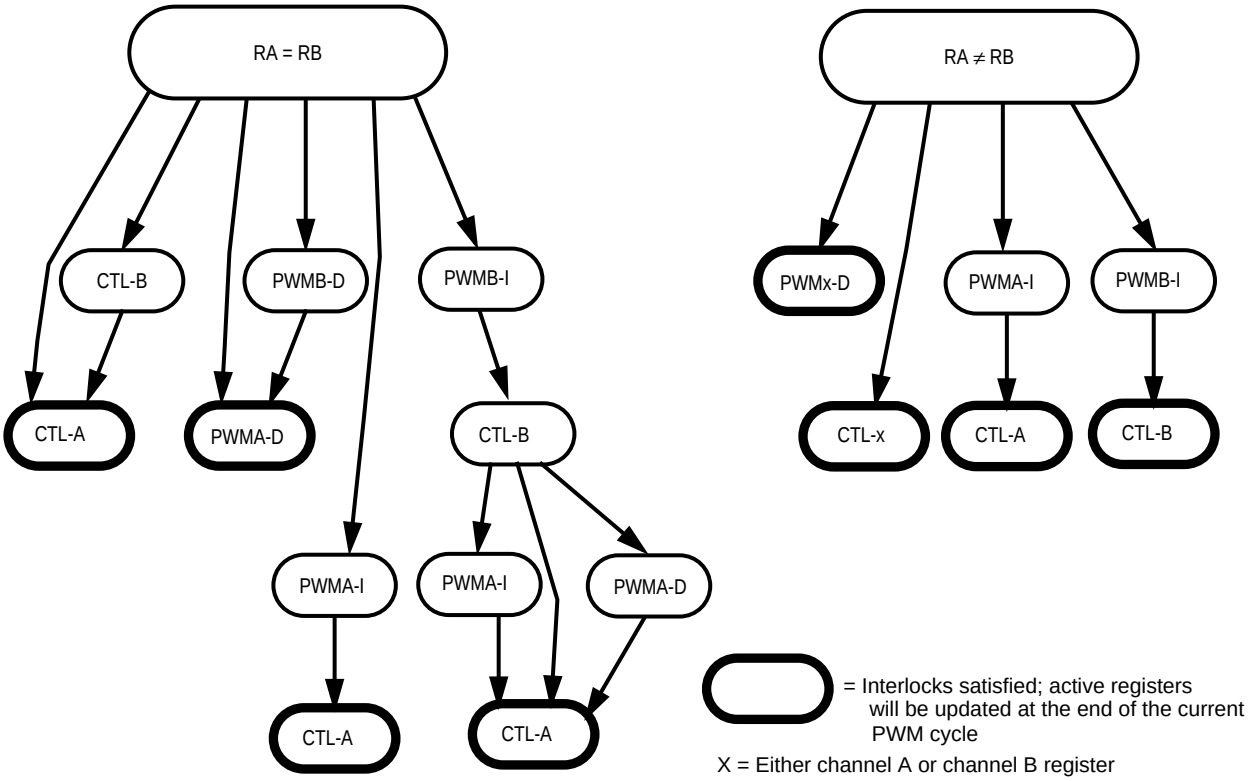

Figure 10-16. PWM Interlock Mechanisms

Writing to the direct address will not activate the interlock mechanism with the control register. The new value will be updated at the end of the current PWM cycle if the update bit is clear. The new value will be updated immediately if the update bit is set.

NOTE: *In either case above (write to interlock or direct addresses), the additional interlock mechanism that interlocks channel A and channel B together may preempt the transfer of the new data to the active registers. See* ***10.7.2 Operation with the Same PWM Rates*** *for more detail.*

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10.7.2 Operation with the Same PWM Rates

If RA equals RB, channel A and channel B are assumed to be operating together in a synchronous fashion and are interlocked. This interlock mechanism is in addition to the buffering and the PWM data/control interlock described in **10.7.1 Interlock Operation**.

A write to either PWMB data register must be followed by a write to either PWMA data register. Any new data written will become effective at the end of the current PWM cycle during which the write to PWMA took place as shown in **Figure 10-16**. The interlocking between the data registers is disabled when the channels have different periods.

A write to CTL-B control register must be followed by a write to the CTL-A control register. Any new data written to either register will become effective at the end of the current PWM cycle during which the write to CTL-A took place. The interlocking between the control registers is disabled when the channels have different periods.

Writing to the PWMx-I interlock address will also activate the interlock mechanism with the CTL-x register as described in **10.7.1 Interlock Operation**. The two interlocking mechanisms, channel A/channel B and data/control, may be in effect at the same time.

Example 1

Writing to PWMB-I ($13) will require a write to CTL-B ($15) to satisfy the data/control interlock. In addition, if RA = RB, the write to either PWMB data register will require a write to either PWMA data register, and the write to CTL-B control register will require a write to CTL-A register to satisfy the channel A/channel B interlock. The new contents of all these registers will be transferred into their respective active registers at the end of the current PWM cycle during which all invoked interlock mechanisms become satisfied if the UPDATE A and UPDATE B bits are clear. For either channel, if the corresponding update bit is set, the transfer for that channel will occur immediately after the interlock mechanism is satisfied.

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Example 2

A write to PWMB-D ($12) will not invoke the data/control interlock. However, if RA = RB, the write to either PWMB data register will require a write to either PWMA data register to satisfy the channel A/channel B interlock. Note that if a write was made to the PWMA interlock data register, the channel A/channel B interlock would still be satisfied but the data/control interlock will now be invoked for channel A. A write to CTL-A control register is now necessary to satisfy the channel A data/control interlock. Assuming UPDATE A and UPDATE B are clear in the UPDATE register, the new contents of all these registers will be transferred into their respective active registers at the end of the current PWM cycle during which all invoked interlock mechanisms become satisfied.

10.7.3 Operation with Different PWM Rates

If RA does not equal RB, channel A and channel B are assumed to be operating independently of each other and are not interlocked. New data values written to either PWM channel will occur as discussed in **10.7.1 Interlock Operation**.

Interlocking between the channels only applies when both channels have the same period (RA = RB). The RATE register is not interlocked with any other registers but it is buffered. Changes to this register will affect the PWM cycle subsequent to the write. Consequently, changing the PWM period while generating a PWM signal will not cause erroneous PWM operation (for example, glitches). Note that the RATE register is treated as two separate 4-bit registers, each buffered with the corresponding PWM channel cycle.

NOTE: *Changing the channels from having different periods to having the same period may cause a phase difference between the channels due to accumulated clock period difference. If synchronization is needed between channel A and channel B, a PRESET cycle must be executed to provide correct operation of the channel A/B interlock mechanism.*

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10.8 PWM during Wait Mode

The PWM continues normal operation during wait mode. To decrease power consumption during wait, it is recommended that the PWM subsystem be put into the PRESET state.

10.9 Application Examples

The following examples demonstrate PWM configuration options to drive brushed DC and permanent magnet brushless motors. The schematic diagrams are simplified for clarity.

10.9.1 Brushed DC Motor Interface

The basic interface for a single brushed DC motor is shown below.

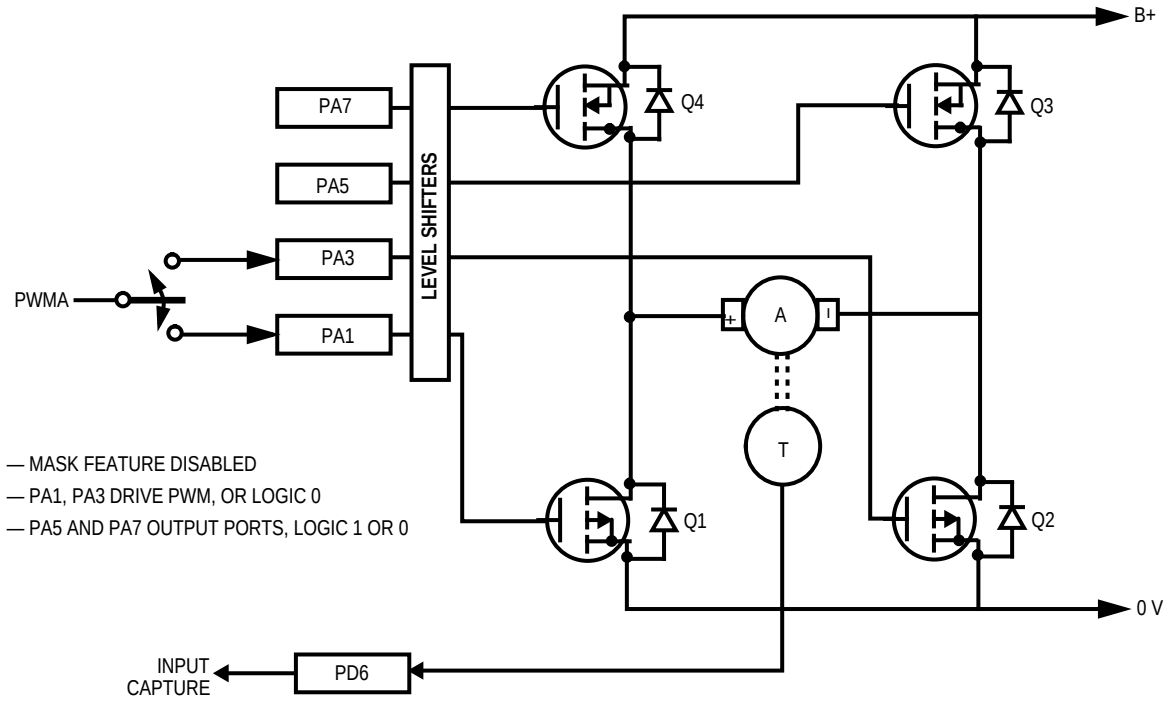

Figure 10-17. Brushed DC Motor Interface

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Table 10-4. Brushed DC Motor Truth Table

Function	Q1	Q2	Q3	Q4
Forward	Off	PWM	Off	On
Reverse	PWM	Off	On	Off
Stop	Off	Off	Off	Off

PWM channel A is configured such that the PWM signal may be directed to either PA1 (CSA1 = 1) or PA3 (CSA2 = 1). When not driving the PWM signal, these ports should drive a logic 0 (MEA = 1, MSKA1 = 0, CSA1 = 0, MSKA2 = 0, CSA2 = 0). PA5 drives either a logic 0 (MEA = 1, MSKA3 = 0, CSA3 = 0) or logic 1 (MEA = 1, MSKA3 = 1, CSA3 = 0). PA7 is configured as an output port (DDRA7 = 1). The software moderates the PWM output pulse width based on speed feedback data obtained from a tachometer or other such device. The tachometer typically would drive an input capture, providing data to the MCU from which velocity and acceleration information can be derived. The system could be modified to provide positional data for servo applications. The motor direction is determined by the current direction through it. Forward rotation requires Q4 (PA7) and Q2 (PA3) enabled. Reverse rotation requires Q3 (PA5) and Q1 (PA1) enabled.

The truth table shown in **Table 10-4** defines the H-bridge drive requirements for the motor from which the software would select based upon other system inputs.

The MC68HC705MC4 can be configured to drive two motors using both PWM channels.

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10.9.2 Brushless DC Motor Interface

A typical interface for a three-phase brushless DC motor is shown in **Figure 10-18**, although many other configurations are possible. The rotor sensor usually consists of a Hall effect sensor, optical encoder, or back-EMF detector. The coil current feedback is shown to be linear in this example, using the on-chip A/D to provide torque data to the MCU. Other systems may only require a current limit, which could be achieved with an interrupt pin (which will offer some hysteresis) and an external amplifier. With some reorganization of the I/O, it is also possible to configure the device to drive two brushless motors simultaneously. However, this will double the load on the processor. Depending upon the complexity of the control algorithms adopted, and considering that the commutation must be performed with software, care must be taken to maintain commutation delays to within acceptable limits. The commutation would follow the sequence shown in **Table 10-5**.

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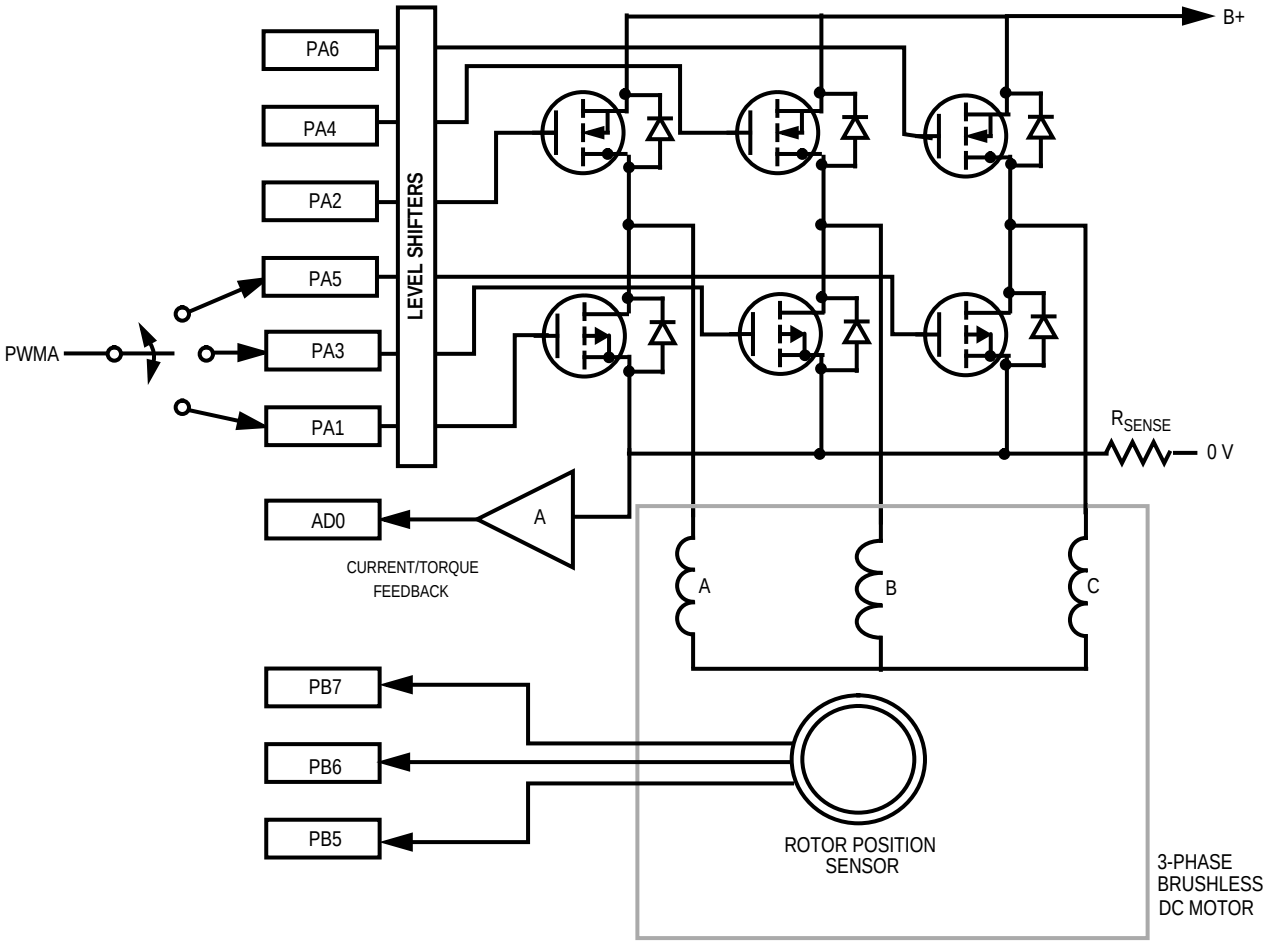

Figure 10-18. 3-Phase Brushless DC Motor Interface

Table 10-5. Brushless DC Motor Commutation Sequence

Motor Phase	0	1	2	3	4	5
Phase A Top Phase A Bottom	Off PWM	Off PWM	Off Off	On Off	On Off	Off Off
Phase B Top Phase B Bottom	On Off	Off Off	Off PWM	Off PWM	Off Off	On Off
Phase C Top Phase C Bottom	Off Off	On Off	On Off	Off Off	Off PWM	Off PWM

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Section 11. Serial Communications Interface

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11.2 Introduction

The serial communications interface (SCI) module allows high-speed asynchronous communication with peripheral devices and other MCUs.

11.3 Features

Features of the SCI module include:

- Standard Mark/Space Nonreturn-to-Zero Format
- Full Duplex Operation
- 32 Programmable Baud Rates
- Programmable 8-Bit or 9-Bit Character Length
- Separately Enabled Transmitter and Receiver
- Two Receiver Wakeup Methods:
  - Idle Line Wakeup
  - Address Mark Wakeup
- Interrupt-Driven Operation Capability with Five Interrupt Flags:
  - Transmitter Data Register Empty
  - Transmission Complete
  - Receiver Data Register Full
  - Receiver Overrun
  - Idle Receiver Input
- Receiver Framing Error Detection
- 1/16 Bit-Time Noise Detection

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11.4 SCI Data Format

The SCI uses the standard nonreturn-to-zero mark/space data format illustrated in **Figure 11-1**.

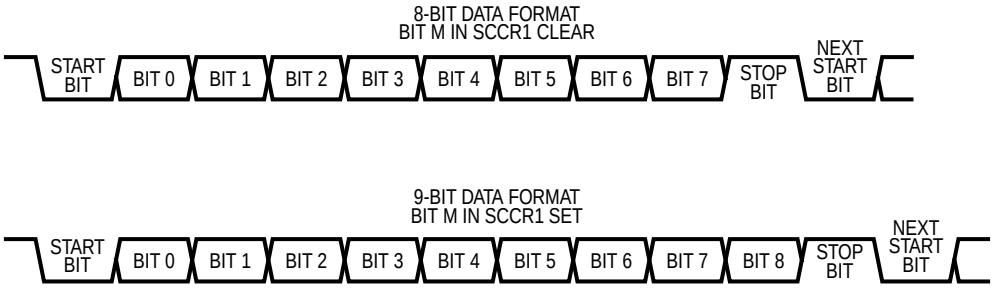

Figure 11-1. SCI Data Format

11.5 SCI Operation

The SCI allows full-duplex, asynchronous, RS232 or RS422 serial communication between the MCU and remote devices, including other MCUs. The transmitter and receiver of the SCI operate independently, although they use the same baud-rate generator. The following paragraphs describe the operation of the SCI transmitter and receiver.

11.5.1 Transmitter

Figure 11-2 shows the structure of the SCI transmitter.

11.5.1.1 Character Length

The transmitter can accommodate either 8-bit or 9-bit data. The state of the M bit in SCI control register 1 (SCCR1) determines character length. When transmitting 9-bit data, bit T8 in SCCR1 is the ninth bit (bit 8).

11.5.1.2 Character Transmission

During transmission, the transmit shift register shifts a character out to the PB4/TDO pin. At this time, the SCI data register (SCDR) is the write-only buffer between the internal data bus and the transmit shift register.

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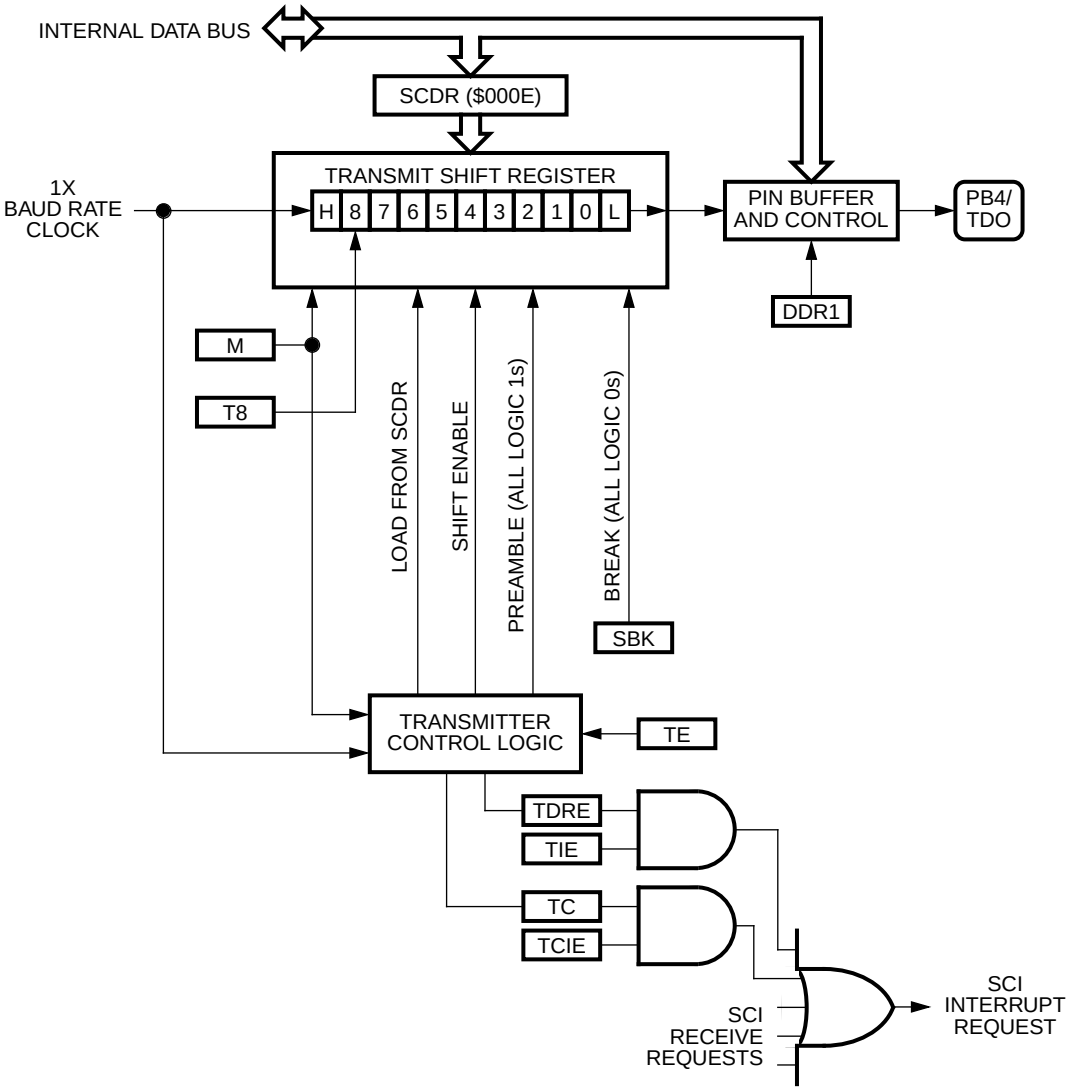

	7	6	5	4	3	2	1	0	
BAUD RATE REGISTER (BAUD)			SCP1	SCP0		SCR2	SCR1	SCR0	$000A
SCI CONTROL REGISTER 1 (SCCR1)	R8	T8		M	WAKE				$000B
SCI CONTROL REGISTER 2 (SCCR2)	TIE	TCIE	RIE	ILIE	TE	RE	RWU	SBK	$000C
SCI STATUS REGISTER (SCSR)	TDRE	TC	RDRF	IDLE	OR	NF	FE	0	$000D
SCI DATA REGISTER (SCDR)	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	$000E

Figure 11-2. SCI Transmitter

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Writing a logic 1 to the TE bit in SCI control register 2 (SCCR2), and then writing data to the SCDR, begins the transmission. At the start of a transmission, transmitter control logic automatically loads the transmit shift register with a preamble of logic 1s. After the preamble shifts out, the control logic transfers the SCDR data into the shift register. A logic 0 start bit automatically goes into the least significant bit position of the shift register, and a logic 1 stop bit goes into the most significant bit position.

When the data in the SCDR transfers to the transmit shift register, the transmit data register empty (TDRE) flag in the SCI status register (SCSR) becomes set. The TDRE flag indicates that the SCDR can accept new data from the internal data bus.

When the shift register is not transmitting a character, the PB4/TDO (transmit data out) pin goes to the idle condition, logic 1. If software clears the TE bit during the idle condition and while TDRE is set, the transmitter relinquishes control of the PB4/TDO pin (acting as a three-stated input port pin).

11.5.1.3 Break Characters

Writing a logic 1 to the SBK bit in SCCR2 loads the shift register with a break character. A break character contains all logic 0s and has no start and stop bits. Break character length depends on the M bit in SCCR1. As long as SBK is at logic 1, transmitter logic continuously loads break characters into the shift register. After software clears the SBK bit, the shift register finishes transmitting the last break character and then transmits at least one logic 1. The automatic logic 1 at the end of a break character is to guarantee the recognition of the start bit of the next character.

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11.5.1.4 Idle Characters

An idle character contains all logic 1s and has no start or stop bits. Idle character length depends on the M bit in SCCR1. The preamble is a synchronizing idle character that begins every transmission.

Clearing the TE bit during a transmission relinquishes the PB4/TDO pin after the last character to be transmitted is shifted out. The last character may already be in the shift register, or waiting in the SCDR, or a break character generated by writing to the SBK bit. Toggling TE from logic 0 to logic 1 while the last character is in transmission generates an idle character (a preamble) that allows the receiver to maintain control of the PB4/TDO pin.

11.5.1.5 Transmitter Interrupts

All SCI interrupt sources share the same interrupt vector at address $0FF2. The following sources can generate SCI transmitter interrupt requests:

- Transmit Data Register Empty (TDRE) — The TDRE bit in the SCSR indicates that the SCDR has transferred a character to the transmit shift register. TDRE is a source of SCI interrupt requests. The transmission interrupt enable bit (TIE) in SCCR2 is the local mask for TDRE interrupts.
- Transmission Complete (TC) — The TC bit in the SCSR indicates that both the transmit shift register and the SCDR are empty and that no break or idle character has been generated. TC is a source of SCI interrupt requests. The transmission complete interrupt enable bit (TCIE) in SCCR2 is the local mask for TC interrupts.

11.5.2 Receiver

Figure 11-3 shows the structure of the SCI receiver.

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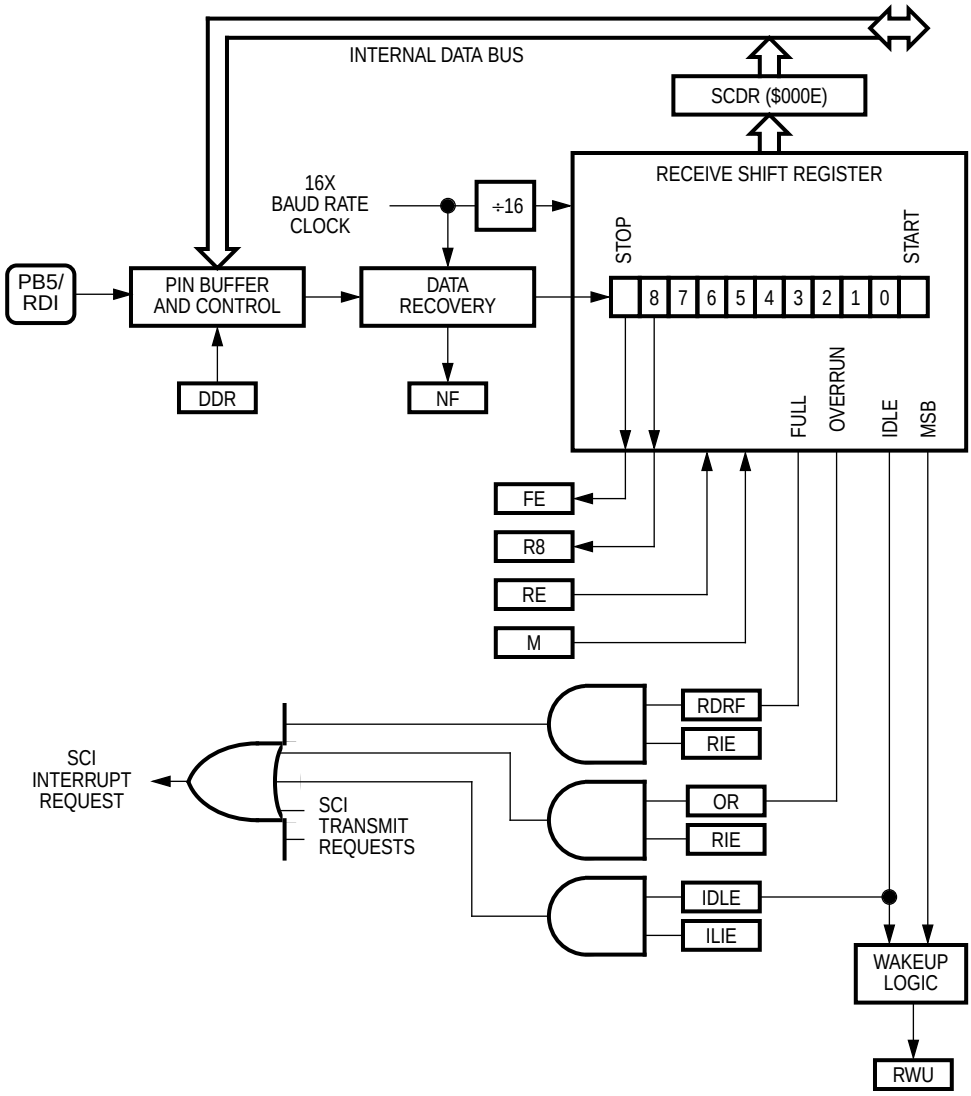

	7	6	5	4	3	2	1	0	
BAUD RATE REGISTER (BAUD)			SCP1	SCP0		SCR2	SCR1	SCR0	$000A
SCI CONTROL REGISTER 1 (SCCR1)	R8	T8		M	WAKE				$000B
SCI CONTROL REGISTER 2 (SCCR2)	TIE	TCIE	RIE	ILIE	TE	RE	RWU	SBK	$000C
SCI STATUS REGISTER (SCSR)	TDRE	TC	RDRF	IDLE	OR	NF	FE	0	$000D
SCI DATA REGISTER (SCDR)	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	$000E

Figure 11-3. SCI Receiver

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11.5.2.1 Character Length

The receiver can accommodate either 8-bit or 9-bit data. The state of the M bit in SCI control register 1 (SCCR1) determines character length. When receiving 9-bit data, bit R8 in SCCR1 is the ninth bit (bit 8).

11.5.2.2 Character Reception

During reception, the receive shift register shifts characters in from the PB5/RDI (receive data input) pin. The SCI data register (SCDR) is the read-only buffer between the internal data bus and the receive shift register.

After a complete character shifts into the receive shift register, the data portion of the character is transferred to the SCDR, setting the receive data register full (RDRF) flag. The RDRF flag can be used to generate an interrupt.

11.5.2.3 Receiver Wakeup

So that the MCU can ignore transmissions intended only for other receivers in multiple-receiver systems, the MCU can be put into a standby state. Setting the receiver wakeup enable (RWU) bit in SCI control register 2 (SCCR2) puts the MCU into a standby state during which receiver interrupts are disabled.

Either of two conditions on the PB5/RDI pin can bring the MCU out of the standby state:

- Idle input line condition — If the PB5/RDI pin is at logic 1 long enough for 10 or 11 logic 1s to shift into the receive shift register, receiver interrupts are again enabled.
- Address mark — If a logic 1 occurs in the most significant bit position of a received character, receiver interrupts are again enabled.

The state of the WAKE bit in SCCR1 determines which of the two conditions wakes up the MCU.

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11.5.2.4 Receiver Noise Immunity

The data recovery logic samples each bit 16 times to identify and verify the start bit and to detect noise. Any conflict between noise-detection samples sets the noise flag (NF) in the SCSR. The NF bit is set at the same time that the RDRF bit is set.

11.5.2.5 Framing Errors

If the data recovery logic does not detect a logic 1 where the stop bit should be in an incoming character, it sets the framing error (FE) bit in the SCSR. The FE bit is set at the same time that the RDRF bit is set.

11.5.2.6 Receiver Interrupts

All SCI interrupt sources share the same interrupt vector at address $0FF2. The following sources can generate SCI receiver interrupt requests:

- Receive Data Register Full (RDRF) — The RDRF bit in the SCSR indicates that the receive shift register has transferred a character to the SCDR.
- Receiver Overrun (OR) — The OR bit in the SCSR indicates that the receive shift register shifted in a new character before the previous character was read from the SCDR.
- Idle Input (IDLE) — The IDLE bit in the SCSR indicates that 10 or 11 consecutive logic 1s shifted in from the PD5/RDI pin.

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11.6 SCI I/O Registers

The following I/O registers control and monitor SCI operation:

- SCI Data Register (SCDR)
- SCI Control Register 1 (SCCR1)
- SCI Control Register 2 (SCCR2)
- SCI Status Register (SCSR)

11.6.1 SCI Data Register

The SCI data register is the buffer for characters received and for characters transmitted.

Address: $000E

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Write:								
Reset:	Unaffected by Reset							

Figure 11-4. SCI Data Register (SCDR)

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11.6.2 SCI Control Register 1

SCI control register 1 has the following functions:

- Stores ninth SCI data bit received and ninth SCI data bit transmitted
- Controls SCI character length
- Controls SCI wakeup method

Address: $000B

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	R8		0	M	WAKE	0	0	0
Write:		T8						
Reset:	Unaffected by Reset							

= Unimplemented

Figure 11-5. SCI Control Register 1 (SCCR1)

R8 — Bit 8 (Received)

When the SCI is receiving 9-bit characters, R8 is the ninth bit of the received character. R8 receives the ninth bit at the same time that the SCDR receives the other eight bits. Reset has no effect on the R8 bit.

T8 — Bit 8 (Transmitted)

When the SCI is transmitting 9-bit characters, T8 is the ninth bit of the transmitted character. T8 is loaded into the transmit shift register at the same time that SCDR is loaded into the transmit shift register. Reset has no effect on the T8 bit.

M — Character Length

This read/write bit determines whether SCI characters are eight bits long or nine bits long. The ninth bit can be used as an extra stop bit, as a receiver wakeup signal, or as a mark or space parity bit. Reset has no effect on the M bit.

1 = 9-bit SCI characters
0 = 8-bit SCI characters

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WAKE — Wakeup Bit

This read/write bit determines which condition wakes up the SCI: a logic 1 (address mark) in the most significant bit position of a received character or an idle condition of the PD5/RDI pin. Reset has no effect on the WAKE bit.

1 = Address mark wakeup
0 = Idle line wakeup

11.6.3 SCI Control Register 2

SCI control register 2 has the following functions:

- Enables the SCI receiver and SCI receiver interrupts
- Enables the SCI transmitter and SCI transmitter interrupts
- Enables SCI receiver idle interrupts
- Enables SCI transmission complete interrupts
- Enables SCI wakeup
- Transmits SCI break characters

Address: $000C

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	TIE	TCIE	RIE	ILIE	TE	RE	RWU	SBK
Reset:	0	0	0	0	0	0	0	0

Figure 11-6. SCI Control Register 2 (SCCR2)

TIE — Transmit Interrupt Enable

This read/write bit enables SCI interrupt requests when the TDRE bit becomes set. Reset clears the TIE bit.

1 = TDRE interrupt requests enabled
0 = TDRE interrupt requests disabled

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TCIE — Transmission Complete Interrupt Enable

This read/write bit enables SCI interrupt requests when the TC bit becomes set. Reset clears the TCIE bit.

1 = TC interrupt requests enabled
0 = TC interrupt requests disabled

RIE — Receive Interrupt Enable

This read/write bit enables SCI interrupt requests when the RDRF bit or the OR bit becomes set. Reset clears the RIE bit.

1 = RDRF interrupt requests enabled
0 = RDRF interrupt requests disabled

ILIE — Idle Line Interrupt Enable

This read/write bit enables SCI interrupt requests when the IDLE bit becomes set. Reset clears the ILIE bit.

1 = IDLE interrupt requests enabled
0 = DLE interrupt requests disabled

TE — Transmit Enable

Setting this read/write bit begins the transmission by sending a preamble of 10 or 11 logic 1s from the transmit shift register to the PB4/TDO pin. Reset clears the TE bit.

1 = Transmission enabled
0 = Transmission disabled

RE — Receive Enable

Setting this read/write bit enables the receiver. Clearing the RE bit disables the receiver and receiver interrupts but does not affect the receiver interrupt flags. Reset clears the RE bit.

1 = Receiver enabled
0 = Receiver disabled

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RWU — Receiver Wakeup Enable

This read/write bit puts the receiver in a standby state. Typically, data transmitted to the receiver clears the RWU bit and returns the receiver to normal operation. The WAKE bit in SCCR1 determines whether an idle input or an address mark brings the receiver out of the standby state. Reset clears the RWU bit.

1 = Standby state
0 = Normal operation

SBK — Send Break

Setting this read/write bit continuously transmits break codes in the form of 10-bit or 11-bit groups of logic 0s. Clearing the SBK bit stops the break codes and transmits a logic 1 as a start bit. Reset clears the SBK bit.

1 = Break codes being transmitted
0 = No break codes being transmitted

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11.6.4 SCI Status Register

The SCI status register contains flags to signal the following conditions:

- Transfer of SCDR data to transmit shift register complete
- Transmission complete
- Transfer of receive shift register data to SCDR complete
- Receiver input idle
- Receiver overrun
- Noisy data
- Framing error

Address: $000D

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	TDRE	TC	RDRF	IDLE	OR	NF	FE	0
Write:								
Reset:	1	1	0	0	0	0	0	U

= Unimplemented U = Unaffected

Figure 11-7. SCI Status Register (SCSR)

TDRE — Transmit Data Register Empty

This clearable, read-only bit is set when the data in the SCDR transfers to the transmit shift register. TDRE generates an interrupt request if the TIE bit in SCCR2 is also set. Clear the TDRE bit by reading the SCSR with TDRE set, and then writing to the SCDR. Reset sets the TDRE bit. Software must initialize the TDRE bit to logic 0 to avoid an instant interrupt request when turning on the transmitter.

1 = SCDR data transferred to transmit shift register
0 = SCDR data not transferred to transmit shift register

TC — Transmission Complete

This clearable, read-only bit is set when the TDRE bit is set, and no data, preamble, or break character is being transmitted. TC generates an interrupt request if the TCIE bit in SCCR2 is also set. Clear the TC bit by reading the SCSR with TC set, and then writing to the SCDR.

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Reset sets the TC bit. Software must initialize the TC bit to logic 0 to avoid an instant interrupt request when turning on the transmitter.

1 = No transmission in progress
0 = Transmission in progress

RDRF — Receive Data Register Full

This clearable, read-only bit is set when the data in the receive shift register transfers to the SCI data register. RDRF generates an interrupt request if the RIE bit in SCCR2 is also set. Clear the RDRF bit by reading the SCSR with RDRF set, and then reading the SCDR. Reset clears the RDRF bit.

1 = Received data available in SCDR
0 = Received data not available in SCDR

IDLE — Receiver Idle

This clearable, read-only bit is set when 10 or 11 consecutive logic 1s appear on the receiver input. IDLE generates an interrupt request if the ILIE bit in SCCR2 is also set. Clear the IDLE bit by reading the SCSR with IDLE set, and then reading the SCDR. Reset clears the IDLE bit.

1 = Receiver input idle
0 = Receiver input not idle

OR — Receiver Overrun

This clearable, read-only bit is set if the SCDR is not read before the receive shift register receives the next word. OR generates an interrupt request if the RIE bit in SCCR2 is also set. The data in the shift register is lost, but the data already in the SCDR is not affected. Clear the OR bit by reading the SCSR with OR set, and then reading the SCRD. Reset clears the OR bit.

1 = Receiver shift register full and RDRF = 1
0 = No receiver overrun

NF — Receiver Noise Flag

This clearable, read-only bit is set when noise is detected in data received in the SCI data register. Clear the NF bit by reading the SCSR, and then reading the SCDR. Reset clears the NF bit.

1 = Noise detected in SCDR
0 = No noise detected in SCDR

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FE — Receiver Framing Error

This clearable, read-only flag is set when there is a logic 0 where a stop bit should be in the character shifted into the receive shift register. If the received word causes both a framing error and an overrun error, the OR bit is set and the FE bit is not set. Clear the FE bit by reading the SCSR, and then reading the SCDR. Reset clears the FE bit.

1 = Framing error
0 = No framing error

11.6.5 Baud Rate Register

The baud rate register selects the baud rate for both the receiver and the transmitter.

Address: $000A

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	0	SCP1	SCP0	0	SCR2	SCR1	SCR0
Write:								
Reset:	U	U	0	0	U	U	U	U

= Unimplemented U = Unaffected

Figure 11-8. Baud Rate Register (BAUD)

SCP1 and SCP0 — SCI Prescaler Select Bits

These read/write bits control prescaling of the baud rate generator clock, as shown in **Table 11-1**. Resets clear both SCP1 and SCP0.

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Table 11-1. Baud Rate Generator Clock Prescaling

SCP[1:0]	Baud Rate Generator Clock
00	Internal Clock ÷ 1
01	Internal Clock ÷ 3
10	Internal Clock ÷ 4
11	Internal Clock ÷ 13

SCR2–SCR0 — SCI Baud Rate Select Bits

These read/write bits select the SCI baud rate, as shown in **Table 11-2**. Reset has no effect on the SCR2–SCR0 bits.

Table 11-2. Baud Rate Selection

SCR[2:1:0]	SCI Baud Rate (Baud)
000	Prescaled Clock ÷ 1
001	Prescaled Clock ÷ 2
010	Prescaled Clock ÷ 4
011	Prescaled Clock ÷ 8
100	Prescaled Clock ÷ 16
101	Prescaled Clock ÷ 32
110	Prescaled Clock ÷ 64
111	Prescaled Clock ÷ 128

Table 11-3 shows all possible SCI baud rates derived from crystal frequencies of 2 MHz, 4 MHz, 4.194304 MHz, and 6 MHz.

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Table 11-3. Baud Rate Selection Examples

SCP[1:0]	SCR[2:1:0]	SCI Baud Rate		
		f_{OSC} = 4 MHz f_{OP} = 2 MHz	f_{OSC} = 4.194304 MHz f_{OP} = 2.097152 MHz	f_{OSC} = 6 MHz f_{OP} = 3 MHz
00	000	125 kBaud	131.1 kBaud	187.5 kBaud
00	001	62.50 kBaud	65.54 kBaud	93.75 kBaud
00	010	31.25 kBaud	32.77 kBaud	46.89 kBaud
00	011	15.63 kBaud	16.38 kBaud	23.44 kBaud
00	100	7813 Baud	8192 Baud	11.72 kBaud
00	101	3906 Baud	4096 Baud	5859 Baud
00	110	1953 Baud	2048 Baud	2930 Baud
00	111	976.6 Baud	1024 Baud	1465 Baud
01	000	41.67 kBaud	43.69 kBaud	62.49 kBaud
01	001	20.83 kBaud	21.85 kBaud	31.26 kBaud
01	010	10.42 kBaud	10.92 kBaud	15.62 kBaud
01	011	5208 Baud	5461 Baud	7812 Baud
01	100	2604 Baud	2731 Baud	3906 Baud
01	101	1302 Baud	1365 Baud	1953 Baud
01	110	651.0 Baud	682.7 Baud	976.5 Baud
01	111	325.5 Baud	341.3 Baud	488.4 Baud
10	000	31.25 kBaud	32.77 kBaud	46.89 kBaud
10	001	15.63 kBaud	16.38 kBaud	23.44 kBaud
10	010	7813 Baud	8192 Baud	11.72 kBaud
10	011	3906 Baud	4906 Baud	5859 Baud
10	100	1953 Baud	2048 Baud	2930 Baud
10	101	976.6 Baud	1024 Baud	1465 Baud
10	110	488.3 Baud	512.0 Baud	732.3 Baud
10	111	244.1 Baud	256.0 Baud	366.3 Baud
11	000	9615 Baud	10.08 kBaud	14.42 kBaud
11	001	4808 Baud	5041 Baud	7212 Baud
11	010	2404 Baud	2521 Baud	3606 Baud
11	011	1202 Baud	1260 Baud	1803 Baud
11	100	601.0 Baud	630.2 Baud	901.5 Baud
11	101	300.5 Baud	315.1 Baud	450.6 Baud
11	110	150.2 Baud	157.5 Baud	225.4 Baud
11	111	75.12 Baud	78.77 Baud	112.7 Baud

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Section 12. Core Timer

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12.2 Introduction

The core timer (Ctimer) for this device is a 15-stage multi-functional ripple counter. The features include timer overflow, power-on reset (POR), real time interrupt, and COP watchdog timer

As seen in **Figure 12-1**, the core timer is driven by the internal bus clock divided by four as a fixed prescaler. This signal drives an 8-bit ripple counter. The value of this 8-bit ripple counter can be read by the CPU at any time by accessing the Ctimer counter register (CTCR) at address $09. A timer overflow function is implemented on the last stage of this counter, giving a possible interrupt at the rate of E/1024. Two additional stages produce the POR function at E/4064. The timer counter bypass circuitry (available only in test mode) is at this point in the timer chain. This circuit is followed by one more stage, with the resulting clock (E/8192) driving the real-time interrupt circuit. The RTI circuit consists of four divider stages with a 1-of-4 selector. The output of the RTI circuit is further divided by eight to drive the mask optional COP watchdog timer circuit. The RTI rate selector bits and the RTI and CTOF enable bits and flags are located in the Ctimer control and status register (CTCSR) at location $08.

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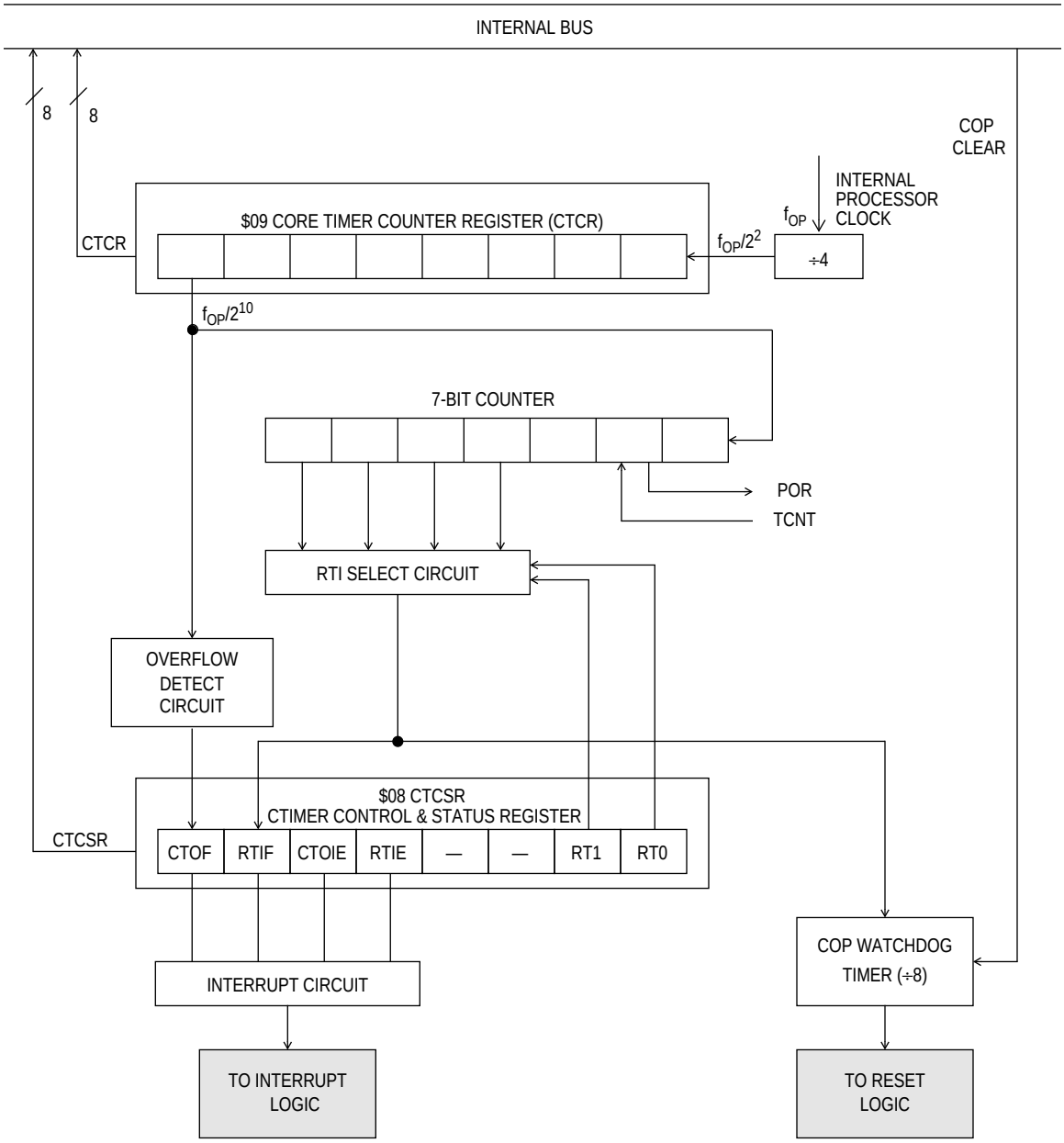

Figure 12-1. Core Timer Block Diagram

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12.3 Ctimer Control and Status Register

The CTCSR contains the timer interrupt flag, the timer interrupt enable bits, and the real-time interrupt rate select bits. **Figure 12-2** shows the value of each bit in the CTCSR when coming out of reset.

Address: $0008

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	CTOF	RTIF	CTOIE	RTIE	0	0	RT1	RT0
Write:								
Reset:	0	0	0	0	0	0	1	1

= Unimplemented

Figure 12-2. Core Timer Control and Status Register (CTCSR)

CTOF — Core Timer Overflow Flag

CTOF is a clearable, read-only status bit and is set when the 8-bit ripple counter rolls over from $FF to $00. A CPU interrupt request will be generated if CTOIE is set. Clearing the CTOF is done by writing a 0 to it. Writing a 1 to CTOF has no effect on the bit's value. Reset clears CTOF.

RTIF — Real-Time Interrupt Flag

The real-time interrupt circuit consists of a four stage divider and a 1-of-4 selector. The clock frequency that drives the RTI circuit is $E/2^{13}$ (or E/8192) with four additional divider stages giving a maximum interrupt period of four seconds at a crystal frequency of 32.768 kHz. RTIF is a clearable, read-only status bit and is set when the output of the chosen (1-of-4 selection) stage goes active. A CPU interrupt request will be generated if RTIE is set. Clearing the RTIF is done by writing a 0 to it. Writing a 1 to RTIF has no effect on this bit. Reset clears RTIF.

CTOIE — Core Timer Overflow Interrupt Enable

When this bit is set, a CPU interrupt request is generated when the CTOF bit is set. Reset clears this bit.

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RTIE — Real-Time Interrupt Enable

When this bit is set, a CPU interrupt request is generated when the RTIF bit is set. Reset clears this bit.

RT1:RT0 — Real-Time Interrupt Rate Select

These two bits select 1-of-4 taps from the real-time interrupt circuit. **Table 12-1** shows the available interrupt rates with several f_{OP} values. Reset sets these RT0 and RT1, selecting the lowest periodic rate and therefore the maximum time in which to alter these bits if necessary. Care should be taken when altering RT0 and RT1 if the time-out period is imminent or uncertain. If the selected tap is modified during a cycle in which the counter is switching, an RTIF could be missed or an additional one could be generated. To avoid problems, the COP should be cleared before changing RTI taps.

Table 12-1. RTI Rates

RT1:RT0	RTI Rates at Bus Frequency of:		
	16.384 kHz	3.0 MHz	Divide Ratio
00	1 sec	5.5 ms	2^{14}
01	2 sec	10.9 ms	2^{15}
10	3 sec	21.8 ms	2^{16}
11	8 sec	43.75 ms	2^{17}

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12.4 Computer Operating Properly (COP) Watchdog Reset

The COP watchdog timer function is implemented on this device by using the output of the RTI circuit and further dividing it by eight. The minimum COP reset rates are listed in **Table 12-2**. If the COP circuit times out, an internal reset is generated and the normal reset vector is fetched. Preventing a COP timeout is done by writing a 0 to bit 0 of address $0FF0. When the COP is cleared, only the final divide-by-eight stage (output of the RTI) is cleared. This function is a mask option.

Table 12-2. Minimum COP Reset Times

RT1:RT0	Minimum COP Reset at Bus Frequency:		
	16.384 kHz	3.0 MHz	f_{op}
00	7 sec	38.2 ms	7 × (RTI Rate)
01	14 sec	76.5 ms	7 × (RTI Rate)
10	28 sec	153.0 ms	7 × (RTI Rate)
11	56 sec	305.9 ms	7 × (RTI Rate)

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12.5 Ctimer Counter Register

The core timer counter register is a read-only register that contains the current value of the 8-bit ripple counter at the beginning of the timer chain. This counter is clocked at f_{op} divided by 4 and can be used for various functions including a software input capture. Extended time periods can be attained using the CTOF function to increment a temporary RAM storage location, thereby simulating a 16-bit (or more) counter.

Address: $0009

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	CTCR7	CTCR6	CTCR5	CTCR4	CTCR3	CTCR2	CTCR1	CTCR0
Reset:	1	1	1	1	1	1	1	1

Figure 12-3. Core Timer Counter Register (CTCR)

The power-on cycle clears the entire counter chain and begins clocking the counter. After 4064 cycles, the power-on reset circuit is released that again clears the counter chain and allows the device to come out of reset. At this point, if $\overline{\text{RESET}}$ is not asserted, the timer will start counting up from zero and normal device operation will begin. When $\overline{\text{RESET}}$ is asserted anytime during operation (other than POR), the counter chain will be cleared.

12.6 Core Timer during Wait Mode

The CPU clock halts during wait mode, but the timer remains active. If the interrupts are enabled, the timer interrupt will cause the processor to exit wait mode.

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Section 13. Instruction Set

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13.2 Introduction

The MCU instruction set has 62 instructions and uses eight addressing modes. The instructions include all those of the M146805 CMOS Family plus one more: the unsigned multiply (MUL) instruction. The MUL instruction allows unsigned multiplication of the contents of the accumulator (A) and the index register (X). The high-order product is stored in the index register, and the low-order product is stored in the accumulator.

13.3 Addressing Modes

The CPU uses eight addressing modes for flexibility in accessing data. The addressing modes provide eight different ways for the CPU to find the data required to execute an instruction. The eight addressing modes are:

- Inherent
- Immediate
- Direct
- Extended
- Indexed, no offset
- Indexed, 8-bit offset
- Indexed, 16-bit offset
- Relative

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13.3.1 Inherent

Inherent instructions are those that have no operand, such as return from interrupt (RTI) and stop (STOP). Some of the inherent instructions act on data in the CPU registers, such as set carry flag (SEC) and increment accumulator (INCA). Inherent instructions require no operand address and are one byte long.

13.3.2 Immediate

Immediate instructions are those that contain a value to be used in an operation with the value in the accumulator or index register. Immediate instructions require no operand address and are two bytes long. The opcode is the first byte, and the immediate data value is the second byte.

13.3.3 Direct

Direct instructions can access any of the first 256 memory locations with two bytes. The first byte is the opcode, and the second is the low byte of the operand address. In direct addressing, the CPU automatically uses $00 as the high byte of the operand address.

13.3.4 Extended

Extended instructions use three bytes and can access any address in memory. The first byte is the opcode; the second and third bytes are the high and low bytes of the operand address.

When using the Freescale assembler, the programmer does not need to specify whether an instruction is direct or extended. The assembler automatically selects the shortest form of the instruction.

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13.3.5 Indexed, No Offset

Indexed instructions with no offset are 1-byte instructions that can access data with variable addresses within the first 256 memory locations. The index register contains the low byte of the effective address of the operand. The CPU automatically uses $00 as the high byte, so these instructions can address locations $0000–$00FF.

Indexed, no offset instructions are often used to move a pointer through a table or to hold the address of a frequently used RAM or I/O location.

13.3.6 Indexed, 8-Bit Offset

Indexed, 8-bit offset instructions are 2-byte instructions that can access data with variable addresses within the first 511 memory locations. The CPU adds the unsigned byte in the index register to the unsigned byte following the opcode. The sum is the effective address of the operand. These instructions can access locations $0000–$01FE.

Indexed 8-bit offset instructions are useful for selecting the kth element in an n-element table. The table can begin anywhere within the first 256 memory locations and could extend as far as location 510 ($01FE). The k value is typically in the index register, and the address of the beginning of the table is in the byte following the opcode.

13.3.7 Indexed,16-Bit Offset

Indexed, 16-bit offset instructions are 3-byte instructions that can access data with variable addresses at any location in memory. The CPU adds the unsigned byte in the index register to the two unsigned bytes following the opcode. The sum is the effective address of the operand. The first byte after the opcode is the high byte of the 16-bit offset; the second byte is the low byte of the offset.

Indexed, 16-bit offset instructions are useful for selecting the kth element in an n-element table anywhere in memory.

As with direct and extended addressing, the Freescale assembler determines the shortest form of indexed addressing.

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13.3.8 Relative

Relative addressing is only for branch instructions. If the branch condition is true, the CPU finds the effective branch destination by adding the signed byte following the opcode to the contents of the program counter. If the branch condition is not true, the CPU goes to the next instruction. The offset is a signed, two's complement byte that gives a branching range of –128 to +127 bytes from the address of the next location after the branch instruction.

When using the Freescale assembler, the programmer does not need to calculate the offset, because the assembler determines the proper offset and verifies that it is within the span of the branch.

13.4 Instruction Types

The MCU instructions fall into the following five categories:

- Register/Memory Instructions
- Read-Modify-Write Instructions
- Jump/Branch Instructions
- Bit Manipulation Instructions
- Control Instructions

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13.4.1 Register/Memory Instructions

These instructions operate on CPU registers and memory locations. Most of them use two operands. One operand is in either the accumulator or the index register. The CPU finds the other operand in memory.

Table 13-1. Register/Memory Instructions

Instruction	Mnemonic
Add Memory Byte and Carry Bit to Accumulator	ADC
Add Memory Byte to Accumulator	ADD
AND Memory Byte with Accumulator	AND
Bit Test Accumulator	BIT
Compare Accumulator	CMP
Compare Index Register with Memory Byte	CPX
EXCLUSIVE OR Accumulator with Memory Byte	EOR
Load Accumulator with Memory Byte	LDA
Load Index Register with Memory Byte	LDX
Multiply	MUL
OR Accumulator with Memory Byte	ORA
Subtract Memory Byte and Carry Bit from Accumulator	SBC
Store Accumulator in Memory	STA
Store Index Register in Memory	STX
Subtract Memory Byte from Accumulator	SUB

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13.4.2 Read-Modify-Write Instructions

These instructions read a memory location or a register, modify its contents, and write the modified value back to the memory location or to the register.

NOTE: *Do not use read-modify-write operations on write-only registers.*

Table 13-2. Read-Modify-Write Instructions

Instruction	Mnemonic
Arithmetic Shift Left (Same as LSL)	ASL
Arithmetic Shift Right	ASR
Bit Clear	BCLR(1)
Bit Set	BSET(1)
Clear Register	CLR
Complement (One's Complement)	COM
Decrement	DEC
Increment	INC
Logical Shift Left (Same as ASL)	LSL
Logical Shift Right	LSR
Negate (Two's Complement)	NEG
Rotate Left through Carry Bit	ROL
Rotate Right through Carry Bit	ROR
Test for Negative or Zero	TST(2)

1. Unlike other read-modify-write instructions, BCLR and BSET use only direct addressing.
2. TST is an exception to the read-modify-write sequence because it does not write a replacement value.

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13.4.3 Jump/Branch Instructions

Jump instructions allow the CPU to interrupt the normal sequence of the program counter. The unconditional jump instruction (JMP) and the jump-to-subroutine instruction (JSR) have no register operand. Branch instructions allow the CPU to interrupt the normal sequence of the program counter when a test condition is met. If the test condition is not met, the branch is not performed.

The BRCLR and BRSET instructions cause a branch based on the state of any readable bit in the first 256 memory locations. These 3-byte instructions use a combination of direct addressing and relative addressing. The direct address of the byte to be tested is in the byte following the opcode. The third byte is the signed offset byte. The CPU finds the effective branch destination by adding the third byte to the program counter if the specified bit tests true. The bit to be tested and its condition (set or clear) is part of the opcode. The span of branching is from –128 to +127 from the address of the next location after the branch instruction. The CPU also transfers the tested bit to the carry/borrow bit of the condition code register.

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Table 13-3. Jump and Branch Instructions

Instruction	Mnemonic
Branch if Carry Bit Clear	BCC
Branch if Carry Bit Set	BCS
Branch if Equal	BEQ
Branch if Half-Carry Bit Clear	BHCC
Branch if Half-Carry Bit Set	BHCS
Branch if Higher	BHI
Branch if Higher or Same	BHS
Branch if $\overline{\text{IRQ}}$ Pin High	BIH
Branch if $\overline{\text{IRQ}}$ Pin Low	BIL
Branch if Lower	BLO
Branch if Lower or Same	BLS
Branch if Interrupt Mask Clear	BMC
Branch if Minus	BMI
Branch if Interrupt Mask Set	BMS
Branch if Not Equal	BNE
Branch if Plus	BPL
Branch Always	BRA
Branch if Bit Clear	BRCLR
Branch Never	BRN
Branch if Bit Set	BRSET
Branch to Subroutine	BSR
Unconditional Jump	JMP
Jump to Subroutine	JSR

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13.4.4 Bit Manipulation Instructions

The CPU can set or clear any writable bit in the first 256 bytes of memory, which includes I/O registers and on-chip RAM locations. The CPU can also test and branch based on the state of any bit in any of the first 256 memory locations.

Table 13-4. Bit Manipulation Instructions

Instruction	Mnemonic
Bit Clear	BCLR
Branch if Bit Clear	BRCLR
Branch if Bit Set	BRSET
Bit Set	BSET

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13.4.5 Control Instructions

These instructions act on CPU registers and control CPU operation during program execution.

Table 13-5. Control Instructions

Instruction	Mnemonic
Clear Carry Bit	CLC
Clear Interrupt Mask	CLI
No Operation	NOP
Reset Stack Pointer	RSP
Return from Interrupt	RTI
Return from Subroutine	RTS
Set Carry Bit	SEC
Set Interrupt Mask	SEI
Stop Oscillator and Enable $\overline{\text{IRQ}}$ Pin	STOP
Software Interrupt	SWI
Transfer Accumulator to Index Register	TAX
Transfer Index Register to Accumulator	TXA
Stop CPU Clock and Enable Interrupts	WAIT

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13.5 Instruction Set Summary

Table 13-6. Instruction Set Summary

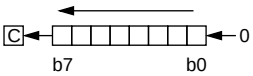
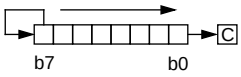
Source Form	Operation	Description	Effect on CCR					Address Mode	Opcode	Operand	Cycles
			H	I	N	Z	C				
ADC #*opr* ADC *opr* ADC *opr* ADC *opr*,X ADC *opr*,X ADC ,X	Add with Carry	A ← (A) + (M) + (C)	↕	—	↕	↕	↕	IMM DIR EXT IX2 IX1 IX	A9 B9 C9 D9 E9 F9	ii dd hh ll ee ff ff	2 3 4 5 4 3
ADD #*opr* ADD *opr* ADD *opr* ADD *opr*,X ADD *opr*,X ADD ,X	Add without Carry	A ← (A) + (M)	↕	—	↕	↕	↕	IMM DIR EXT IX2 IX1 IX	AB BB CB DB EB FB	ii dd hh ll ee ff ff	2 3 4 5 4 3
AND #*opr* AND *opr* AN*D opr* AND *opr*,X AND *opr*,X AND ,X	Logical AND	A ← (A) ∧ (M)	—	—	↕	↕	—	IMM DIR EXT IX2 IX1 IX	A4 B4 C4 D4 E4 F4	ii dd hh ll ee ff ff	2 3 4 5 4 3
ASL *opr* ASLA ASLX ASL *opr*,X ASL ,X	Arithmetic Shift Left (Same as LSL)		—	—	↕	↕	↕	DIR INH INH IX1 IX	38 48 58 68 78	dd ff 	5 3 3 6 5
ASR *opr* ASRA ASRX ASR *opr*,X ASR ,X	Arithmetic Shift Right		—	—	↕	↕	↕	DIR INH INH IX1 IX	37 47 57 67 77	dd ff 	5 3 3 6 5
BCC *rel*	Branch if Carry Bit Clear	PC ← (PC) + 2 + *rel* ? C = 0	—	—	—	—	—	REL	24	rr	3
BCLR *n opr*	Clear Bit n	Mn ← 0	—	—	—	—	—	DIR (b0) DIR (b1) DIR (b2) DIR (b3) DIR (b4) DIR (b5) DIR (b6) DIR (b7)	11 13 15 17 19 1B 1D 1F	dd dd dd dd dd dd dd dd	5 5 5 5 5 5 5 5
BCS *rel*	Branch if Carry Bit Set (Same as BLO)	PC ← (PC) + 2 + *rel* ? C = 1	—	—	—	—	—	REL	25	rr	3
BEQ *rel*	Branch if Equal	PC ← (PC) + 2 + *rel* ? Z = 1	—	—	—	—	—	REL	27	rr	3
BHCC *rel*	Branch if Half-Carry Bit Clear	PC ← (PC) + 2 + *rel* ? H = 0	—	—	—	—	—	REL	28	rr	3
BHCS *rel*	Branch if Half-Carry Bit Set	PC ← (PC) + 2 + *rel* ? H = 1	—	—	—	—	—	REL	29	rr	3
BHI *rel*	Branch if Higher	PC ← (PC) + 2 + *rel* ? C ∨ Z = 0	—	—	—	—	—	REL	22	rr	3
BHS *rel*	Branch if Higher or Same	PC ← (PC) + 2 + *rel* ? C = 0	—	—	—	—	—	REL	24	rr	3

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Table 13-6. Instruction Set Summary (Continued)

Source Form	Operation	Description	Effect on CCR					Address Mode	Opcode	Operand	Cycles
			H	I	N	Z	C				
BIH *rel*	Branch if IRQ Pin High	PC ← (PC) + 2 + *rel* ? IRQ = 1	—	—	—	—	—	REL	2F	rr	3
BIL *rel*	Branch if IRQ Pin Low	PC ← (PC) + 2 + *rel* ? IRQ = 0	—	—	—	—	—	REL	2E	rr	3
BIT #*opr* BIT *opr* BIT *opr* BIT *opr*,X BIT *opr*,X BIT ,X	Bit Test Accumulator with Memory Byte	(A) ∧ (M)	—	—	↕	↕	—	IMM DIR EXT IX2 IX1 IX	A5 B5 C5 D5 E5 F5	ii dd hh ll ee ff ff	2 3 4 5 4 3
BLO *rel*	Branch if Lower (Same as BCS)	PC ← (PC) + 2 + *rel* ? C = 1	—	—	—	—	—	REL	25	rr	3
BLS *rel*	Branch if Lower or Same	PC ← (PC) + 2 + *rel* ? C ∨ Z = 1	—	—	—	—	—	REL	23	rr	3
BMC *rel*	Branch if Interrupt Mask Clear	PC ← (PC) + 2 + *rel* ? I = 0	—	—	—	—	—	REL	2C	rr	3
BMI *rel*	Branch if Minus	PC ← (PC) + 2 + *rel* ? N = 1	—	—	—	—	—	REL	2B	rr	3
BMS *rel*	Branch if Interrupt Mask Set	PC ← (PC) + 2 + *rel* ? I = 1	—	—	—	—	—	REL	2D	rr	3
BNE *rel*	Branch if Not Equal	PC ← (PC) + 2 + *rel* ? Z = 0	—	—	—	—	—	REL	26	rr	3
BPL *rel*	Branch if Plus	PC ← (PC) + 2 + *rel* ? N = 0	—	—	—	—	—	REL	2A	rr	3
BRA *rel*	Branch Always	PC ← (PC) + 2 + *rel* ? 1 = 1	—	—	—	—	—	REL	20	rr	3
BRCLR *n opr rel*	Branch if Bit n Clear	PC ← (PC) + 2 + *rel* ? Mn = 0	—	—	—	—	↕	DIR (b0) DIR (b1) DIR (b2) DIR (b3) DIR (b4) DIR (b5) DIR (b6) DIR (b7)	01 03 05 07 09 0B 0D 0F	dd rr dd rr dd rr dd rr dd rr dd rr dd rr dd rr	5 5 5 5 5 5 5 5
BRN *rel*	Branch Never	PC ← (PC) + 2 + *rel* ? 1 = 0	—	—	—	—	—	REL	21	rr	3
BRSET *n opr rel*	Branch if Bit n Set	PC ← (PC) + 2 + *rel* ? Mn = 1	—	—	—	—	↕	DIR (b0) DIR (b1) DIR (b2) DIR (b3) DIR (b4) DIR (b5) DIR (b6) DIR (b7)	00 02 04 06 08 0A 0C 0E	dd rr dd rr dd rr dd rr dd rr dd rr dd rr dd rr	5 5 5 5 5 5 5 5
BSET *n opr*	Set Bit n	Mn ← 1	—	—	—	—	—	DIR (b0) DIR (b1) DIR (b2) DIR (b3) DIR (b4) DIR (b5) DIR (b6) DIR (b7)	10 12 14 16 18 1A 1C 1E	dd dd dd dd dd dd dd dd	5 5 5 5 5 5 5 5
BSR *rel*	Branch to Subroutine	PC ← (PC) + 2; push (PCL) SP ← (SP) – 1; push (PCH) SP ← (SP) – 1 PC ← (PC) + *rel*	—	—	—	—	—	REL	AD	rr	6
CLC	Clear Carry Bit	C ← 0	—	—	—	—	0	INH	98		2
CLI	Clear Interrupt Mask	I ← 0	—	0	—	—	—	INH	9A		2

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Table 13-6. Instruction Set Summary (Continued)

Source Form	Operation	Description	Effect on CCR					Address Mode	Opcode	Operand	Cycles
			H	I	N	Z	C				
CLR *opr* CLRA CLRX CLR *opr*,X CLR ,X	Clear Byte	M ← $00 A ← $00 X ← $00 M ← $00 M ← $00	—	—	0	1	—	DIR INH INH IX1 IX	3F 4F 5F 6F 7F	dd ff 	5 3 3 6 5
CMP #*opr* CMP *opr* CMP *opr* CMP *opr*,X CMP *opr*,X CMP ,X	Compare Accumulator with Memory Byte	(A) – (M)	—	—	↕	↕	↕	IMM DIR EXT IX2 IX1 IX	A1 B1 C1 D1 E1 F1	ii dd hh ll ee ff ff 	2 3 4 5 4 3
COM *opr* COMA COMX COM *opr*,X COM ,X	Complement Byte (One's Complement)	M ← ($\overline{M}$) = $FF – (M) A ← ($\overline{A}$) = $FF – (A) X ← ($\overline{X}$) = $FF – (X) M ← ($\overline{M}$) = $FF – (M) M ← ($\overline{M}$) = $FF – (M)	—	—	↕	↕	1	DIR INH INH IX1 IX	33 43 53 63 73	dd ff 	5 3 3 6 5
CPX #*opr* CPX *opr* CPX *opr* CPX *opr*,X CPX *opr*,X CPX ,X	Compare Index Register with Memory Byte	(X) – (M)	—	—	↕	↕	↕	IMM DIR EXT IX2 IX1 IX	A3 B3 C3 D3 E3 F3	ii dd hh ll ee ff ff 	2 3 4 5 4 3
DEC *opr* DECA DECX DEC *opr*,X DEC ,X	Decrement Byte	M ← (M) – 1 A ← (A) – 1 X ← (X) – 1 M ← (M) – 1 M ← (M) – 1	—	—	↕	↕	—	DIR INH INH IX1 IX	3A 4A 5A 6A 7A	dd ff 	5 3 3 6 5
EOR #*opr* EOR *opr* EOR *opr* EOR *opr*,X EOR *opr*,X EOR ,X	EXCLUSIVE OR Accumulator with Memory Byte	A ← (A) ⊕ (M)	—	—	↕	↕	—	IMM DIR EXT IX2 IX1 IX	A8 B8 C8 D8 E8 F8	ii dd hh ll ee ff ff 	2 3 4 5 4 3
INC *opr* INCA INCX INC *opr*,X INC ,X	Increment Byte	M ← (M) + 1 A ← (A) + 1 X ← (X) + 1 M ← (M) + 1 M ← (M) + 1	—	—	↕	↕	—	DIR INH INH IX1 IX	3C 4C 5C 6C 7C	dd ff 	5 3 3 6 5
JMP *opr* JMP *opr* JMP *opr*,X JMP *opr*,X JMP ,X	Unconditional Jump	PC ← Jump Address	—	—	—	—	—	DIR EXT IX2 IX1 IX	BC CC DC EC FC	dd hh ll ee ff ff 	2 3 4 3 2

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Table 13-6. Instruction Set Summary (Continued)

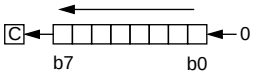
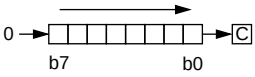
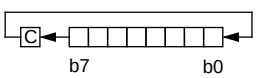
Source Form	Operation	Description	Effect on CCR					Address Mode	Opcode	Operand	Cycles
			H	I	N	Z	C				
JSR *opr* JSR *opr* JSR *opr*,X JSR *opr*,X JSR ,X	Jump to Subroutine	PC ← (PC) + n (n = 1, 2, or 3) Push (PCL); SP ← (SP) – 1 Push (PCH); SP ← (SP) – 1 PC ← Effective Address	—	—	—	—	—	DIR EXT IX2 IX1 IX	BD CD DD ED FD	dd hh ll ee ff ff	5 6 7 6 5
LDA #*opr* LDA *opr* LDA *opr* LDA *opr*,X LDA *opr*,X LDA ,X	Load Accumulator with Memory Byte	A ← (M)	—	—	↕×	↕	—	IMM DIR EXT IX2 IX1 IX	A6 B6 C6 D6 E6 F6	ii dd hh ll ee ff ff	2 3 4 5 4 3
LDX #*opr* LDX *opr* LDX *opr* LDX *opr*,X LDX *opr*,X LDX ,X	Load Index Register with Memory Byte	X ← (M)	—	—	↕×	↕×	—	IMM DIR EXT IX2 IX1 IX	AE BE CE DE EE FE	ii dd hh ll ee ff ff	2 3 4 5 4 3
LSL *opr* LSLA LSLX LSL *opr*,X LSL ,X	Logical Shift Left (Same as ASL)		—	—	↕×	↕	↕	DIR INH INH IX1 IX	38 48 58 68 78	dd ff 	5 3 3 6 5
LSR *opr* LSRA LSRX LSR *opr*,X LSR ,X	Logical Shift Right		—	—	0	↕	↕	DIR INH INH IX1 IX	34 44 54 64 74	dd ff 	5 3 3 6 5
MUL	Unsigned Multiply	X : A ← (X) × (A)	0	—	—	—	0	INH	42		11
NEG *opr* NEGA NEGX NEG *opr*,X NEG ,X	Negate Byte (Two's Complement)	M ← –(M) = $00 – (M) A ← –(A) = $00 – (A) X ← –(X) = $00 – (X) M ← –(M) = $00 – (M) M ← –(M) = $00 – (M)	—	—	↕×	↕	↕	DIR INH INH IX1 IX	30 40 50 60 70	dd ff 	5 3 3 6 5
NOP	No Operation		—	—	—	—	—	INH	9D		2
ORA #*opr* ORA *opr* ORA *opr* ORA *opr*,X ORA *opr*,X ORA ,X	Logical OR Accumulator with Memory	A ← (A) ∨ (M)	—	—	↕×	↕	—	IMM DIR EXT IX2 IX1 IX	AA BA CA DA EA FA	ii dd hh ll ee ff ff	2 3 4 5 4 3
ROL *opr* ROLA ROLX ROL *opr*,X ROL ,X	Rotate Byte Left through Carry Bit		—	—	↕×	↕	↕	DIR INH INH IX1 IX	39 49 59 69 79	dd ff 	5 3 3 6 5

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Table 13-6. Instruction Set Summary (Continued)

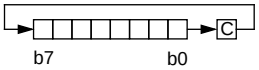
Source Form	Operation	Description	Effect on CCR					Address Mode	Opcode	Operand	Cycles
			H	I	N	Z	C				
ROR *opr* RORA RORX ROR *opr*,X ROR ,X	Rotate Byte Right through Carry Bit		— — — — —	— — — — —	↕ ↕ ↕ ↕ ↕	× ↕ ↕ ↕ ↕	↕ ↕ ↕ ↕ ↕	DIR INH INH IX1 IX	36 46 56 66 76	dd ff 	5 3 3 6 5
RSP	Reset Stack Pointer	SP ← $00FF	—	—	—	—	—	INH	9C		2
RTI	Return from Interrupt	SP ← (SP) + 1; Pull (CCR) SP ← (SP) + 1; Pull (A) SP ← (SP) + 1; Pull (X) SP ← (SP) + 1; Pull (PCH) SP ← (SP) + 1; Pull (PCL)	↕	↕	↕	↕	↕	INH	80		9
RTS	Return from Subroutine	SP ← (SP) + 1; Pull (PCH) SP ← (SP) + 1; Pull (PCL)	—	—	—	—	—	INH	81		6
SBC #*opr* SBC *opr* SBC *opr* SBC *opr*,X SBC *opr*,X SBC ,X	Subtract Memory Byte and Carry Bit from Accumulator	A ← (A) – (M) – (C)	—	—	↕	↕	↕	IMM DIR EXT IX2 IX1 IX	A2 B2 C2 D2 E2 F2	ii dd hh ll ee ff ff 	2 3 4 5 4 3
SEC	Set Carry Bit	C ← 1	—	—	—	—	1	INH	99		2
SEI	Set Interrupt Mask	I ← 1	—	1	—	—	—	INH	9B		2
STA *opr* STA *opr* STA *opr*,X STA *opr*,X STA ,X	Store Accumulator in Memory	M ← (A)	—	—	↕	↕	—	DIR EXT IX2 IX1 IX	B7 C7 D7 E7 F7	dd hh ll ee ff ff 	4 5 6 5 4
STOP	Stop Oscillator and Enable IRQ Pin		—	0	—	—	—	INH	8E		2
STX *opr* STX *opr* STX *opr*,X STX *opr*,X STX ,X	Store Index Register In Memory	M ← (X)	—	—	↕	↕	—	DIR EXT IX2 IX1 IX	BF CF DF EF FF	dd hh ll ee ff ff 	4 5 6 5 4
SUB #*opr* SUB *opr* SUB *opr* SUB *opr*,X SUB *opr*,X SUB ,X	Subtract Memory Byte from Accumulator	A ← (A) – (M)	—	—	↕	↕	↕	IMM DIR EXT IX2 IX1 IX	A0 B0 C0 D0 E0 F0	ii dd hh ll ee ff ff 	2 3 4 5 4 3
SWI	Software Interrupt	PC ← (PC) + 1; Push (PCL) SP ← (SP) – 1; Push (PCH) SP ← (SP) – 1; Push (X) SP ← (SP) – 1; Push (A) SP ← (SP) – 1; Push (CCR) SP ← (SP) – 1; I ← 1 PCH ← Interrupt Vector High Byte PCL ← Interrupt Vector Low Byte	—	1	—	—	—	INH	83		10
TAX	Transfer Accumulator to Index Register	X ← (A)	—	—	—	—	—	INH	97		2

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Table 13-6. Instruction Set Summary (Continued)

Source Form	Operation	Description	Effect on CCR					Address Mode	Opcode	Operand	Cycles
			H	I	N	Z	C				
TST *opr* TSTA TSTX TST *opr*,X TST ,X	Test Memory Byte for Negative or Zero	(M) – $00	—	—	↕	↕	—	DIR INH INH IX1 IX	3D 4D 5D 6D 7D	dd ff 	4 3 3 5 4
TXA	Transfer Index Register to Accumulator	A ← (X)	—	—	—	—	—	INH	9F		2
WAIT	Stop CPU Clock and Enable Interrupts		—	0×	—	—	—	INH	8F		2

A	Accumulator	*opr*	Operand (one or two bytes)
C	Carry/borrow flag	PC	Program counter
CCR	Condition code register	PCH	Program counter high byte
dd	Direct address of operand	PCL	Program counter low byte
dd rr	Direct address of operand and relative offset of branch instruction	REL	Relative addressing mode
DIR	Direct addressing mode	*rel*	Relative program counter offset byte
ee ff	High and low bytes of offset in indexed, 16-bit offset addressing	rr	Relative program counter offset byte
EXT	Extended addressing mode	SP	Stack pointer
ff	Offset byte in indexed, 8-bit offset addressing	X	Index register
H	Half-carry flag	Z	Zero flag
hh ll	High and low bytes of operand address in extended addressing	#	Immediate value
I	Interrupt mask	∧	Logical AND
ii	Immediate operand byte	∨	Logical OR
IMM	Immediate addressing mode	⊕	Logical EXCLUSIVE OR
INH	Inherent addressing mode	( )	Contents of
IX	Indexed, no offset addressing mode	–( )	Negation (two's complement)
IX1	Indexed, 8-bit offset addressing mode	←	Loaded with
IX2	Indexed, 16-bit offset addressing mode	?	If
M	Memory location	:	Concatenated with
N	Negative flag	↕	Set or cleared
n	Any bit	—	Not affected

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Table 13-7. Opcode Map

	Bit Manipulation		Branch	Read-Modify-Write					Control		Register/Memory						
	DIR	DIR	REL	DIR	INH	INH	IX1	IX	INH	INH	IMM	DIR	EXT	IX2	IX1	IX	
MSB / LSB	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	MSB / LSB
0	5 BRSET0 3 DIR	5 BSET0 2 DIR	3 BRA 2 REL	5 NEG 2 DIR	3 NEGA 1 INH	3 NEGX 1 INH	6 NEG 2 IX1	5 NEG 1 IX	9 RTI 1 INH		2 SUB 2 IMM	3 SUB 2 DIR	4 SUB 3 EXT	5 SUB 3 IX2	4 SUB 2 IX1	3 SUB 1 IX	0
1	5 BRCLR0 3 DIR	5 BCLR0 2 DIR	3 BRN 2 REL						6 RTS 1 INH		2 CMP 2 IMM	3 CMP 2 DIR	4 CMP 3 EXT	5 CMP 3 IX2	4 CMP 2 IX1	3 CMP 1 IX	1
2	5 BRSET1 3 DIR	5 BSET1 2 DIR	3 BHI 2 REL		11 MUL 1 INH						2 SBC 2 IMM	3 SBC 2 DIR	4 SBC 3 EXT	5 SBC 3 IX2	4 SBC 2 IX1	3 SBC 1 IX	2
3	5 BRCLR1 3 DIR	5 BCLR1 2 DIR	3 BLS 2 REL	5 COM 2 DIR	3 COMA 1 INH	3 COMX 1 INH	6 COM 2 IX1	5 COM 1 IX	10 SWI 1 INH		2 CPX 2 IMM	3 CPX 2 DIR	4 CPX 3 EXT	5 CPX 3 IX2	4 CPX 2 IX1	3 CPX 1 IX	3
4	5 BRSET2 3 DIR	5 BSET2 2 DIR	3 BCC 2 REL	5 LSR 2 DIR	3 LSRA 1 INH	3 LSRX 1 INH	6 LSR 2 IX1	5 LSR 1 IX			2 AND 2 IMM	3 AND 2 DIR	4 AND 3 EXT	5 AND 3 IX2	4 AND 2 IX1	3 AND 1 IX	4
5	5 BRCLR2 3 DIR	5 BCLR2 2 DIR	3 BCS/BLO 2 REL								2 BIT 2 IMM	3 BIT 2 DIR	4 BIT 3 EXT	5 BIT 3 IX2	4 BIT 2 IX1	3 BIT 1 IX	5
6	5 BRSET3 3 DIR	5 BSET3 2 DIR	3 BNE 2 REL	5 ROR 2 DIR	3 RORA 1 INH	3 RORX 1 INH	6 ROR 2 IX1	5 ROR 1 IX			2 LDA 2 IMM	3 LDA 2 DIR	4 LDA 3 EXT	5 LDA 3 IX2	4 LDA 2 IX1	3 LDA 1 IX	6
7	5 BRCLR3 3 DIR	5 BCLR3 2 DIR	3 BEQ 2 REL	5 ASR 2 DIR	3 ASRA 1 INH	3 ASRX 1 INH	6 ASR 2 IX1	5 ASR 1 IX		2 TAX 1 INH		4 STA 2 DIR	5 STA 3 EXT	6 STA 3 IX2	5 STA 2 IX1	4 STA 1 IX	7
8	5 BRSET4 3 DIR	5 BSET4 2 DIR	3 BHCC 2 REL	5 ASL/LSL 2 DIR	3 ASLA/LSLA 1 INH	3 ASLX/LSLX 1 INH	6 ASL/LSL 2 IX1	5 ASL/LSL 1 IX		2 CLC 1 INH	2 EOR 2 IMM	3 EOR 2 DIR	4 EOR 3 EXT	5 EOR 3 IX2	4 EOR 2 IX1	3 EOR 1 IX	8
9	5 BRCLR4 3 DIR	5 BCLR4 2 DIR	3 BHCS 2 REL	5 ROL 2 DIR	3 ROLA 1 INH	3 ROLX 1 INH	6 ROL 2 IX1	5 ROL 1 IX		2 SEC 1 INH	2 ADC 2 IMM	3 ADC 2 DIR	4 ADC 3 EXT	5 ADC 3 IX2	4 ADC 2 IX1	3 ADC 1 IX	9
A	5 BRSET5 3 DIR	5 BSET5 2 DIR	3 BPL 2 REL	5 DEC 2 DIR	3 DECA 1 INH	3 DECX 1 INH	6 DEC 2 IX1	5 DEC 1 IX		2 CLI 1 INH	2 ORA 2 IMM	3 ORA 2 DIR	4 ORA 3 EXT	5 ORA 3 IX2	4 ORA 2 IX1	3 ORA 1 IX	A
B	5 BRCLR5 3 DIR	5 BCLR5 2 DIR	3 BMI 2 REL							2 SEI 1 INH	2 ADD 2 IMM	3 ADD 2 DIR	4 ADD 3 EXT	5 ADD 3 IX2	4 ADD 2 IX1	3 ADD 1 IX	B
C	5 BRSET6 3 DIR	5 BSET6 2 DIR	3 BMC 2 REL	5 INC 2 DIR	3 INCA 1 INH	3 INCX 1 INH	6 INC 2 IX1	5 INC 1 IX		2 RSP 1 INH		2 JMP 2 DIR	3 JMP 3 EXT	4 JMP 3 IX2	3 JMP 2 IX1	2 JMP 1 IX	C
D	5 BRCLR6 3 DIR	5 BCLR6 2 DIR	3 BMS 2 REL	4 TST 2 DIR	3 TSTA 1 INH	3 TSTX 1 INH	5 TST 2 IX1	4 TST 1 IX		2 NOP 1 INH	6 BSR 2 REL	5 JSR 2 DIR	6 JSR 3 EXT	7 JSR 3 IX2	6 JSR 2 IX1	5 JSR 1 IX	D
E	5 BRSET7 3 DIR	5 BSET7 2 DIR	3 BIL 2 REL						2 STOP 1 INH		2 LDX 2 IMM	3 LDX 2 DIR	4 LDX 3 EXT	5 LDX 3 IX2	4 LDX 2 IX1	3 LDX 1 IX	E
F	5 BRCLR7 3 DIR	5 BCLR7 2 DIR	3 BIH 2 REL	5 CLR 2 DIR	3 CLRA 1 INH	3 CLRX 1 INH	6 CLR 2 IX1	5 CLR 1 IX	2 WAIT 1 INH	2 TXA 1 INH		4 STX 2 DIR	5 STX 3 EXT	6 STX 3 IX2	5 STX 2 IX1	4 STX 1 IX	F

INH = Inherent
IMM = Immediate
DIR = Direct
EXT = Extended
REL = Relative
IX = Indexed, No Offset
IX1 = Indexed, 8-Bit Offset
IX2 = Indexed, 16-Bit Offset

LSB of Opcode in Hexadecimal

MSB / LSB	0
0	5 BRSET0 3 DIR

MSB of Opcode in Hexadecimal
Number of Cycles
Opcode Mnemonic
Number of Bytes/Addressing Mode

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Section 14. Electrical Specifications

14.1 Contents

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14.2 Introdution

This section contains electrical and timing specifications.

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14.3 Absolute Maximum Ratings

Maximum ratings are the extreme limits to which the MCU can be exposed without permanently damaging it.

NOTE: *This device is not guaranteed to operate properly at the maximum ratings. Refer to* ***14.6 DC Electrical Characteristics*** *for guaranteed operating conditions.*

Table 14-1. Absolute Maximum Ratings(1)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{DD}	–0.3 to +7.0	V
Input Voltage	V_{IN}	V_{SS} –0.3 to V_{DD} +0.3	V
Self-Check Mode ($\overline{IRQ}$ Pin Only)	V_{IN}	V_{SS} –0.3 to 2 x V_{DD} +0.3	V
Current Drain Per Pin Excluding V_{DD} and V_{SS}	I	25	mA
Storage Temperature Range	T_{STG}	–65 to +150	°C

NOTE:
1. Voltages referenced to V_{SS}..

NOTE: *This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum-rated voltages to this high-impedance circuit. For proper operation, it is recommended that V_{IN} and V_{OUT} be constrained to the range $V_{SS} \le (V_{IN}$ or $V_{OUT}) \le V_{DD}$. Reliability of operation is enhanced if unused inputs are connected to an appropriate logic voltage level (for example, either V_{SS} or V_{DD}.)*

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14.4 Functional Operating Range

Table 14-2. Operating Range

Characteristic	Symbol	Value	Unit
Operating Temperature Range MC68HC705MC4P, DW, S (Standard) MC68HC705MC4CP, CDW, CS (Extended) MC68HC705MC4VP, VDW, VS (Automotive) MC68HC705MC4MP, MDW, MS(Automotive)	T_A	T_L to T_H 0 to 70 –40 to 85 –40 to 105 –40 to 125	°C
Operating Voltage Range	V_{DD}	5.0 ± 10%	V

14.5 Thermal Characteristics

Table 14-3. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance Plastic (28 Pin) SOIC (28 Pin)	θ_{JA}	 60 60	°C/W
I/O Pin Power Dissipation	$P_{I/O}$	User Determined	W
Power Dissipation(1)	P_D	$P_D = (I_{DD} \times V_{DD}) + P_{I/O} = K/(T_J + 273\ °C)$	W
Constant(2)	K	$P_D \times (T_A + 273\ °C) + P_D^2 \times \theta_{JA}$	W/°C
Average Junction Temperature	T_J	$T_A + (P_D \times \theta_{JA})$	°C
Maximum Junction Temperature	T_{JM}	125	°C

NOTES:
1. Power dissipation is a function of temperature.
2. K is a constant unique to the device. K can be determined for a known T_A and measured P_D. With this value of K, P_D and T_J can be determined for any value of T_A.

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14.6 DC Electrical Characteristics

Table 14-4. DC Electrical Characteristics (V_{DD} = 5.0 Vdc ± 10%)(1)

Characteristic	Symbol	Min	Typ(2)	Max	Unit
Output High Voltage (I_{Load}= 10.0 µA)	V_{OH}	V_{DD} –0.1	—	—	V
Output Low Voltage (I_{Load} = 10.0 µA)	V_{OL}	—	—	0.1	V
Output High Voltage (I_{Load} = –0.8 mA) PB4–PB7, PC0–PC7, PD6/TCMP (I_{Load} = –10.0 mA) PA0–PA7 (Max Total I_{Load} = 20 mA)	V_{OH}	V_{DD} –0.8 V_{DD} –2.0	— —	— —	V
Output Low Voltage (I_{Load} = 1.6 mA) PA0–PA7, PB4– PB6, PC0–PC7, PD6/TCMP, $\overline{RESET}$ (I_{Load} = 10.0 mA) PB7	V_{OL}	— —	— —	0.4 1.0	V
Input High Voltage PA0–PA7, PB4–PB7, PC0–PC7, PD6, TCAP/PD7, $\overline{IRQ}$, $\overline{RESET}$, OSC1	V_{IH}	0.7 x V_{DD}	—	V_{DD}	V
Input Low Voltage PA0–PA7, PB4–PB7, PC0–PC7, PD6, TCAP/PD7, $\overline{IRQ}$, $\overline{RESET}$, OSC1	V_{IL}	V_{SS}	—	0.2 x V_{DD}	V
V_{DD} Supply Current (see Notes) Run Wait with A/D On Wait with A/D Off Quiescent 25 °C 0 to 70 °C (Standard) –40 to 85 °C (Extended) –40 to 105 °C (Automotive) –40 to 125 °C (Automotive)	I_{DD}	 — — — — — — — —	 7.0 2.5 1.8 8 8 12 18 25	 8.5 3.3 3.0 50 50 50 50 50	 mA mA mA µA µA µA µA µA
I/O Ports Hi-Z Leakage Current PA0–PA7, PB4–PB7, PC0–PC7, PD6/TCAP/TCMP	I_{IL}	—	—	± 10	µA
A/D Ports Hi-Z Leakage Current PC0–PC5	I_{IL}	—	—	± 1	µA
Input Current, $\overline{RESET}$, $\overline{IRQ}$, OSC1, PD7/TCAP2	I_{IN}	—	—	± 1	µA
Capacitance Ports (as Input or Output) $\overline{RESET}$, $\overline{IRQ}$	 C_{OUT} C_{IN}	 — —	 — —	 12 8	 pF
Input Injection Current, PA7	I_{INJ}	—	—	± 100	µA

NOTES:

1. V_{DD} = 5.0 Vdc ± 10%, V_{SS} = 0 Vdc, T_A = –40 to 125°C, with 6-MHz crystal, unless otherwise noted.
2. All values reflect average measurements at midpoint of voltage range, 25 °C only.
3. Wait I_{DD}: Only timer system active, unless otherwise noted
4. Run (operating) I_{DD}, Wait I_{DD}: measured using external square wave clock source (f_{osc} = 6.0 MHz). All inputs 0.2 V from rail. No dc loads. Less than 50 pF on all outputs. C_L = 20 pF on OSC2.
5. Wait, quiescent I_{DD}: All ports configured as inputs, V_{IL} = 0.2 V, V_{IH} = V_{DD} –0.2 V
6. Wait I_{DD} is affected linearly by the OSC2 capacitance
7. Run I_{DD} measured with PWM, A/D, and SCI systems active

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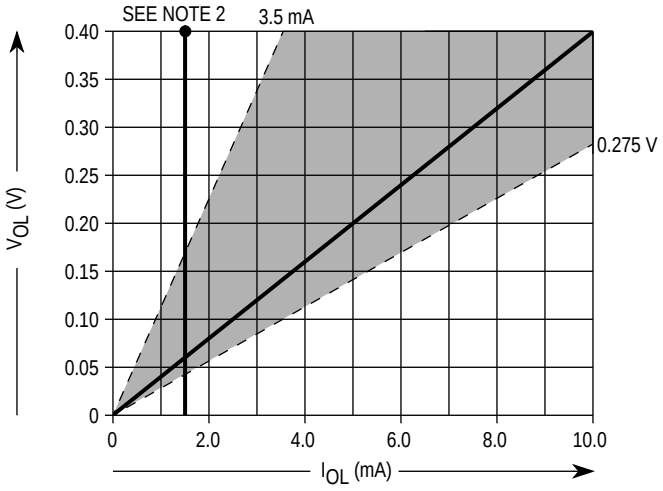
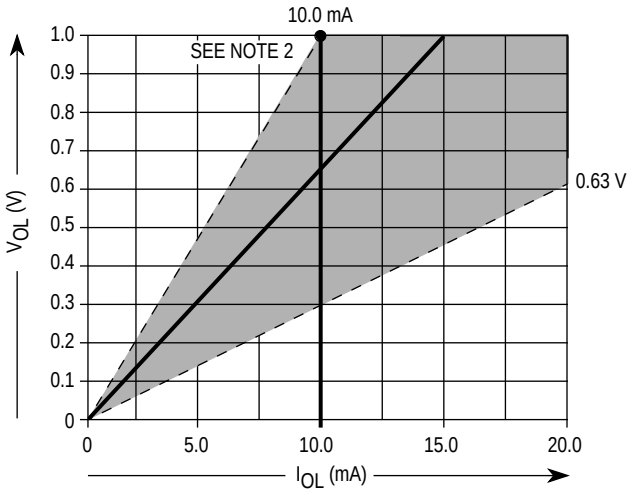


NOTES:
1. Shaded area indicates variation in driver characteristics due to changes in temperature (–40 °C < T < 125 °C) and for normal processing tolerances. Within the limited range of values shown, V vs I curves are approximately straight lines.
2. At V_{DD} = 5.0 V ± 10%, devices are tested for $V_{OL} \leq$ 400 mV @ I_{OL} = 1.6 mA.

Figure 14-1. Typical Low-Side Driver Characteristics for Standard Port Pins: PA0–PA7, PB4–PB6, PC0–PC7, PD6



NOTES:
1. Shaded area indicates variation in driver characteristics due to changes in temperature (–40 °C < T < 125 °C) and for normal processing tolerances. Within the limited range of values shown, V vs I curves are approximately straight lines.
2. At V_{DD} = 5.0 V ± 10%, devices are tested for $V_{OL} \leq$ 1.0 V @ I_{OL} = 10.0 mA.

Figure 14-2. Typical Low-Side Driver Characteristics for High Sink Current Pin, PB7

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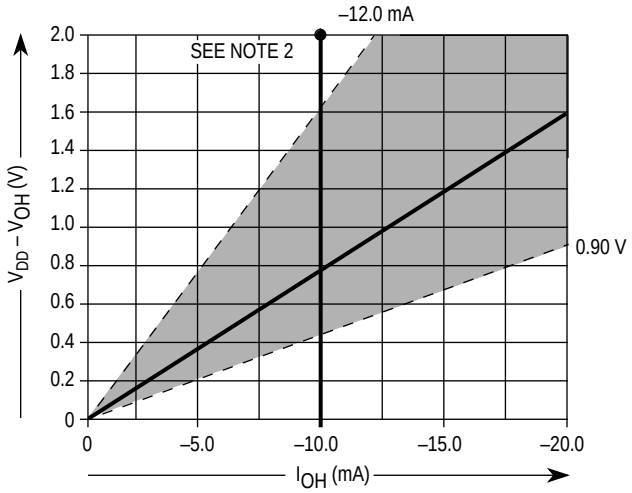
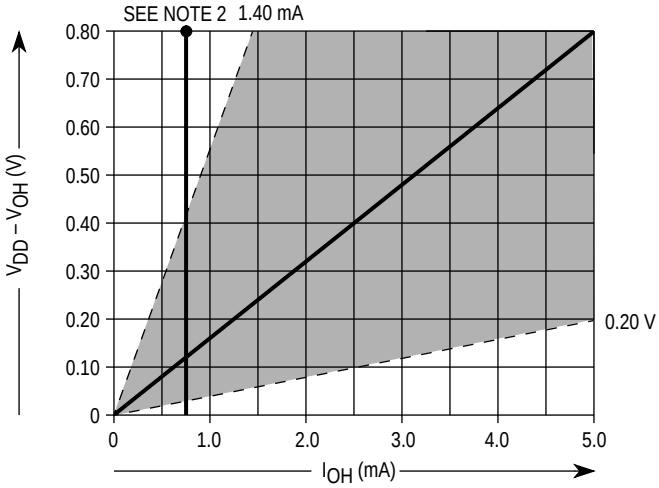


NOTES:
1. Shaded area indicates variation in driver characteristics due to changes in temperature (–40 °C < T < 125 °C) and for normal processing tolerances. Within the limited range of values shown, V vs I curves are approximately straight lines.
2. At V_{DD} = 5.0 V ± 10%, devices are tested for $V_{DD} – V_{OH} \leq 2.0$ V @ I_{OH} = –10.0 mA.

Figure 14-3. Typical High-Side Driver Characteristics for High Source Port Pins, PA0–PA7



NOTES:
1. Shaded area indicates variation in driver characteristics due to changes in temperature (–40 °C < T < 125 °C) and for normal processing tolerances. Within the limited range of values shown, V vs I curves are approximately straight lines.
2. At V_{DD} = 5.0 V ± 10%, devices are tested for $V_{DD} – V_{OH} \leq 0.8$ V @ I_{OH} = 0.80 mA.

Figure 14-4. Typical High-Side Driver Characteristics for Standard Port Pins: PB4–PB7, PC0–PC7, PD6

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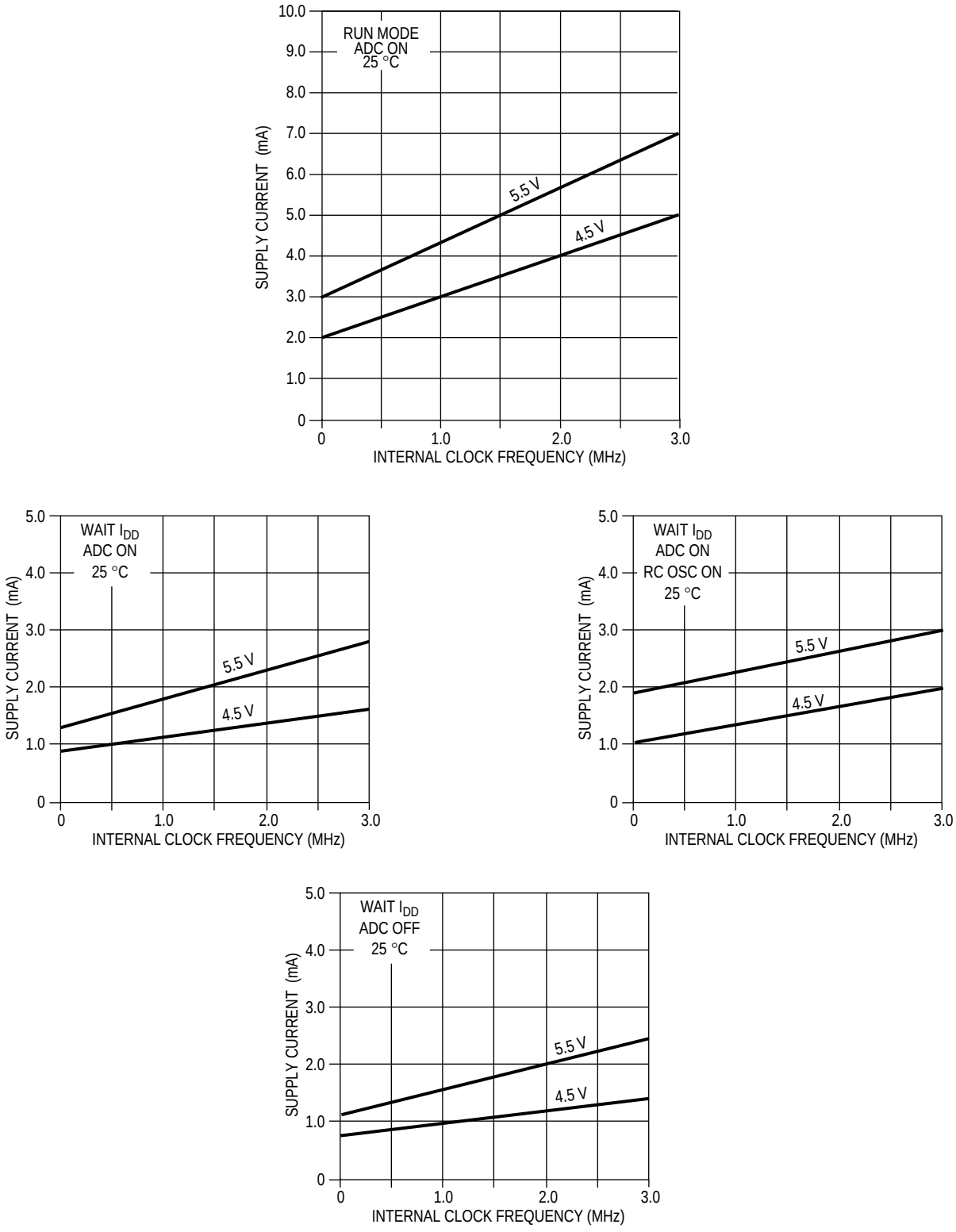

Figure 14-5. Typical Supply Current vs Internal Clock Frequency

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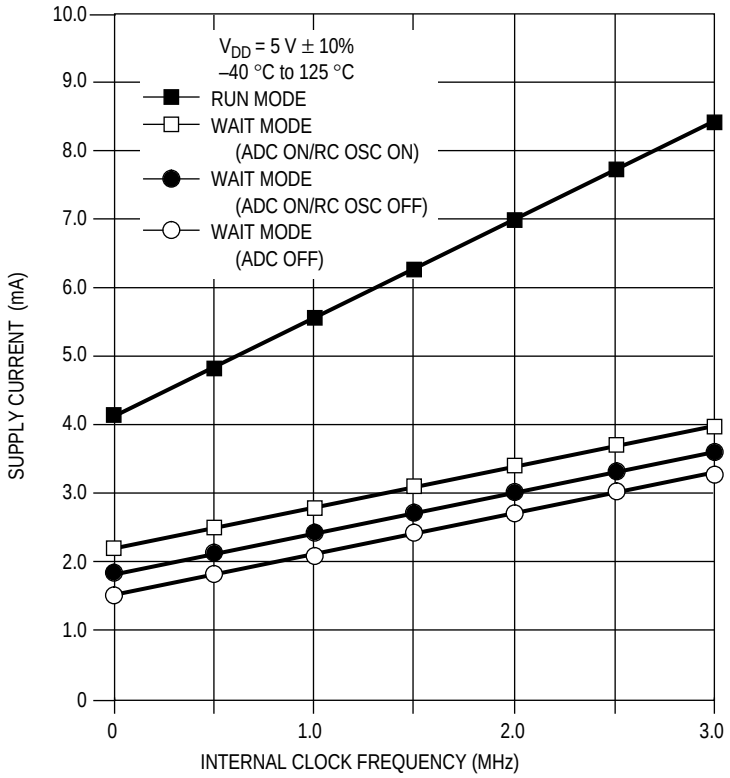

Figure 14-6. Maximum Supply Current vs Internal Clock Frequency

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14.7 A/D Converter Characteristics

Table 14-5. A/D Converter Characteristics(1)

Characteristic	Min	Max	Unit	Notes
Resolution	8	8	Bits	
Absolute Accuracy ($V_{DD} \geq V_{REFH} > 4.0$)	—	± 1 1/2	LSB	Includes Quantization
Conversion Range V_{REFH}	V_{SS} V_{SS}	V_{REFH} V_{DD}	V	A/D accuracy may decrease proportionately as V_{REFH} is reduced below 4.0.
Input Leakage AD0–AD5 V_{REFH}	— —	± 1 ± 1	µA	
Conversion Time (Includes Sampling Time)	32	32	t_{AD} (see Note 2)	
Monotonicity	Inherent (Within Total Error)			
Zero Input Reading	00	01	Hex	$V_{IN} = 0$ V
Full-Scale Reading	FE	FF	Hex	$V_{IN} = V_{REFH}$
Sample Time	12	12	t_{AD} (see Note 2)	
Input Capacitance	—	12	pF	
Analog Input Voltage	V_{SS}	V_{REFH}	V	

NOTES:
1. V_{DD} = 5.0 Vdc ± 10%, V_{SS} = 0 Vdc, T_A = –40 to 125°C, unless otherwise noted.
2. $t_{AD} = t_{cyc}$ if clock source equals MCU.

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14.8 Control Timing

Table 14-6. Control Timing (V_{DD} = 5.0 Vdc ± 10%)(1)

Characteristic	Symbol	Min	Max	Unit
Frequency of Operation Crystal Option External Clock Option	f_{osc}	— dc	6 6	MHz
Internal Operating Frequency Crystal (f_{osc} ÷ 2) External Clock (f_{osc} ÷ 2)	f_{op}	— dc	3 3	MHz
Cycle Time	t_{cyc}	333	—	ns
Crystal Oscillator Startup Time	t_{OXOV}	—	100	ms
Stop Recovery Startup Time (Crystal Oscillator)	t_{ILCH}	—	100	ms
$\overline{\text{RESET}}$ Pulse Width	t_{RL}	1.5	—	t_{cyc}
Interrupt Pulse Width Low (Edge-Triggered)	t_{ILIH}	350	—	ns
Interrupt Pulse Period	t_{ILIL}	see Note 2	—	t_{cyc}
OSC1 Pulse Width	t_{OH}, t_{OL}	200	—	ns
A/D On Current Stabilization Time	t_{ADON}	—	100	µs
RC Oscillator Stabilization Time (A/D)	t_{RCON}	—	5.0	µs
Internal $\overline{\text{RESET}}$ Pulldown Pulse Width	t_{RPD}	—	4	t_{cyc}

NOTES:
1. V_{DD} = 5.0 Vdc ± 10%, V_{SS} = 0 Vdc, T_A = –40 to 125°C, unless otherwise noted.
2. The minimum period, t_{ILIL}, should not be less than the number of cycles it takes to execute the interrupt service routine plus 19 t_{cyc}.

14.9 EPROM Programming Characteristics

Table 14-7. EPROM Programming Characteristics (V_{DD} = 5.0 Vdc ± 10%)(1)

Characteristic	Symbol	Min	Typ	Max	Unit
Programming Voltage $\overline{\text{IRQ}}$/V_{PP}	V_{PP}	15.25	15.5	15.75	V
Programming Current $\overline{\text{IRQ}}$/V_{PP}	I_{PP}	—	4.0	10.0	mA
Programming Time Per Array Byte MOR	 t_{EPGM} t_{MPGM}	 4 4	 — —	 — —	ms

NOTE:
1. V_{DD} = 5.0 Vdc ± 10%, V_{SS} = 0 Vdc, T_A = –40 to 125°C, unless otherwise noted.

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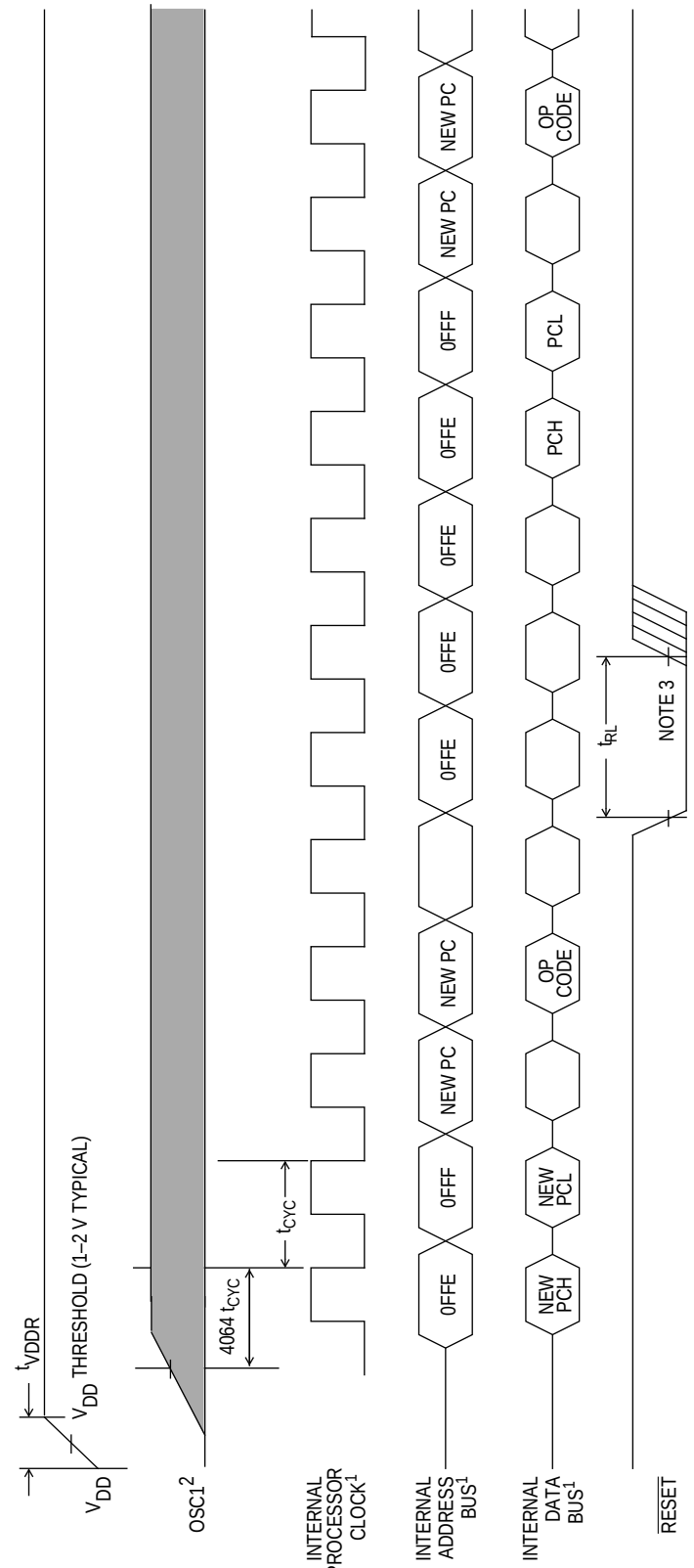

NOTES:
1. Internal timing signal and bus information not available externally.
2. OSC1 line is not meant to represent frequency. It is only used to represent time.
3. The next rising edge of the internal clock following the rising edge of $\overline{\text{RESET}}$ initiates the reset sequence.

Figure 14-7. Power-On Reset and External Reset Timing Diagram

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Section 15. Mechanical Specifications

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15.4 Small Outline Integrated Circuit (Case 751F) 176

15.2 Introduction

The MC68HC705MC4 is available in both a 28-pin plastic dual in-line package (PDIP) and a small outline integrated circuit (SOIC) package.

The following figures show the latest packages at the time of this publication. To make sure that you have the latest package specifications, contact one of the following:

- Local Freescale Sales Office
- Worldwide Web http://www.freescale.com

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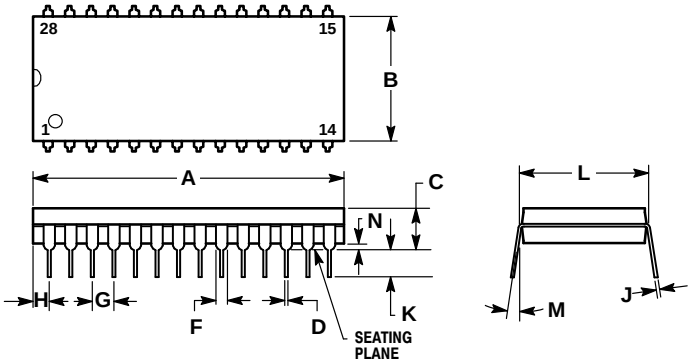
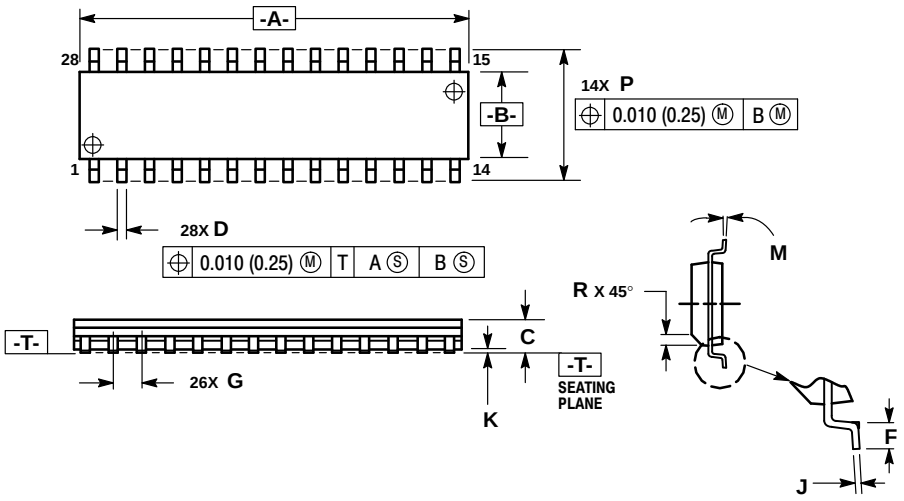
15.3 Plastic Dual In-Line Package (Case 710)



NOTES:
1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25mm (0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	36.45	37.21	1.435	1.465
B	13.72	14.22	0.540	0.560
C	3.94	5.08	0.155	0.200
D	0.36	0.56	0.014	0.022
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.65	2.16	0.065	0.085
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	15.24 BSC		0.600 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

15.4 Small Outline Integrated Circuit (Case 751F)



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	17.80	18.05	0.701	0.711
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.41	0.90	0.016	0.035
G	1.27 BSC		0.050 BSC	
J	0.23	0.32	0.009	0.013
K	0.13	0.29	0.005	0.011
M	0°	8°	0°	8°
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

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Section 16. Ordering Information

16.1 Contents

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16.3 MC Order Numbers 178

16.2 Introduction

This section provides ordering information.

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16.3 MC Order Numbers

The following table shows the MC order numbers for the available package types.

MC Order Number	Operating Temperature Range
MC68HC705MC4P (Standard)	–0 to 70 °C
MC68HC705MC4CP (Extended)	–40 to 85 °C
MC68HC705MC4VP (Automotive)	–40 to 105 °C
MC68HC705MC4MP (Automotive)	–40 to 125 °C
MC68HC705MC4DW (Standard)	–0 to 70 °C
MC68HC705MC4CDW (Extended)	–40 to 85 °C
MC68HC705MC4VDW (Automotive)	–40 to 105 °C
MC68HC705MC4MDW (Automotive)	–40 to 125 °C
MC68HC705MC4S (Standard)	–0 to 70 °C
MC68HC705MC4CS (Extended)	–40 to 85 °C
MC68HC705MC4VS (Automotive)	–40 to 105 °C
MC68HC705MC4MS (Automotive)	–40 to 125 °C

NOTE:
P = Plastic Dual In-Line Package (PDIP)
DW = Small Outline Integrated Circuit (SOIC) Package
S = Ceramic Dual In-Line (Cerdip) Package

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