1 PRODUCT OVERVIEW

OVERVIEW

Samsung's S3C8-series of 8-bit single-chip CMOS microcontrollers offers a fast and efficient CPU, a wide range of integrated peripherals, and various mask-programmable ROM sizes. Important CPU features include:

— Efficient register-oriented architecture

— Selectable CPU clock sources

— Idle and Stop power-down mode release by interrupt

— Built-in basic timer with watchdog function

A sophisticated interrupt structure recognizes up to eight interrupt levels. Each level can have one or more interrupt sources and vectors. Fast interrupt processing (within a minimum six CPU clocks) can be assigned to specific interrupt levels.

S3C80A4/C80A8/C80A5/C80B4/C80B8/C80B5 MICROCONTROLLER

The S3C80A4/C80A8/C80A5/C80B4/C80B8/C80B5 single-chip CMOS microcontroller is fabricated using a highly advanced CMOS process and is based on Samsung's newest CPU architecture.

The S3C80A4/C80A8/C80A5/C80B4/C80B8/C80B5 is the microcontroller which has mask-programmable ROM.

The S3P80A4/P80A8/P80A5/P80B4/P80B8/P80B5 is the microcontroller which has one-time-programmable EPROM.

Using a proven modular design approach, Samsung engineers developed the S3C80A4/C80A8/C80A5/C80B4/C80B8/C80B5 by integrating the following peripheral modules with the powerful SAM87 RC core:

— Three programmable I/O ports, including two 8-bit ports and one 3-bit port, for a total of 19 pins.

— Internal LVD circuit and eight bit-programmable pins for external interrupts.

— One 8-bit basic timer for oscillation stabilization and watchdog functions (system reset).

— One 8-bit timer/counter and one 16-bit timer/counter with selectable operating modes.

— One 8-bit counter with auto-reload function and one-shot or repeat control.

The S3C80A4/C80A8/C80A5/C80B4/C80B8/C80B5 is a versatile general-purpose microcontroller which is especially suitable for use as remote transmitter controller. It is currently available in a 24-pin SOP and SDIP package.

FEATURES

CPU

- SAM87RC CPU core

Memory

- Program memory (ROM)
  - S3C80A4/C80B4: 4-Kbyte (0000H–0FFFH)
  - S3C80A8/C80B8: 8-Kbyte (0000H–1FFFH)
  - S3C80A5/C80B5: 15,872 byte (0000H–3E00H)
- Data memory: 256-byte RAM

Instruction Set

- 78 instructions
- IDLE and STOP instructions added for power-down modes

Instruction Execution Time

- 500 ns at 8-MHz f_{OSC} (minimum)

Interrupts

- 13 interrupt sources with 10 vector.
- 5 level, 10 vector interrupt structure

I/O Ports

- Two 8-bit I/O ports (P0-P1) and one 3-bit port (P2) for a total of 19 bit-programmable pins
- Eight input pins for external interrupts

Carrier Frequency Generator

- One 8-bit counter with auto-reload function and one-shot or repeat control (Counter A)

Back-up mode

- When V_{DD} is lower than V_{LVD}, the chip enters Back-up mode to block oscillation and reduce the current consumption.

Timers and Timer/Counters

- One programmable 8-bit basic timer (BT) for oscillation stabilization control or watchdog timer function
- One 8-bit timer/counter (Timer 0) with two operating modes; Interval mode and PWM mode.
- One 16-bit timer/counter with one operating modes; Interval mode

Low Voltage Detect Circuit

- Low voltage detect for reset or Back-up mode.
- Low level detect voltage
  – S3C80A4/C80A8/C80A5: 2.20 V (Typ) ± 200 mV
  – S3C80B4/C80B8/C80B5: 1.90 V (Typ) ± 200 mV

Auto Reset Function

- Reset occurs when stop mode is released by P0.
- When a falling edge is detected at Port 0 during Stop mode, system reset occurs.

Operating Temperature Range

- –40°C to + 85°C

Operating Voltage Range

- 1.7 V to 3.6 V at 4 MHz f_{OSC}
- 2.0 V to 3.6 V at 8 MHz f_{OSC}

Package Type

- 24-pin SOP/SDIP

BLOCK DIAGRAM

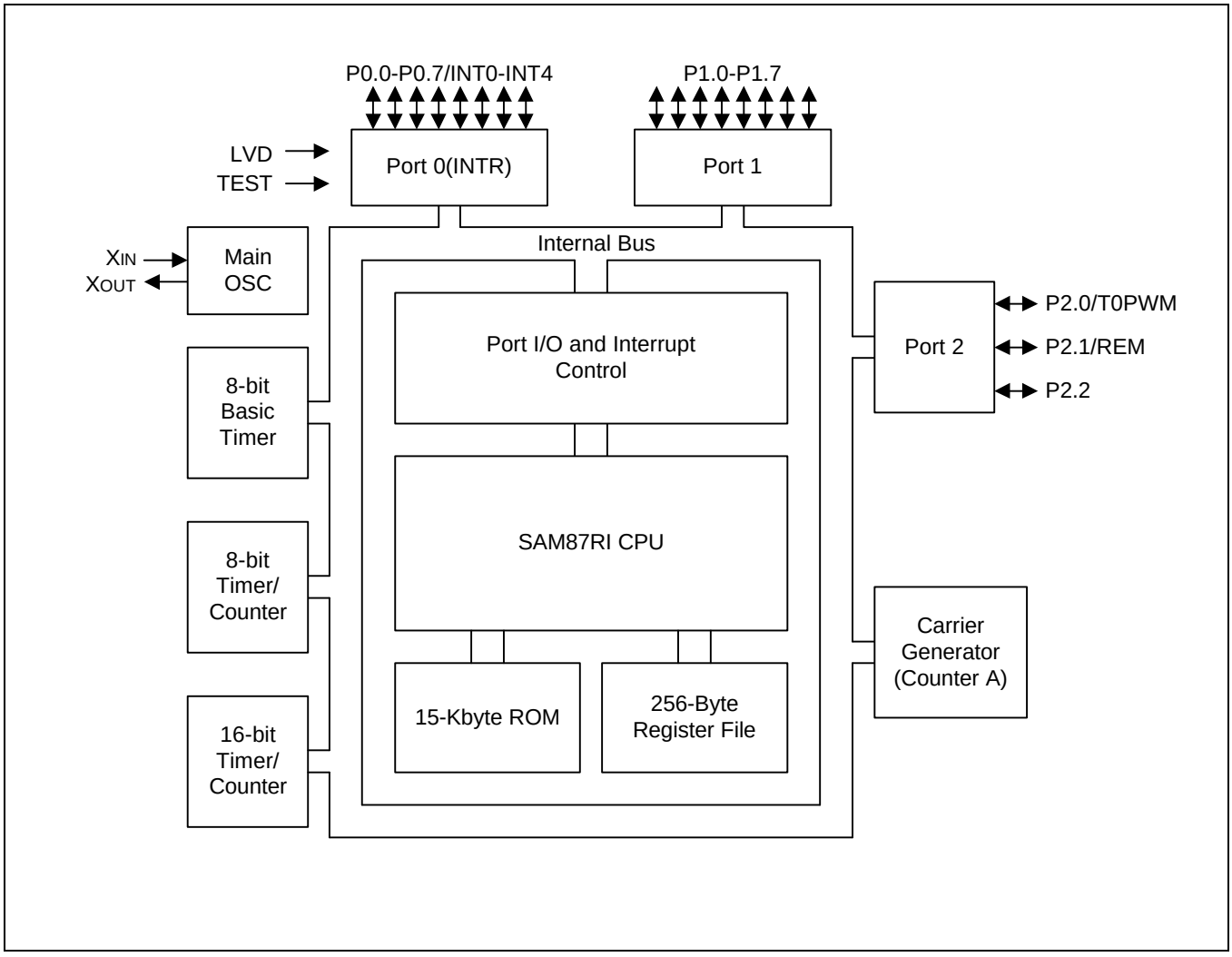


Figure 1-1. Block Diagram

PIN ASSIGNMENTS

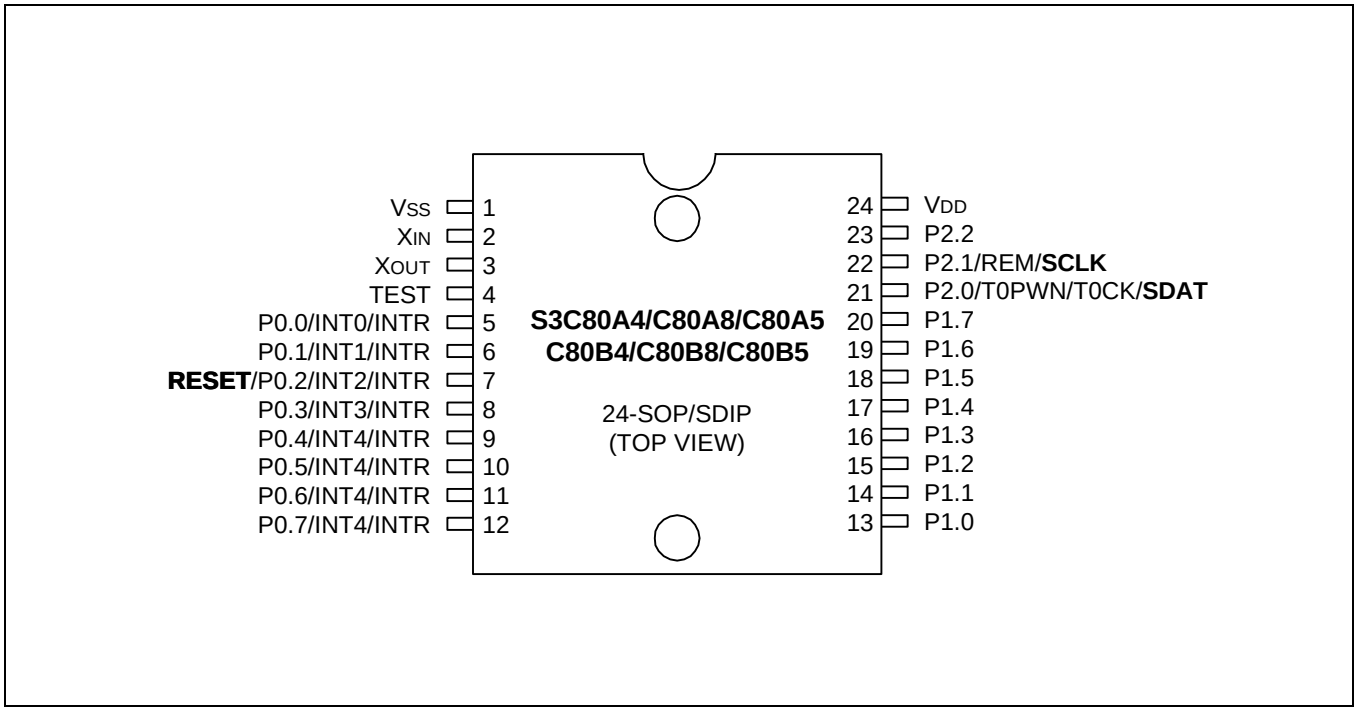


Figure 1-2. Pin Assignment Diagram (24-Pin SOP/SDIP Package)

PIN DESCRIPTIONS

Table 1-1. Pin Descriptions

Pin Names	Pin Type	Pin Description	Circuit Type	24-Pin Number	Shared Functions
P0.0–P0.7	I/O	I/O port with bit-programmable pins. Configurable to input or push-pull output mode. Pull-up resistors are assignable by software. Pins can be assigned individually as external interrupt inputs with noise filters, interrupt enable/ disable, and interrupt pending control. Interrupt with Reset(INTR) is assigned to Port 0.	1	5–12	INT0 – INT4/INTR
P1.0–P1.7	I/O	I/O port with bit-programmable pins. Configurable to input mode or output mode. Pin circuits are either push-pull or n-channel open-drain type. Pull-up resistors are assignable by software.	2	13–20	
P2.0 P2.1 P2.2	I/O	3-bit I/O port with bit-programmable pins. Configurable to input mode, push-pull output mode, or n-channel open-drain output mode. Input mode with pull-up resistors are assignable by software. The two pins of port 2 have high current drive capability.	3 4 5	21–23	REM/T0CK
X_{IN}, X_{OUT}	–	System clock input and output pins	–	2, 3	–
TEST	I	Test signal input pin (for factory use only; must be connected to V_{SS}).	–	4	–
V_{DD}	–	Power supply input pin	–	24	–
V_{SS}	–	Ground pin	–	1	–

PIN CIRCUITS

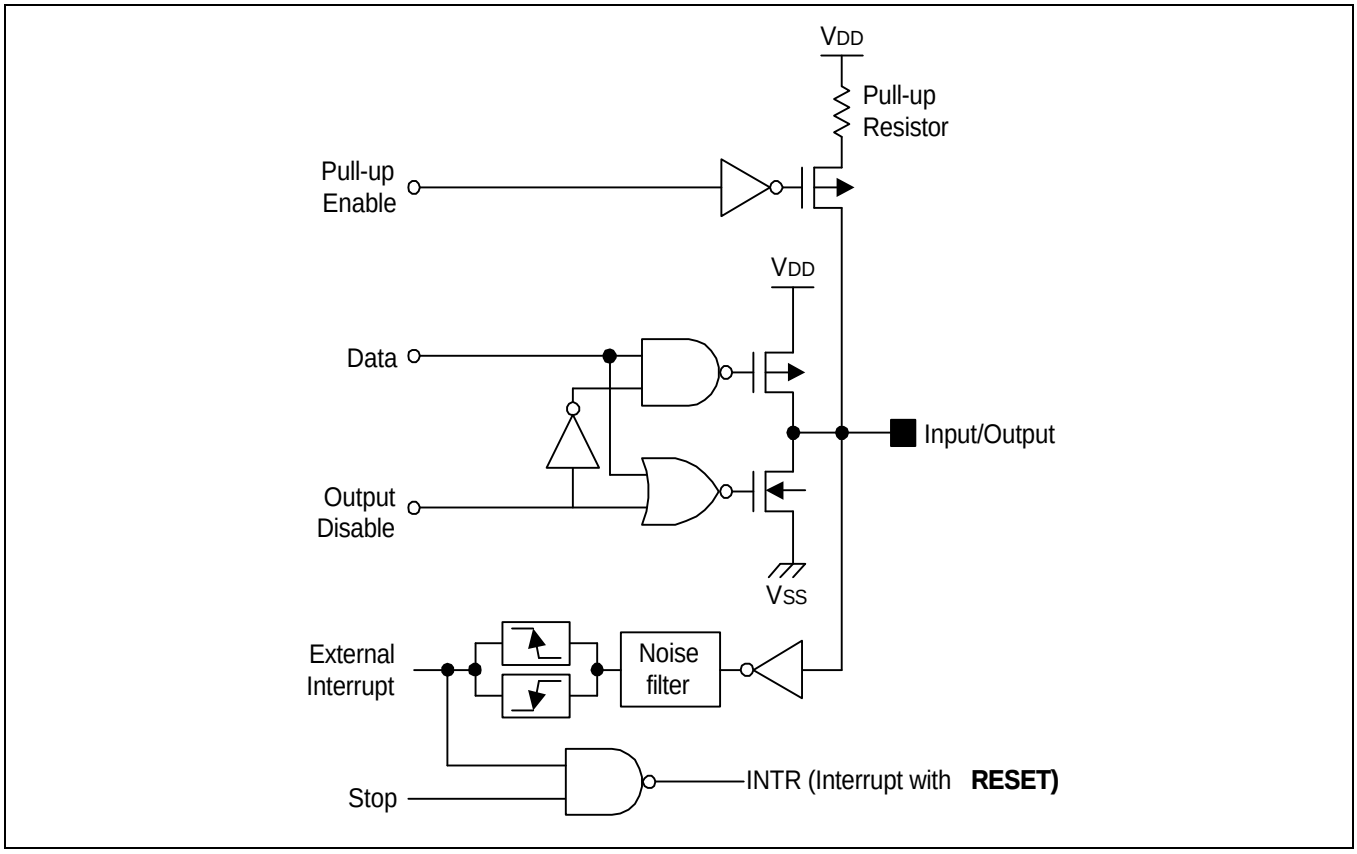


Figure 1-3. Pin Circuit Type 1 (Port 0)

NOTE

Interrupt with reset (INTR) is assigned to port 0 of S3C80A4/C80A8/C80A5/C80B4/C80B8/C80B5. It is designed to release stop status with reset. When the falling/rising edge is detected at any pin of Port 0 during stop status, non vectored interrupt INTR signal occurs, after then system reset occurs automatically. It is designed for a application which are using “stop mode” like remote controller. If stop mode is not used, INTR do not operates and it can be discarded.

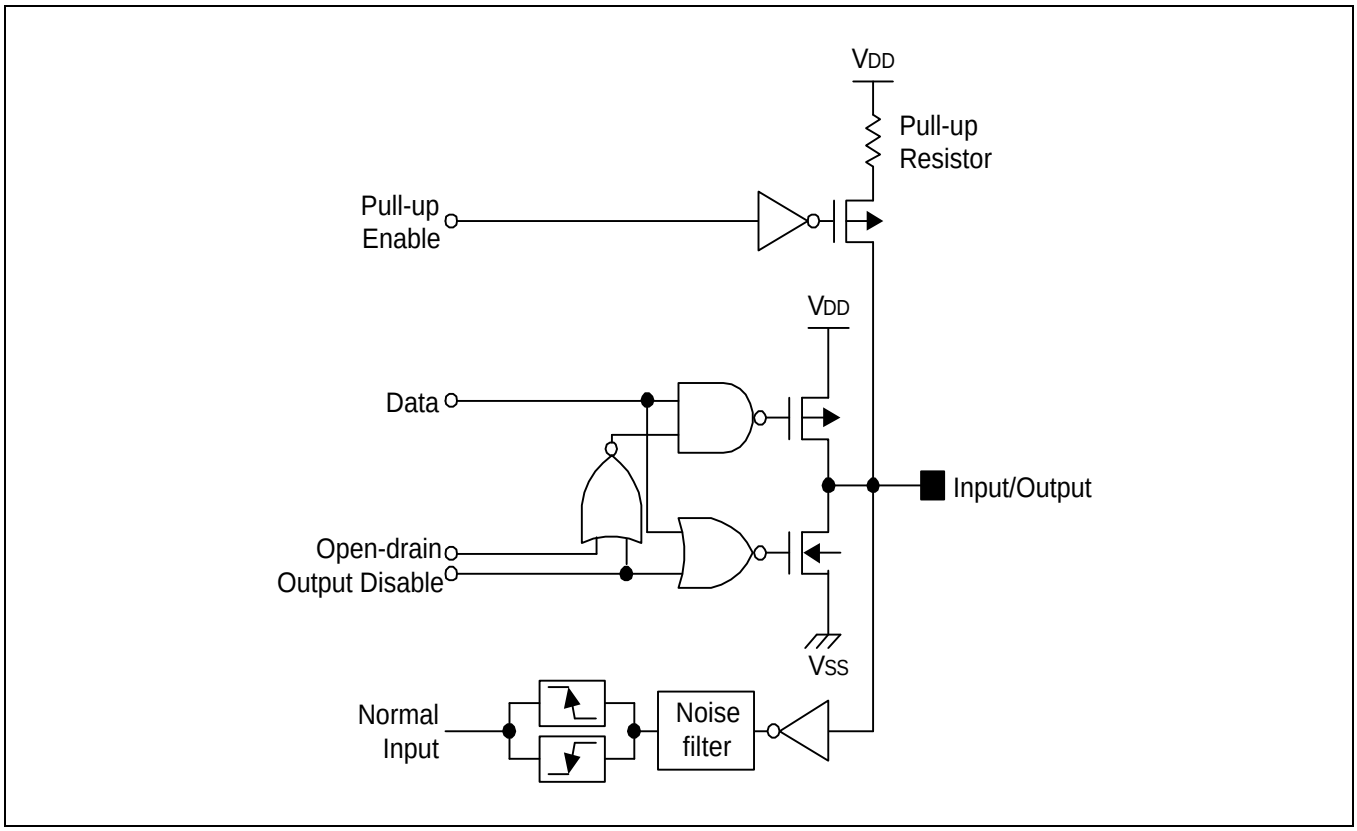


Figure 1-4. Pin Circuit Type 2 (Port 1)

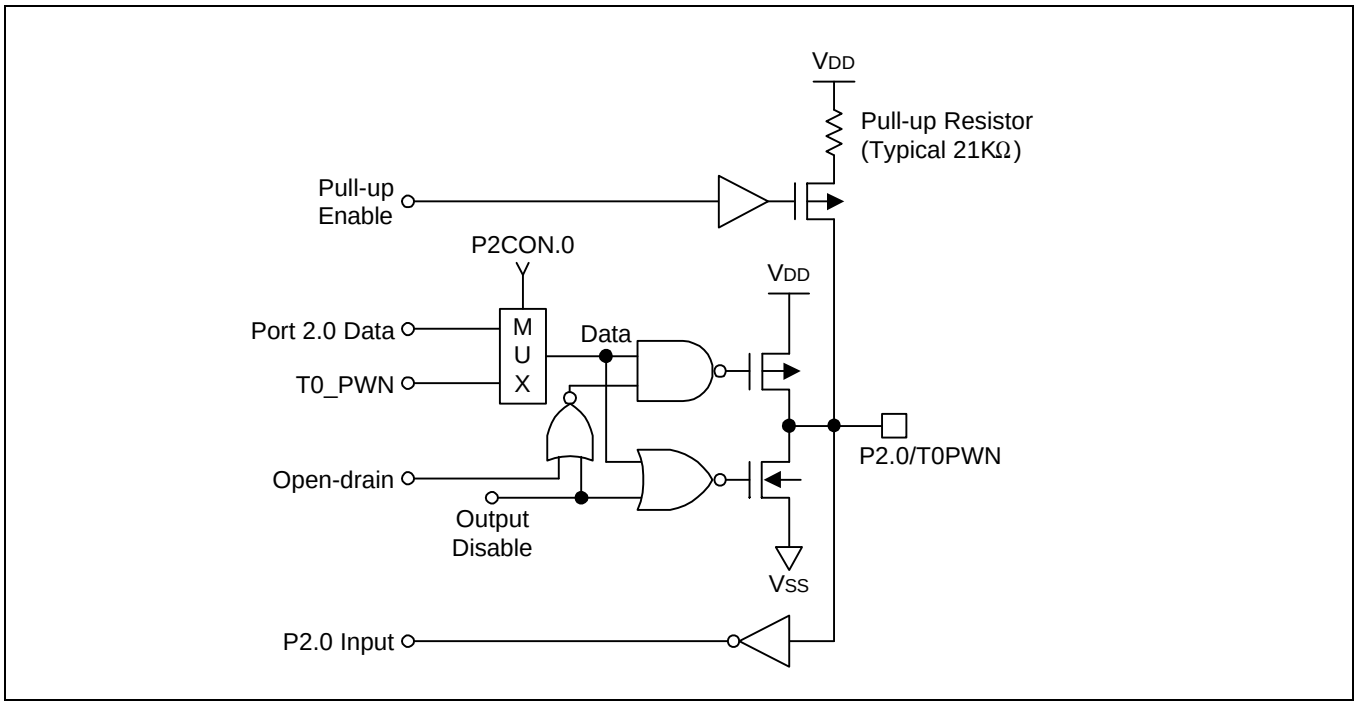


Figure 1-5. Pin Circuit Type 3 (P2.0)

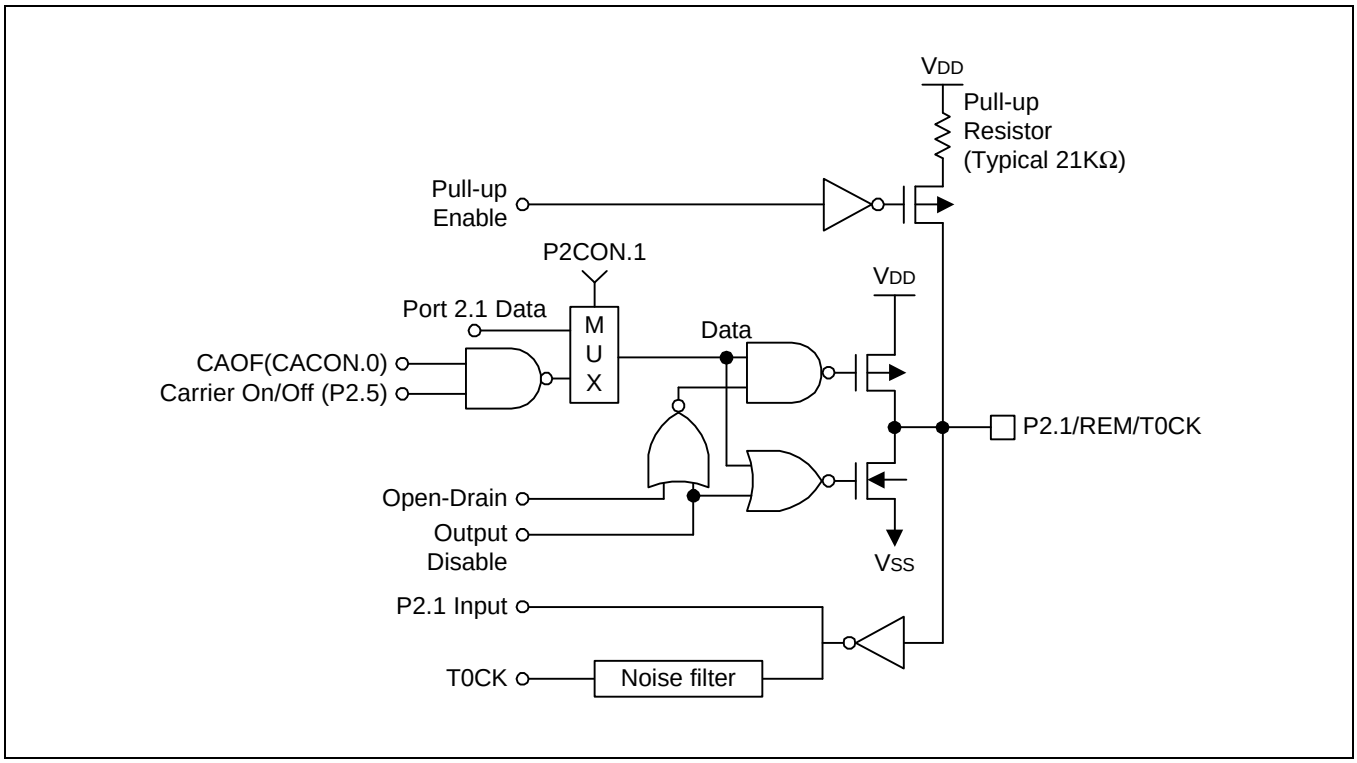


Figure 1-6. Pin Circuit Type 4 (P2.1)

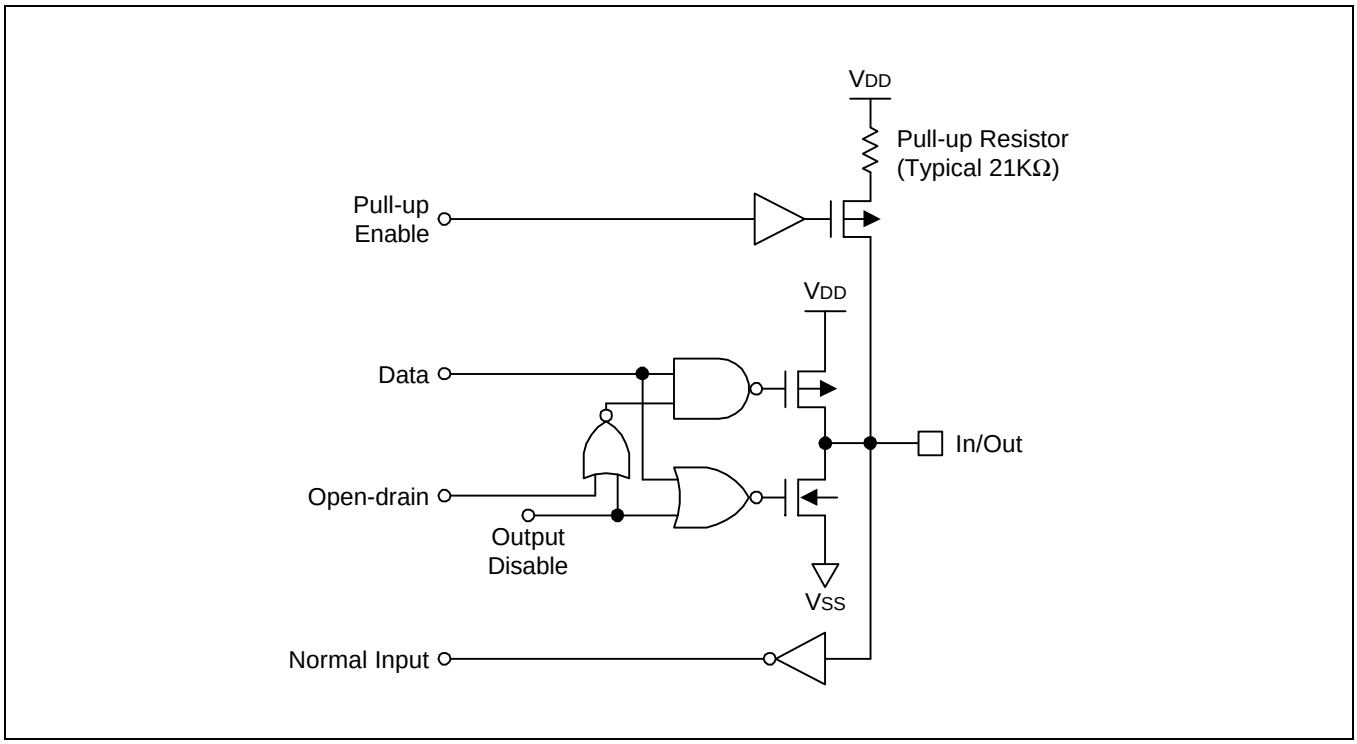


Figure 1-7. Pin Circuit Type 5 (P2.2)

13 ELECTRICAL DATA

OVERVIEW

In this section, S3C80A4/C80A8/C80A5/C80B4/C80B8/C80B5 electrical characteristics are presented in tables and graphs. The information is arranged in the following order:

— Absolute maximum ratings
— D.C. electrical characteristics
— Data retention supply voltage in Stop mode
— Stop mode release timing when initiated by a Reset
— I/O capacitance
— A.C. electrical characteristics
— Input timing for external interrupts (port 0)
— Oscillation characteristics
— Oscillation stabilization time

Table 13-1. Absolute Maximum Ratings

(T_A = 25 °C)

Parameter	Symbol	Conditions	Rating	Unit
Supply voltage	V_{DD}	–	– 0.3 to + 6.5	V
Input voltage	V_{IN}	–	– 0.3 to V_{DD} + 0.3	V
Output voltage	V_O	All output pins	– 0.3 to V_{DD} + 0.3	V
Output current High	I_{OH}	One I/O pin active	– 18	mA
		All I/O pins active	– 60	
Output current Low	I_{OL}	One I/O pin active	+ 30	mA
		Total pin current for ports 0, 1, and 2	+ 100	
		Total pin current for port 3	+ 40	
Operating temperature	T_A	–	– 40 to + 85	°C
Storage temperature	T_{STG}	–	– 65 to + 150	°C

Table 13-2. D.C. Electrical Characteristics

(T_A = – 40 °C to + 85 °C, V_{DD} = 2.0 V to 3.6 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Operating Voltage	V_{DD}	f_{OSC} =8MHz (Instruction clock = 1.33 MHz)	2.0	–	3.6	V
		f_{OSC} = 4MHz (Instruction clock = 0.67 MHz)	1.7	–	3.6	
Input High voltage	V_{IH1}	All input pins except V_{IH2} and V_{IH3}	0.8 V_{DD}	–	V_{DD}	V
	V_{IH2}	X_{IN}	V_{DD} – 0.3		V_{DD}	
Input Low voltage	V_{IL1}	All input pins except V_{IL2} and V_{IL3}	0	–	0.2 V_{DD}	V
	V_{IL2}	X_{IN}			0.3	
Output High voltage	V_{OH1}	V_{DD}= 2.4 V, I_{OH} = – 6 mA Port 2.1 only, T_A = 25°C	V_{DD} – 0.7	–	–	V
	V_{OH2}	V_{DD} = 2.4 V, I_{OH} = – 2.2mA Port 2.0, 2.2, T_A = 25°C	V_{DD} - 0.7			
	V_{OH3}	V_{DD} = 2.4 V, I_{OH} = – 1 mA All output pins except Port2, T_A = 25 °C	V_{DD} - 1.0	–	–	

Table 13-2. D.C. Electrical Characteristics (Continued)

(T_A = – 40 °C to + 85 °C, V_{DD} = 2.0 V to 3.6 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Output Low voltage	V_{OL1}	V_{DD} = 2.4 V, I_{OL} = 12 mA, port 2.1 only, T_A = 25 °C	–	0.4	0.5	
	V_{OL2}	V_{DD} = 2.4 V, I_{OL} = 5 mA Port 2.0,2.2, T_A = 25 °C		0.4	0.5	
	V_{OL3}	I_{OL} = 1 mA Ports 0 and 1, T_A = 25 °C		0.4	1.0	
Input High leakage current	I_{LIH1}	V_{IN} = V_{DD} All input pins except X_{IN} and X_{OUT}	–	–	1	µA
	I_{LIH2}	V_{IN} = V_{DD}, X_{IN} and X_{OUT}			20	
Input Low leakage current	I_{LIL1}	V_{IN} = 0 V All input pins except X_{IN}, X_{OUT}	–	–	– 1	µA
	I_{LIL2}	V_{IN} = 0 V X_{IN} and X_{OUT}			– 20	
Output High leakage current	I_{LOH}	V_{OUT} = V_{DD} All output pins	–	–	1	µA
Output Low leakage current	I_{LOL}	V_{OUT} = 0 V All output pins	–	–	– 1	µA
Pull-up resistors	R_{L1}	V_{DD} = 2.4V, V_{IN} = 0 V; T_A = 25 °C , Ports 0-2	44	55	95	KΩ
Supply current (note)	I_{DD1}	V_{DD} = 3.6 V ± 10% 8-MHz crystal	–	5	9	mA
		4-MHz crystal		2.6	5	
	I_{DD2}	Idle mode; V_{DD} = 3.6 V ± 10 % 8-MHz crystal	–	1.0	2.5	
		4-MHz crystal		0.7	2.0	
	I_{DD3}	Stop mode; V_{DD} = 3.6 V	–	1	6	uA

NOTE: Supply current does not include current drawn through internal pull-up resistors or external output current loads.

Table 13-3. Characteristics of Low Voltage Detect circuit

(T_A = – 40 °C to + 85 °C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Hysteresys Voltage of LVD (Slew Rate of LVD)	ΔV	–	–	30	300	mV
Low level detect voltage (S3C80A4/C80A8/C80A5)	V_{LVD}	–	2.0	2.20	2.40	V
Low level detect voltage (S3C80B4/C80B8/C80B5)	V_{LVD}	–	1.70	1.90	2.1	V

Table 13-4. Data Retention Supply Voltage in Stop Mode

(T_A = – 40 °C to + 85 °C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Data retention supply voltage	V_{DDDR}	–	1.0	–	3.6	V
Data retention supply current	I_{DDDR}	V_{DDDR} = 1.0 V Stop mode	–	–	1	μA

Table 13-5. Input/output Capacitance

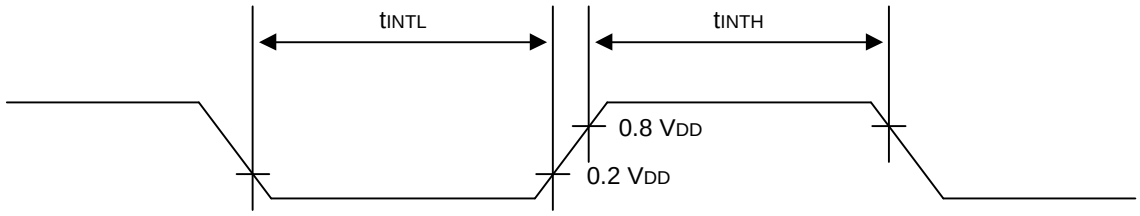
(T_A = – 40°C to + 85 °C, V_{DD} = 0 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input capacitance	C_{IN}	f = 1 MHz; unmeasured pins are connected to V_{SS}	—	—	10	pF
Output capacitance	C_{OUT}					
I/O capacitance	C_{IO}					

Table 13-6. A.C. Electrical Characteristics

(T_A = – 40 °C to + 85 °C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Interrupt input, High, Low width	t_{INTH}, t_{INTL}	P0.0–P0.7, V_{DD} =3.6 V	200	300	—	ns



NOTE: The unit tCPU means one CPU clock period.

Figure 13-1. Input Timing for External Interrupts (Port 0)

Table 13-7. Oscillation Characteristics

(T_A = – 40 °C + 85 °C)

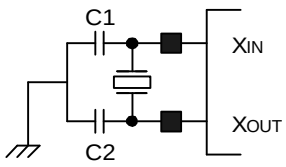
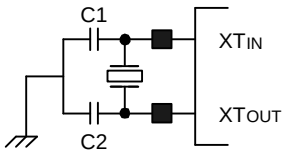
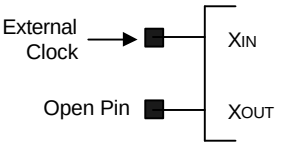
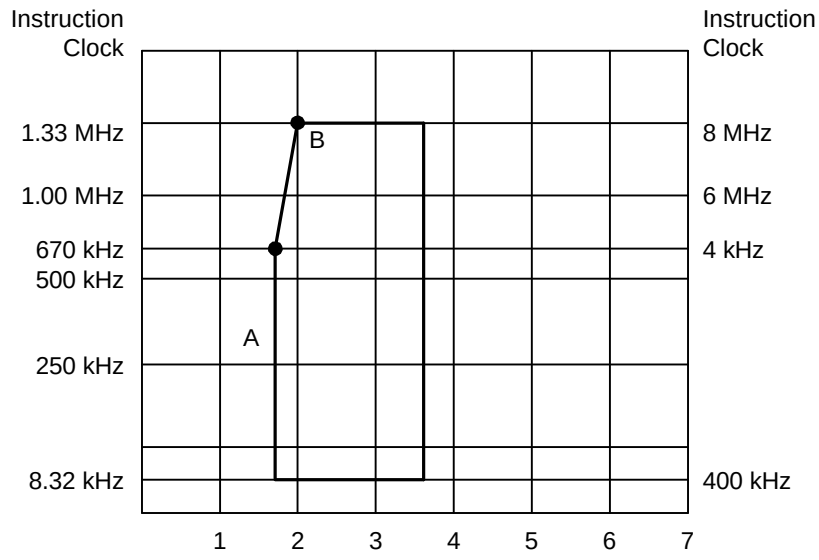
Oscillator	Clock Circuit	Conditions	Min	Typ	Max	Unit
Crystal		CPU clock oscillation frequency	1	–	8	MHz
Ceramic		CPU clock oscillation frequency	1	–	8	MHz
External clock		X_{IN} input frequency	1	–	8	MHz

Table 13-8. Oscillation Stabilization Time

(T_A = – 40 °C + 85 °C, V_{DD} = 3.6 V)

Oscillator	Test Condition	Min	Typ	Max	Unit
Main crystal	f_{OSC} > 400 kHz	–	–	20	ms
Main ceramic	Oscillation stabilization occurs when V_{DD} is equal to the minimum oscillator voltage range.	–	–	10	ms
External clock (main system)	X_{IN} input High and Low width (t_{XH}, t_{XL})	25	–	500	ns
Oscillator stabilization wait time	t_{WAIT} when released by a reset (1)	–	$2^{16}/f_{OSC}$	–	ms
	t_{WAIT} when released by an interrupt (2)	–	–	–	ms

NOTES:
1. f_{OSC} is the oscillator frequency.
2. The duration of the oscillation stabilization time (t_{WAIT}) when it is released by an interrupt is determined by the setting in the basic timer control register, BTCON.



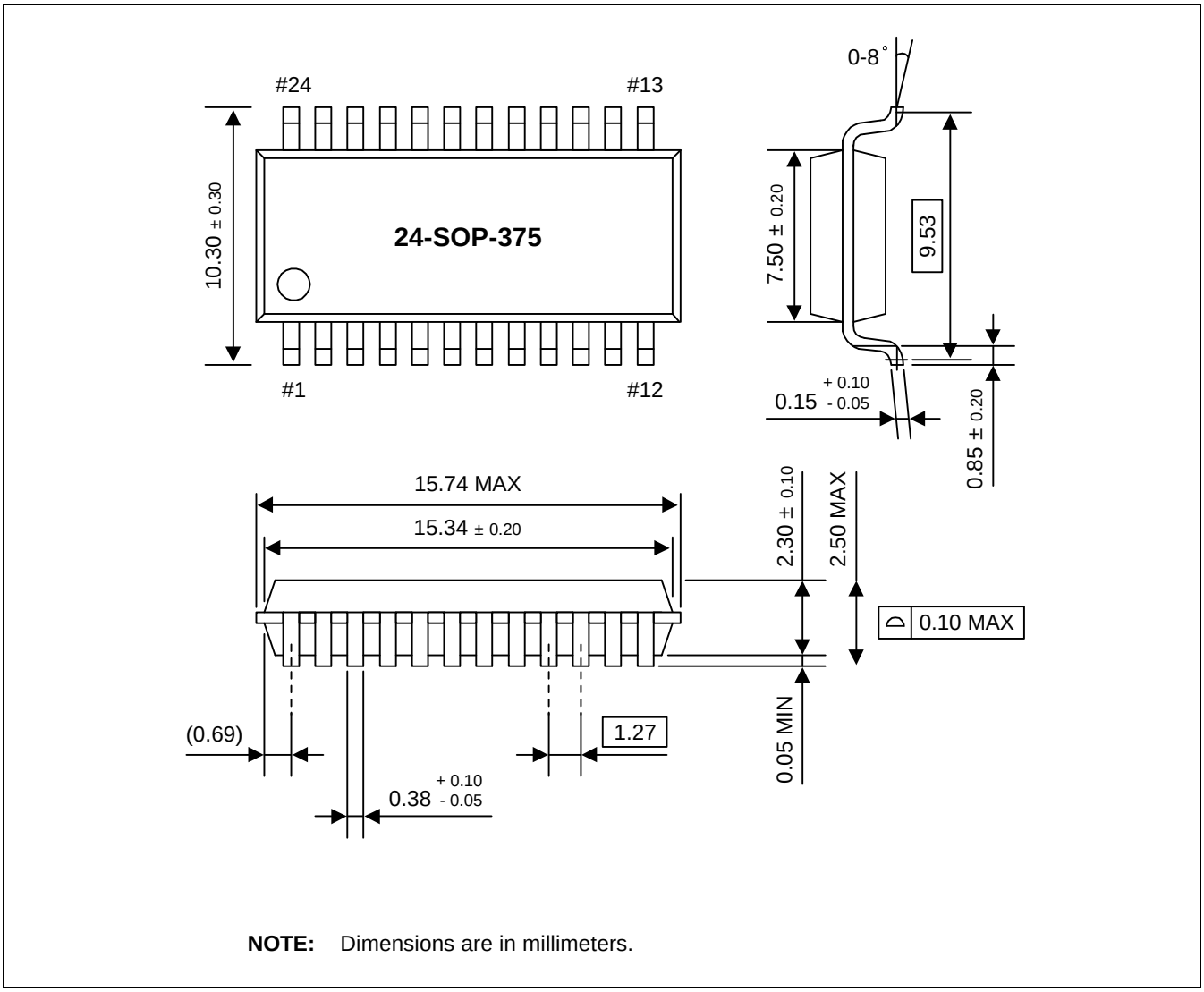
Instruction Clock = 1/6n x oscillator frequency (n = 1, 2, 8, 16)
A 1.7 V: 4 MHz
b 2.0 V: 8 MHz

Figure 13-2. Operating Voltage Range of S3C80A4/C80A8/C80A5/C80B4/C80B8/C80B5

14 MECHANICAL DATA

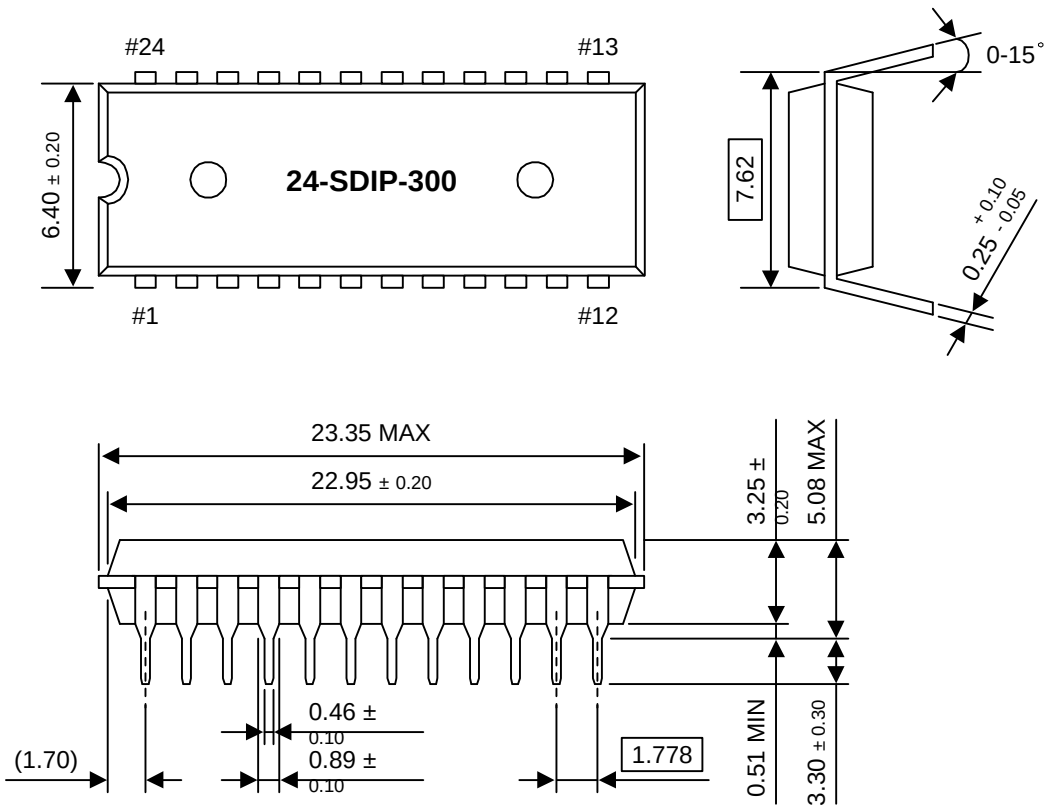
OVERVIEW

The S3C80A4/C80A8/C80A5/C80B4/C80B8/C80B5 microcontroller is currently available in a 24-pin SOP and SDIP package.



NOTE: Dimensions are in millimeters.

Figure 14-1. 24-Pin SOP Package Mechanical Data



NOTE: Dimensions are in millimeters.

Figure 14-2. 24-Pin SDIP Package Mechanical Data