4x128Kx72, 3.3V Sync/Sync Burst SRAM Dual Key DIMM

FEATURES

- 4x128Kx72 Synchronous, Synchronous Burst
- Access Speed(s): t_{KHQV} = 8.5, 10, 12, 15ns
- Flow-Through Architecture
- Linear and Sequential Burst Support via MODE pin
- Clock Controlled Registered Module Enable (EM\)
- Clock Controlled Registered Bank Enables (E_1\, E_2\, E_3\, E_4\)
- Clock Controlled Byte Write Mode Enable (BWE\)
- Clock Controlled Byte Write Enables (BW_{1-8}\)
- Clock Controlled Registered Address
- Clock Controlled Registered Global Write (GW\)
- Aysnchronous Output Enable (G\)
- Internally self-timed Write
- Individual Bank Sleep Mode enables (ZZ_1, ZZ_2, ZZ_3, ZZ_4)
- Gold Lead Finish
- 3.3V ± 10% Operation
- Common Data I/O
- High Capacitance (30pF) drive, at rated Access Speed
- Single total array Clock
- Multiple Vcc and Vss

The EDI2CG472128VxxD2 is a Synchronous/Synchronous Burst SRAM, 84 position Dual Key; Double High DIMM (168 contacts) Module, organized as 4x128Kx72. The Module contains eight (8) Synchronous Burst Ram Devices, packaged in the industry standard JEDEC 14mmx20mm TQFP placed on a Multilayer FR4 Substrate. The module architecture is defined as a Sync/Sync Burst, Flow-Through, with support for either linear or sequential burst. This module provides High Performance, 2-1-1-1 accesses when used in Burst Mode, and used as a Synchronous Only Mode, provides a high performance cost advantage over BiCMOS asynchronous device architectures.

Synchronous Only operations are performed via strapping ADSC\ Low, and ADSP\ / ADV\ High, which provides for Ultra Fast Accesses in Read Mode while providing for internally self-timed Early Writes.

Synchronous/Synchronous Burst operations are in relation to an externally supplied clock, Registered Address, Registered Global Write, Registered Enables as well as an Asynchronous Output enable. This Module has been defined with full flexibility, which allows individual control of each of the eight bytes, as well as Quad Words in both Read and Write Operations.

PIN CONFIGURATION

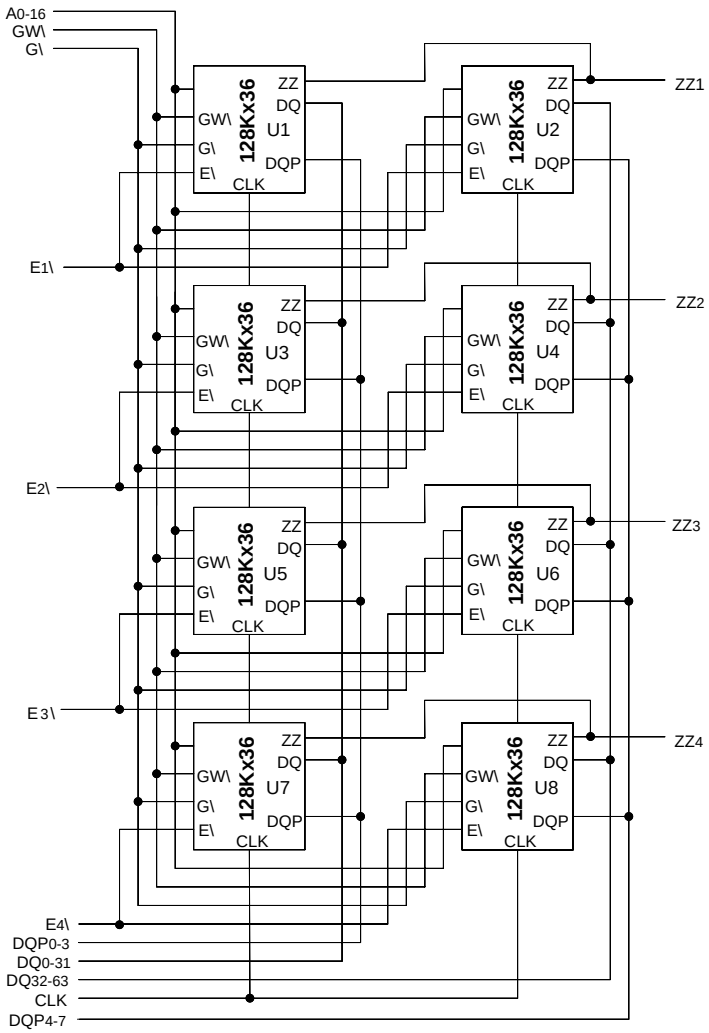
PIN SYMBOLS

PIN	FRONT	PIN	BACK	PIN	FRONT	PIN	BACK
1	VSS	85	VSS	43	NC	127	DQP2
2	A0	86	RFU	44	VCC	128	VCC
3	A16	87	A1	45	DQ16	129	DQ23
4	A2	88	A15	46	DQ17	130	DQ22
5	A14	89	A3	47	DQ18	131	DQ21
6	VCC	90	VCC	48	DQ19	132	DQ20
7	A4	91	A13	49	VSS	133	VSS
8	A12	92	A5	50	ZZ2	134	DQP3
9	A6	93	A11	51	VCC	135	VCC
10	A10	94	A7	52	DQ24	136	DQ31
11	VSS	95	VSS	53	DQ25	137	DQ30
12	A8	96	A9	54	DQ26	138	DQ29
13	RFU	97	RFU	55	DQ27	139	DQ28
14	E4\	98	E1\	56	VSS	140	VSS
15	E2\	99	E3\	57	NC	141	DQP4
16	VSS	100	VSS	58	VCC	142	VCC
17	MODE	101	CLK	59	DQ32	143	DQ39
18	EM\	102	VSS	60	DQ33	144	DQ38
19	GW\	103	G\	61	DQ34	145	DQ37
20	RFU	104	BWE\	62	DQ35	146	DQ36
21	VCC	105	VCC	63	VSS	147	VSS
22	BW4\	106	BW2\	64	ZZ3	148	DQP5
23	BW3\	107	BW1\	65	VCC	149	VCC
24	BW8\	108	BW6\	66	DQ40	150	DQ47
25	BW7\	109	BW5\	67	DQ41	151	DQ46
26	ADSC\	110	VSS	68	DQ42	152	DQ45
27	ADSP\	111	ADV\	69	DQ43	153	DQ44
28	VSS	112	VSS	70	VSS	154	VSS
29	NC	113	DQP0	71	NC	155	DQP6
30	VCC	114	VCC	72	VCC	156	VCC
31	DQ0	115	DQ7	73	DQ48	157	DQ55
32	DQ1	116	DQ6	74	DQ49	158	DQ54
33	DQ2	117	DQ5	75	DQ50	159	DQ53
34	DQ3	118	DQ4	76	DQ51	160	DQ52
35	VSS	119	VSS	77	VSS	161	VSS
36	ZZ1	120	DQP1	78	ZZ4	162	DQP7
37	VCC	121	VCC	79	VCC	163	VCC
38	DQ8	122	DQ15	80	DQ56	164	DQ63
39	DQ9	123	DQ14	81	DQ57	165	DQ62
40	DQ10	124	DQ13	82	DQ58	166	DQ61
41	DQ11	125	DQ12	83	DQ59	167	DQ60
42	VSS	126	VSS	84	VSS	168	VSS

PIN NAMES

DQ0-63	Input/Output Bus
DQP0-7	Parity Bits
A0-6	Address Bus
E1\, E2\, E3\, E4\	Synchronous Bank Enables
BWE\	Byte Write Mode Enable
BW1-8\	Byte Write Enables
CLK	Array Clock
GW\	Synchronous Global Write Enable
G\	Asynchronous Output Enable
ZZ1, ZZ2, ZZ3, ZZ4	Synchronous Bank Enables
Vcc	3.3V Power Supply
Vss	Ground
NC	No Connect

FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTIONS

DIMM Pins	Symbol	Type	Description
2, 87, 4, 89, 7, 92 9, 94, 12, 96, 10 93, 8, 91, 5, 88, 3	A_{0-16}	Input Synchronous	Addresses: These inputs are registered and must meet the setup and hold times around the rising edge of CLK. The burst counter generates internal addresses associated with A_0 and A_1, during burst and wait cycle.
107, 106, 23, 22, 109, 108, 25, 24	BW_1\, BW_1\, BW_3\, BW_4\, BW_5\, BW_6\, BW_7\, BW_8\	Input Synchronous	Byte Write: A byte write is LOW for a WRITE cycle and HIGH for a READ cycle. BW_0/ controls DQ_{0-7} and DQP_0, BW_1\ controls DQ_{8-15} and DQP_1. BW_2\ controls DQ_{16-23} and DQP_2. BW_3\ controls DQ_{24-31} and DQP_3. BW_4\ controls DQ_{32-39} and DQP_4. BW_5\ controls DQ_{40-47} and DQP_5. BW_6\ controls DQ_{48-55} and DQP_6. BW_7\ controls DQ_{56-64} and DQP_7.
104	BWE\	Input Synchronous	Write Enable: This active LOW input gates byte write operations and must meet the setup and hold times around the rising edge of CLK.
19	GW\	Input Synchronous	Global Write: This active LOW input allows a full 72-bit WRITE to occur independent of the BWE\ and BWx\ lines and must meet the setup and hold times around the rising edge of CLK.
101	CLK	Input Synchronous	Clock: This signal registers the addresses, data, chip enables, write control and burst control inputs on its rising edge. All synchronous inputs must meet setup and hold times around the clock's rising edge.
98, 15, 99,14	E_1\, E_2\ E_3\, E_4\	Input Synchronous	Bank Enables: These active LOW inputs are used to enable each individual bank and to gate ADSP\.
103	G\	Input	Output Enable: This active LOW asynchronous input enables the data output drivers.
111	ADV\	Input Synchronous	Address Status Processor: This active LOW input is used to control the internal burst counter. A HIGH on this pin generates wait cycle (no address advance).
27	ADSP\	Input Synchronous	Address Status Processor: This active LOW input, along with EL\ and EH\ being LOW, causes a new external address to be registered and a READ cycle is initiated using the new address.
26	ADSC\	Input Synchronous	Address Status Controller: This active LOW input causes device to be de-selected or selected along with new external address to be registered. A READ or WRITE cycle is initiated depending upon write control inputs.
17	MODE	Input Static	Mode: This input selects the burst sequence. A LOW on this pin selects LINEAR BURST. A NC or HIGH on this pin selects INTERLEAVED BURST.
36, 50, 64, 78	ZZ_1, ZZ_2, ZZ_3, ZZ_4	Input Asynchronous	Snooze: These active HIGH inputs put the individual banks in low power consumption standby mode. For normal operation, this input has to be either LOW or NC (no connect).
Various	DQ_{0-63}	Input/Output	Data Inputs/Outputs: First byte is DQ_{0-7}, second byte is DQ_{8-15}, third byte is DQ_{16-23}, fourth byte is DQ_{24-31}, fifth byte is DQ_{32-39}, sixth byte is DQ_{40-47}, seventh byte is DQ_{48-55} and the eight byte is DQ_{56-64}.
113, 120, 127, 134, 141, 148, 155, 162	DQP_{0-7}	Input/Output	Parity Inputs/Outputs: DQP_0 is parity bit for DQ_{0-7}. DQP_1 is parity bit for DQ_{8-15}. DQP_2 is parity bit for DQ_{16-23}. DQP_3 is parity bit for DQ_{24-31}. DQP_4\ is parity bit for $DQ3_{2-39}$. DQP_5 is parity bit for DQ_{40-47}. DQP_6\ is parity bit for DQ_{48-55}. DQP_7 is parity bit for DQ_{56-64} and DQP_7. In order to use the device configured as a 128K x 64, the parity bits need to be tied to Vss through a 10K ohm resistor.
Various	Vcc	Supply	Core power supply: +3.3V -5%/+10%
Various	Vss	Ground	Ground

SYNCHRONOUS BURST - TRUTH TABLE

Operation	E1\	E2\	E3\	E4\	ADSP\	ADSC\	ADV\	GW\	G\	CLK	DQ	Addr. Used
Deselected Cycle, Power Down; Bank 1	H	X	*	*	X	L	X	X	X	L-H	High-Z	None
Deselected Cycle, Power Down; Bank 2	X	H	*	*	X	L	X	X	X	L-H	High-Z	None
Read Cycle, Begin Burst; Bank 1	L	H	*	*	L	X	X	X	L	L-H	Q	External
Read Cycle, Begin Burst; Bank 1	L	H	*	*	L	X	X	X	H	L-H	High-Z	External
Read Cycle, Begin Burst; Bank 2	H	L	*	*	L	X	X	X	L	L-H	Q	External
Read Cycle, Begin Burst; Bank 2	H	L	*	*	L	X	X	X	H	L-H	High-Z	External
Write Cycle, Begin Burst; Bank 1	L	H	*	*	H	L	X	L	X	L-H	D	External
Write Cycle, Begin Burst; Bank 2	H	L	*	*	H	L	X	L	X	L-H	D	External
Read Cycle, Begin Burst; Bank 1	L	H	*	*	H	L	X	H	L	L-H	Q	External
Read Cycle, Begin Burst; Bank 1	L	H	*	*	H	L	X	H	H	L-H	High-Z	External
Read Cycle, Begin Burst; Bank 2	H	L	*	*	H	L	X	H	L	L-H	Q	External
Read Cycle, Begin Burst; Bank 2	H	L	*	*	H	L	X	H	H	L-H	High-Z	External
Read Cycle, Continue Burst; Bank 1	X	H	*	*	X	H	L	H	L	L-H	Q	Next
Read Cycle, Continue Burst; Bank 1	X	H	*	*	X	H	L	H	H	L-H	High-Z	Next
Read Cycle, Continue Burst; Bank 2	H	X	*	*	X	H	L	H	L	L-H	Q	Next
Read Cycle, Continue Burst; Bank 2	H	X	*	*	X	H	L	H	H	L-H	High-Z	Next
Read Cycle, Continue Burst; Bank 1	H	H	*	*	X	H	L	H	L	L-H	Q	Next
Read Cycle, Continue Burst; Bank 1	H	H	*	*	X	H	L	H	H	L-H	High-Z	Next
Read Cycle, Continue Burst; Bank 2	H	H	*	*	X	H	L	H	L	L-H	Q	Next
Read Cycle, Continue Burst; Bank 2	H	H	*	*	X	H	L	H	H	L-H	High-Z	Next
Write Cycle, Continue Burst; Bank 1	X	H	*	*	H	H	L	L	X	L-H	D	Next
Write Cycle, Continue Burst; Bank 1	H	H	*	*	X	H	L	L	X	L-H	D	Next
Write Cycle, Continue Burst; Bank 2	H	X	*	*	H	H	L	L	X	L-H	D	Next
Write Cycle, Continue Burst; Bank 2	H	H	*	*	X	H	L	L	X	L-H	D	Next
Read Cycle, Suspend Burst; Bank 1	X	H	*	*	H	H	H	H	L	L-H	Q	Current
Read Cycle, Suspend Burst; Bank 1	X	H	*	*	H	H	H	H	H	L-H	High-Z	Current
Read Cycle, Suspend Burst; Bank 2	H	X	*	*	H	H	H	H	L	L-H	Q	Current
Read Cycle, Suspend Burst; Bank 2	H	X	*	*	H	H	H	H	H	L-H	High-Z	Current
Read Cycle, Suspend Burst; Bank 1	H	H	*	*	X	H	H	H	L	L-H	Q	Current
Read Cycle, Suspend Burst; Bank 1	H	H	*	*	X	H	H	H	H	L-H	High-Z	Current
Read Cycle, Suspend Burst; Bank 2	H	H	*	*	X	H	H	H	L	L-H	Q	Current
Read Cycle, Suspend Burst; Bank 2	H	H	*	*	X	H	H	H	H	L-H	High-Z	Current
Write Cycle, Suspend Burst; Bank 1	X	H	*	*	H	H	H	L	X	L-H	D	Current
Write Cycle, Suspend Burst; Bank 1	H	H	*	*	X	H	H	L	X	L-H	D	Current
Write Cycle, Suspend Burst; Bank 2	H	X	*	*	H	H	H	L	X	L-H	D	Current
Write Cycle, Suspend Burst; Bank 2	H	H	*	*	X	H	H	L	X	L-H	D	Current

*All Truth Table Functions Repeat for Bank 3 (E_3\) and Bank 4 (E_4\)

SYNCHRONOUS ONLY - TRUTH TABLE

Operation	E1\	E2\	E3\	E4\	GW\	G\	ZZ	CLK	DQ
Synchronous Write-Bank 1	L	H	H	H	L	H	L	↑	High-Z
Synchronous Read-Bank 1	L	H	H	H	H	L	L	↑	
Synchronous Write-Bank 2	H	L	H	H	L	H	L	↑	High-Z
Synchronous Read-Bank 2	H	L	H	H	H	L	L	↑	
Synchronous Write-Bank 3	H	H	L	H	L	H	L	↑	High-Z
Synchronous Read-Bank 3	H	H	L	H	H	L	L	↑	
Synchronous Write-Bank 4	H	H	H	L	L	H	L	↑	High-Z
Synchronous Read-Bank 4	H	H	H	L	H	L	L	↑	
Snooze Mode	X	X	X	X	X	X	H	X	High-Z

ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc Relative to Vss	-0.5V to +4.6V
Vin	-0.5V to Vcc +0.5V
Storage Temperature	-55°C to +125°C
Operating Temperature (Commercial)	0°C to +70°C
Operating Temperature (Industrial)	-40°C to +85°C
Short Circuit Output Current	10 mA

*Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions greater than those indicated in operational sections of this specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

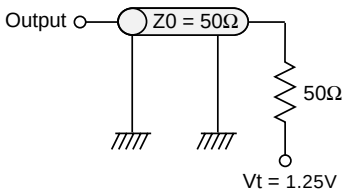
RECOMMENDED DC OPERATING CONDITIONS

Parameter	Sym	Min	Typ	Max	Units
Supply Voltage	V_{CC}	3.14	3.3	3.6	V
Supply Voltage	V_{SS}	0.0	0.0	0.0	V
Input High	V_{IH}	2.2	3.0	V_{CC} +0.3	V
Input Low	V_{IL}	-0.3	0.0	0.3	V
Input Leakage	I_{LI}	-2	1	2	µA
Output Leakage	I_{LO}	-2	1	2	µA

DC ELECTRICAL CHARACTERISTICS - READ CYCLE

Description	Symbol	Typ	Max 8.5	Max 10	Max 12	Max 15	Units
Power Supply Current	I_{CC1}	2.0	2.9	2.7	2.7	2.5	A
Power Supply Current Device Selected,No Operation	Icc	875	1.8	1.8	1.3	1.3	A
Snooze Mode	IccZZ	500	700	700	700	700	mA
CMOS Standby	I_{CC3}	270	300	350	350	350	mA
Clock Running-Deselect	IccK	900	1.1	1.1	1.0	1.0	A

AC TEST CIRCUIT



AC Output Load Equivalent

AC TEST CONDITIONS

Parameter	I/O	Unit
Input Pulse Levels	V_{SS} to 3.0	V
Input and Output Timing Levels	1.25	V
Output Test Equivalencies	See figure, at left	

BURST ADDRESS TABLE (MODE = NC/Vcc)

First Address (external)	Second Address (internal)	Third Address (internal)	Fourth Address (internal)
A..A00	A..A01	A..A10	A..A11
A..A01	A..A00	A..A11	A..A10
A..A10	A..A11	A..A00	A..A01
A..A11	A..A10	A..A01	A..A00

BURST ADDRESS TABLE (MODE = Vss)

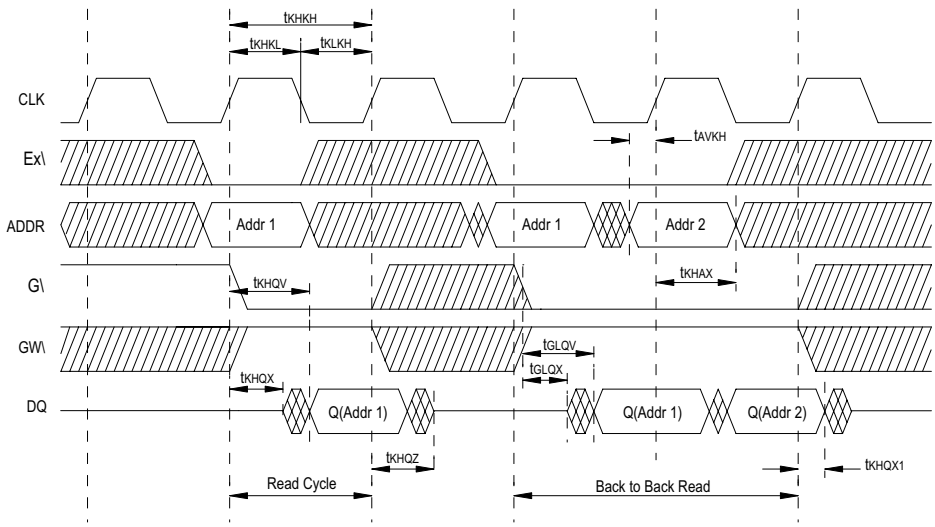
First Address (external)	Second Address (internal)	Third Address (internal)	Fourth Address (internal)
A..A00	A..A01	A..A10	A..A11
A..A01	A..A10	A..A11	A..A00
A..A10	A..A11	A..A00	A..A01
A..A11	A..A00	A..A01	A..A10

READ CYCLE TIMING PARAMETERS

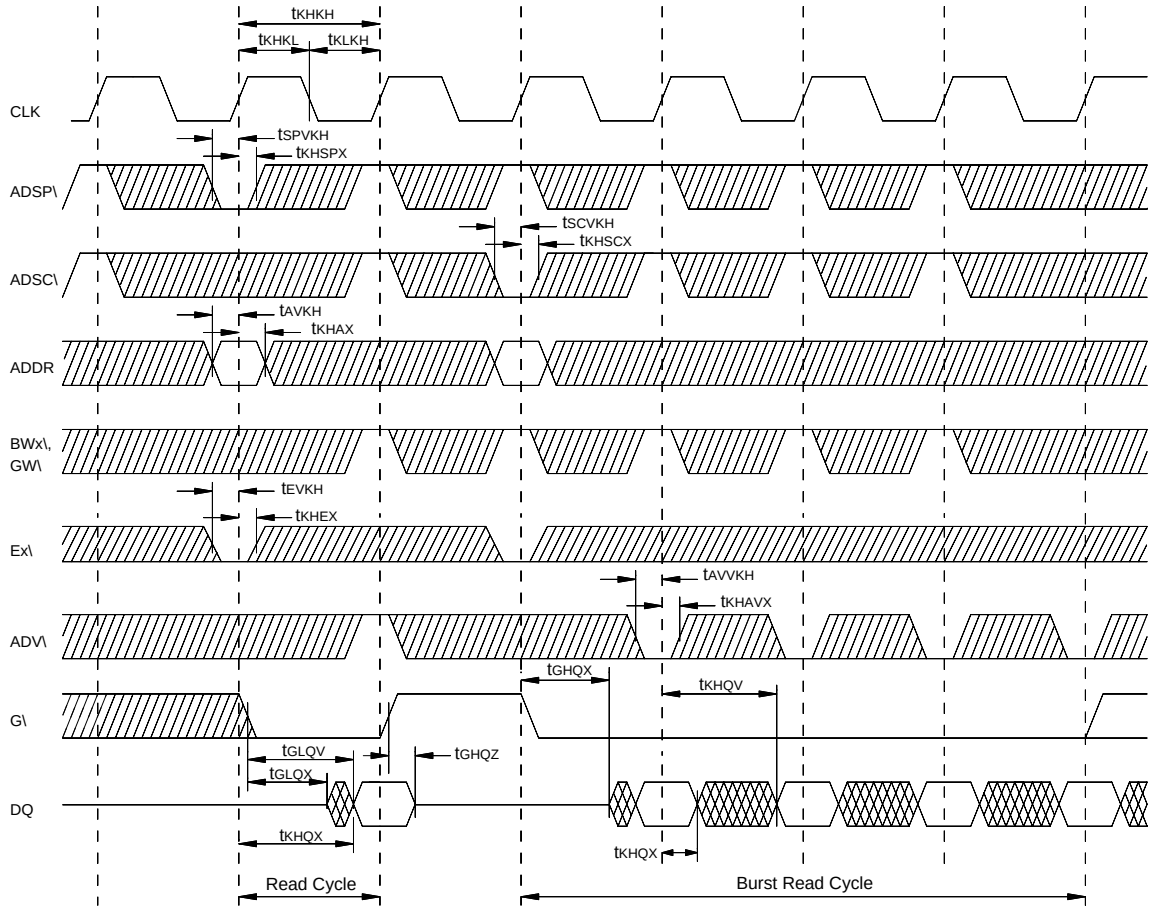
Description	Sym	8.5ns Min	8.5ns Max	10ns Min	10ns Max	12ns Min	12ns Max	15ns Min	15ns Max	Units
Clock Cycle Time	t_{KHKH}	*	*	15		15		20		ns
Clock High Time	t_{KHKL}	*	*	5		5		6		ns
Clock Low Time	t_{KLKH}	*	*	5		5		6		ns
Clock to Output Valid	t_{KHQV}	*	*		10		12		15	ns
Clock to Output Invalid	t_{KHQX1}	*	*	3		3		3		ns
Clock to Output Low-Z	t_{KHQX}	*	*	4		4		4		ns
Output Enable to Output Valid	t_{GLQV}	*	*		5		5		6	ns
Output Enable to Output Low-Z	t_{GLQX}	*	*	0		0		0		ns
Output Enable to Output High-Z	t_{GHQZ}	*	*		5		5		5	ns
Address Setup	t_{AVKH}	*	*	2.5		2.5		2.5		ns
Bank Enable Setup	t_{EVKH}	*	*	2.5		2.5		2.5		ns
Address Hold	t_{KHAX}	*	*	1.0		1.0		1.0		ns
Bank Enable Hold	t_{KHEX}	*	*	1.0		1.0		1.0		ns

**TBD*

SYNCHRONOUS ONLY READ CYCLE



SYNCHRONOUS-BURST READ CYCLE

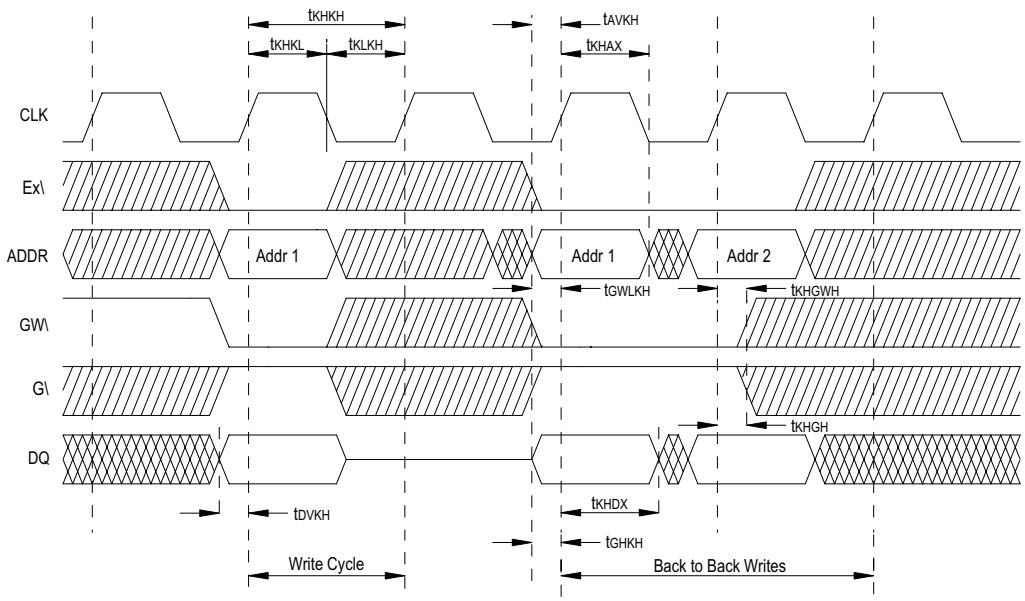


WRITE CYCLE TIMING PARAMETERS

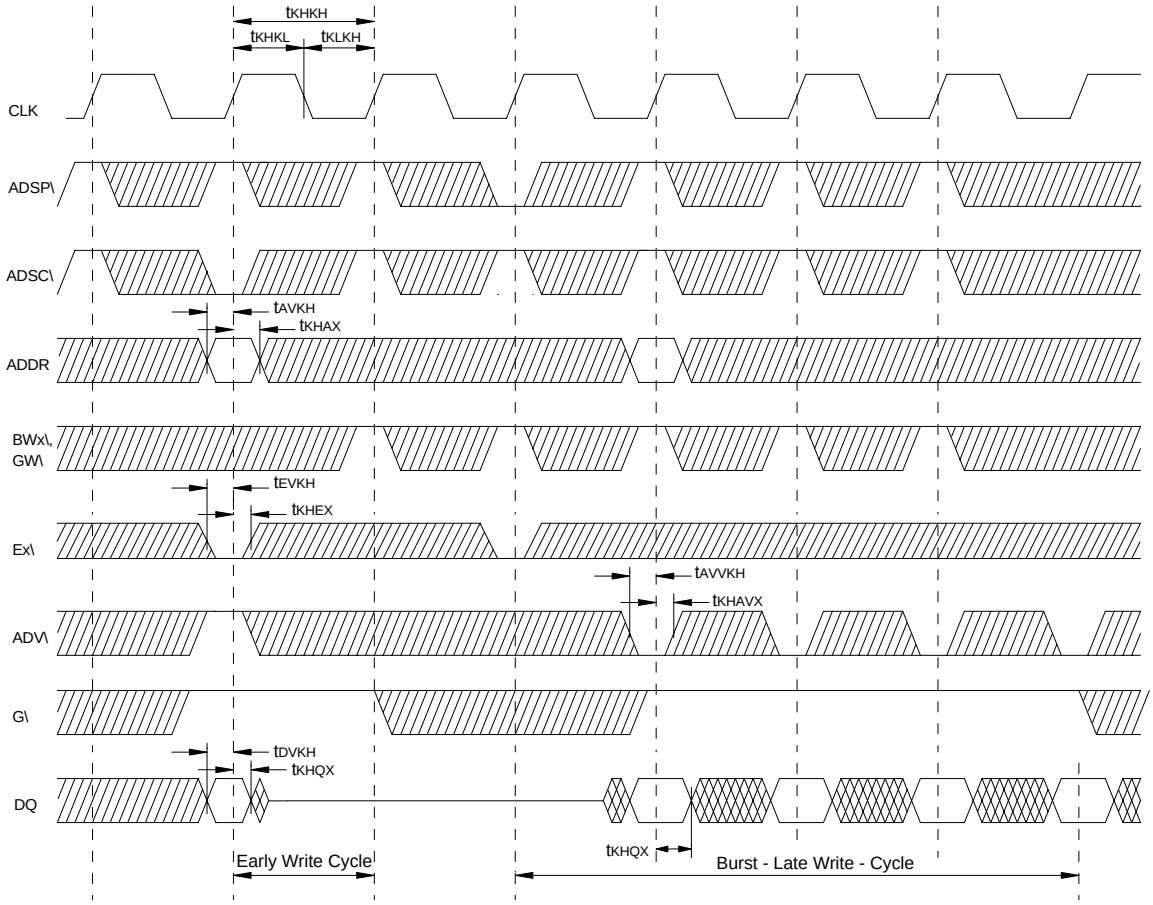
Description	Sym	8.5ns Min	8.5ns Max	10ns Min	10ns Max	12ns Min	12ns Max	15ns Min	15ns Max	Units
Clock Cycle Time	t_{KHKH}	*	*	15		15		20		ns
Clock High Time	t_{KHKL}	*	*	5		5		6		ns
Clock Low Time	t_{KLKH}	*	*	5		5		6		ns
Address Setup	t_{AVKH}	*	*	2.5		2.5		2.5		ns
Address Hold	t_{KHAX}	*	*	1.0		1.0		1.0		ns
Bank Enable Setup	t_{EVKH}	*	*	2.5		2.5		2.5		ns
Bank Enable Hold	t_{KHEX}	*	*	1.0		1.0		1.0		ns
Global Write Enable Setup	t_{WVKH}	*	*	2.5		2.5		2.5		ns
Global Write Enable Hold	t_{KHWX}	*	*	1.0		1.0		1.0		ns
Data Setup	t_{DVKH}	*	*	2.5		2.5		2.5		ns
Data Hold	t_{KHDX}	*	*	1.0		1.0		1.0		ns

**TBD*

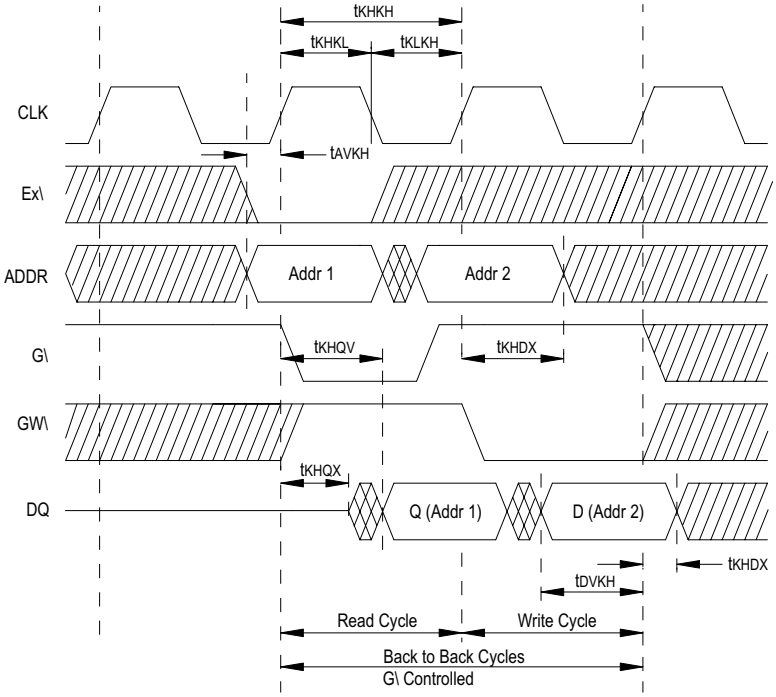
SYNCHRONOUS (NON-BURST) WRITE CYCLE



SYNCHRONOUS-BURST WRITE CYCLE

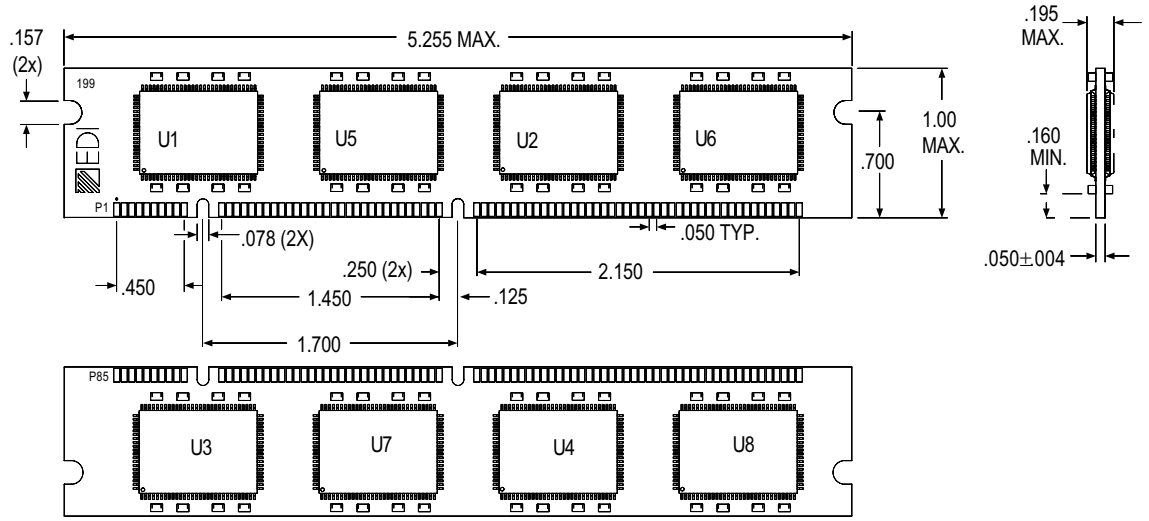


SYNCHRONOUS (NON-BURST) READ/WRITE CYCLE



PACKAGE DESCRIPTION: 168 GOLD LEAD DIMM

Package No. 410



ALL DIMENSIONS ARE IN INCHES

ORDERING INFORMATION

Part Number	Organization	Voltage	Speed (ns)	Package
EDI2CG472128V85D2*	4x128Kx72	3.3	8.5	168 Gold Lead DIMM
EDI2CG472128V10D2*	4x128Kx72	3.3	10	168 Gold Lead DIMM
EDI2CG472128V12D2	4x128Kx72	3.3	12	168 Gold Lead DIMM
EDI2CG472128V15D2	4x128Kx72	3.3	15	168 Gold Lead DIMM

**Consult Factory for Availability*